On Compaction-Based Concurrent Error Detection

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1. Extended Abstract

We examine a low-cost, zero-latency, non-intrusive CED method for restricted error models. The method is based on compaction of the circuit outputs, prediction of the compacted responses, and comparison. As opposed to duplication-based CED, which targets the unrestricted error model, this method achieves significant hardware cost reduction by utilizing the information available through a restricted error model. We assume that the error model is not defined through permanent or transient faults in the hardware, but rather in terms of the erroneous behavior that such faults induce. Thus, any fault model can be prescribed by providing for every input combination the error-free response and all erroneous responses resulting from faults in the model. Consider a combinational circuit with m inputs and n outputs. For every input combination $a \in [0, \ldots, 2^m - 1]$, we define the error-free response of the circuit as $GM(a)$, the set of erroneous responses resulting from faults in the prescribed fault model as $BM(a)$, and the set of responses that will never occur for faults in the prescribed fault model as $DC(a)$. For every input a, the CED circuit needs to distinguish between the error-free response $GM(a)$ and erroneous responses in the set $BM(a)$, but not between the error-free response $GM(a)$ and erroneous responses in the set $DC(a)$, since the latter will never occur for targeted faults.Thus, the proposed scheme utilizes an alias-free compactor is added to compact the n-bit output into k bits, sufficient to distinguish between error-free and possible erroneous responses. A predictor is consequently required to predict the value of the k-bit responses for each m-bit input. Finally, a k-bit comparator is employed to indicate any discrepancy between the predicted and the actual compacted response. A compactor is alias-free if the k-bit compacted error-free response $GM(a)$ differs from all k-bit compacted erroneous responses in $BM(a)$, $\forall a \in [0, \ldots, 2^m - 1]$. The compaction can be achieved by constructing a conflict graph and solving for the minimum number of colors needed to color the graph. More specifically, the k outputs of the compactor correspond to the bits necessary to represent the number of distinct colors of the graph. Minimization of the number of necessary colors results in minimization of k and, on average, minimization of the cost of the compactor and the predictor. We experiment with arbitrary circuits that were generated through tables filled uniformly at random. In these experiments, the circuits have an equal number of inputs and outputs and the restricted error model comprises all errors resulting from the single stuck-at fault model. The circuits are synthesized and internally developed software employing fault simulation is used to identify the error-free and erroneous responses, generate the conflict graph and apply a graph coloring heuristic to color the nodes of the conflict graph and assign random binary codes to each color. The functionality of the compactor and the predictor is defined through assignment of binary codes to each node. Addition of a simple comparator completes the construction of the proposed CED method. The proposed method is compared to duplication-based CED in the table of Figure 1. As can be seen, duplication is cheaper for the smaller circuits, while the proposed method outperforms duplication for the larger circuits due to the density of the conflict graph. As the circuit size increases, the number of erroneous responses per error-free response appears to be growing much slower than the exponentially growing number of possible responses. As a result, conflict graphs become sparser and the number of bits necessary to color them is a diminishing proportion of the output width. Thus, as the circuit size increases, the proposed CED method is expected to provide higher savings over duplication-based CED.

	Duplication (D) (Unrestricted Error Model)			Proposed Compaction-Based Method (PM) (Restricted Error Models)						
Circuit	Replica	Comparator	Total	Compactor	Predictor	Comparator	Colors	Bits	Total	PM/D
4 I/O	46864	24592	71456	31088	39904	18096	5	3	89088	1.247
5 I/O	100224	31088	131312	67744	77024	18096	6	3	162864	1.240
6 I/O	251488	37584	289072	147552	149872	18096	8	3	315520	1.092
7 I/O	541952	44080	586032	220400	254272	18096	7	3	492768	0.841
8 I/O	1332144	50576	1382720	247312	336400	11600	4	2	595312	0.431
9 I/O	2786784	57072	2837360	558656	645424	11600	4	2	1215680	0.429
10 I/O	6265856	63568	6329424	880672	1092720	18096	5	3	1991488	0.314

Figure 1. Comparison of the proposed method to duplication-based CED

Proceedings of the 9th IEEE International On-Line Testing Symposium (IOLTS'03)
0-7695-1968-7/03 $17.00 © 2003 IEEE