Supporting Interdisiplinary Domain Specific Architecture Research with Reconfigurable Devices

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For better and for worse, much computer architecture research is highly theoretical. Few results make the jump from simulation to implementation, and if they do it comes with significant expense both in terms of time and money. When an architecture design requires a diverse set of expertise, as is the case with network, security, and signal processors, this is a serious impediment to interdisciplinary collaboration.

In our experience, it is critical to the success of a project and its impact across disciplines, to include domain experts from other fields. Domain experts can quickly summarize the state of the art in the field and predict possible future directions. Without their involvement, one can easily fall into the trap of searching the web for "benchmarks" that were written 10 years ago and are no longer applicable to the problems encountered in real designs. For example, it would be easy to assume that a patricia-trie is a critical data structure for network processors if one did a simple search for network code, when in fact the state of the art in network algorithms has advanced far beyond this method.

The problem in getting domain experts to engage in real collaboration is that at the end of the day our collaborators want a physical device that they can use to solve or study the problems they face. In fact, we would argue that this is a critical step, as only through deployment can our users provide feedback and application level changes that can be used to iteratively improve our approach. Closing this feedback loop is both critical and difficult

Reconfigurable devices offer an opportunity to close this gap. It is unlikely at best that an FPGA based implementation will be able to match a custom design in terms of performance or density. Coming close to the performance of even a structured ASIC is difficult and requires careful tuning of the design and its compilation. A key point that we believe should be discussed is *how and when we should draw the line between building a functional and useful prototype, and when time is being wasted over-engineering for performanc*e.

We believe that care must be taken in applying any optimization that does not have a clear analog in the custom design space (unless the goal is to develop an architecture specifically for instantiation on a reconfigurable device). While this may mean that the cycle-times and density of our research prototypes will not be indicative of the fully engineered solution, it will guide many critical decisions as to how a machine can best be organized. In other words, what is great for architecture research may not be adequate for micro-architecture research.

This also brings up an important point, the changing role of the computer architect. Many applications are now being built specifically for implementation on advanced reconfigurable devices (with block RAMs and hardware multipliers, these devices are no longer a simple sea of gates) and it is clear that soft-architectures will have to be developed to accommodate this new method of implementation.

In our talk, we will present a brief overview of our FPGA prototyping experience for the purposes of interdisciplinary collaboration, both good and bad. Currently we have three different projects and various stages. Our first design (and the one that is furthest along) is being built to provide a functional platform for high-speed multi-path cancellation in wireless communication and radio location. Our second design is a prototype of a new class of string matching algorithms for intrusion detection. Our third project is a more general network and security processor which is just now being architected. All three of these projects happened in collaboration with domain experts, and we plan to discuss our experiences, lessons learned, and the lessons we hope to learn in the near future.