NOTE: The Intel 64 and IA-32 Architectures Software Developer's Manual consists of three volumes: Basic Architecture, Order Number 253665; Instruction Set Reference A-Z, Order Number 325383; System Programming Guide, Order Number 325384. Refer to all three volumes when evaluating your design needs.
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The Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volumes 2A, 2B & 2C: Instruction Set Reference (order numbers 253666, 253667 and 326018) are part of a set that describes the architecture and programming environment of all Intel 64 and IA-32 architecture processors. Other volumes in this set are:

- The Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1: Basic Architecture (Order Number 253665).

The Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, describes the basic architecture and programming environment of Intel 64 and IA-32 processors. The Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volumes 2A, 2B & 2C, describe the instruction set of the processor and the opcode structure. These volumes apply to application programmers and to programmers who write operating systems or executives. The Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volumes 3A, 3B & 3C, describe the operating-system support environment of Intel 64 and IA-32 processors. These volumes target operating-system and BIOS designers. In addition, the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B, addresses the programming environment for classes of software that host operating systems.

### 1.1 IA-32 Processors Covered in This Manual

This manual set includes information pertaining primarily to the most recent Intel 64 and IA-32 processors, which include:

- Pentium® processors
- P6 family processors
- Pentium® 4 processors
- Pentium® M processors
- Intel® Xeon® processors
- Pentium® D processors
- Pentium® processor Extreme Editions
- 64-bit Intel® Xeon® processors
- Intel® Core™ Duo processor
- Intel® Core™ Solo processor
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- Dual-Core Intel® Xeon® processor LV
- Intel® Core™2 Duo processor
- Intel® Core™2 Quad processor Q6000 series
- Intel® Xeon® processor 3000, 3200 series
- Intel® Xeon® processor 5000 series
- Intel® Xeon® processor 5100, 5300 series
- Intel® Core™2 Extreme processor X7000 and X6800 series
- Intel® Core™2 Extreme QX6000 series
- Intel® Xeon® processor 7100 series
- Intel® Pentium® Dual-Core processor
- Intel® Xeon® processor 7200, 7300 series
- Intel® Xeon® processor 5200, 5400, 7400 series
- Intel® Core™2 Extreme processor QX9000 and X9000 series
- Intel® Core™2 Quad processor Q9000 series
- Intel® Core™2 Duo processor E8000, T9000 series
- Intel® Atom™ processor family
- Intel® Core™ i7 processor
- Intel® Core™ i5 processor
- Intel® Xeon® processor E7-8800/4800/2800 product families

P6 family processors are IA-32 processors based on the P6 family microarchitecture. This includes the Pentium® Pro, Pentium® II, Pentium® III, and Pentium® III Xeon® processors.


The Intel® Core™ Duo, Intel® Core™ Solo and dual-core Intel® Xeon® processor LV are based on an improved Pentium® M processor microarchitecture.

The Intel® Xeon® processor 3000, 3200, 5100, 5300, 7200, and 7300 series, Intel® Pentium® dual-core, Intel® Core™2 Duo, Intel® Core™2 Quad, and Intel® Core™2 Extreme processors are based on Intel® Core™ microarchitecture.

The Intel® Xeon® processor 5200, 5400, 7400 series, Intel® Core™2 Quad processor Q9000 series, and Intel® Core™2 Extreme processors QX9000, X9000 series, Intel® Core™2 processor E8000 series are based on Enhanced Intel® Core™ microarchitecture.

The Intel® Atom™ processor family is based on the Intel® Atom™ microarchitecture and supports Intel 64 architecture.
The Intel® Core™ i7 processor and the Intel® Core™ i5 processor are based on the Intel® microarchitecture code name Nehalem and support Intel 64 architecture.

Processors based on Intel® microarchitecture code name Westmere support Intel 64 architecture.

P6 family, Pentium® M, Intel® Core™ Solo, Intel® Core™ Duo processors, dual-core Intel® Xeon® processor LV, and early generations of Pentium 4 and Intel Xeon processors support IA-32 architecture. The Intel® Atom™ processor Z5xx series support IA-32 architecture.

The Intel® Xeon® processor E7-8800/4800/2800 product families, Intel® Xeon® processor 3000, 3200, 5000, 5100, 5200, 5300, 5400, 7100, 7200, 7300, 7400 series, Intel® Core™2 Duo, Intel® Core™2 Extreme, Intel® Core™2 Quad processors, Pentium® D processors, Pentium® Dual-Core processor, newer generations of Pentium 4 and Intel Xeon processor family support Intel® 64 architecture.

IA-32 architecture is the instruction set architecture and programming environment for Intel's 32-bit microprocessors.

Intel® 64 architecture is the instruction set architecture and programming environment which is the superset of Intel's 32-bit and 64-bit architectures. It is compatible with the IA-32 architecture.

1.2 OVERVIEW OF VOLUME 2A, 2B AND 2C: INSTRUCTION SET REFERENCE

A description of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volumes 2A, 2B & 2C, content follows:

Chapter 1 — About This Manual. Gives an overview of all seven volumes of the Intel® 64 and IA-32 Architectures Software Developer’s Manual. It also describes the notational conventions in these manuals and lists related Intel® manuals and documentation of interest to programmers and hardware designers.

Chapter 2 — Instruction Format. Describes the machine-level instruction format used for all IA-32 instructions and gives the allowable encodings of prefixes, the operand-identifier byte (ModR/M byte), the addressing-mode specifier byte (SIB byte), and the displacement and immediate bytes.

Chapter 3 — Instruction Set Reference, A-L. Describes Intel 64 and IA-32 instructions in detail, including an algorithmic description of operations, the effect on flags, the effect of operand- and address-size attributes, and the exceptions that may be generated. The instructions are arranged in alphabetical order. General-purpose, x87 FPU, Intel MMX™ technology, SSE/SSE2/SSE3/SSSE3/SSE4 extensions, and system instructions are included.

Chapter 4 — Instruction Set Reference, M-Z. Continues the description of Intel 64 and IA-32 instructions started in Chapter 3. It provides the balance of the alpha-
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betized list of instructions and starts Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B.

Chapter 5—Safer Mode Extensions Reference. Describes the safer mode extensions (SMX). SMX is intended for a system executive to support launching a measured environment in a platform where the identity of the software controlling the platform hardware can be measured for the purpose of making trust decisions. This chapter starts Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2C.

Appendix A — Opcode Map. Gives an opcode map for the IA-32 instruction set.

Appendix B — Instruction Formats and Encodings. Gives the binary encoding of each form of each IA-32 instruction.

Appendix C — Intel® C/C++ Compiler Intrinsics and Functional Equivalents. Lists the Intel® C/C++ compiler intrinsics and their assembly code equivalents for each of the IA-32 MMX and SSE/SSE2/SSE3 instructions.

1.3 NOTATIONAL CONVENTIONS

This manual uses specific notation for data-structure formats, for symbolic representation of instructions, and for hexadecimal and binary numbers. A review of this notation makes the manual easier to read.

1.3.1 Bit and Byte Order

In illustrations of data structures in memory, smaller addresses appear toward the bottom of the figure; addresses increase toward the top. Bit positions are numbered from right to left. The numerical value of a set bit is equal to two raised to the power of the bit position. IA-32 processors are “little endian” machines; this means the bytes of a word are numbered starting from the least significant byte. Figure 1-1 illustrates these conventions.
1.3.2 Reserved Bits and Software Compatibility

In many register and memory layout descriptions, certain bits are marked as **reserved**. When bits are marked as reserved, it is essential for compatibility with future processors that software treat these bits as having a future, though unknown, effect. The behavior of reserved bits should be regarded as not only undefined, but unpredictable. Software should follow these guidelines in dealing with reserved bits:

- Do not depend on the states of any reserved bits when testing the values of registers which contain such bits. Mask out the reserved bits before testing.
- Do not depend on the states of any reserved bits when storing to memory or to a register.
- Do not depend on the ability to retain information written into any reserved bits.
- When loading a register, always load the reserved bits with the values indicated in the documentation, if any, or reload them with values previously read from the same register.

**NOTE**

Avoid any software dependence upon the state of reserved bits in IA-32 registers. Depending upon the values of reserved register bits will make software dependent upon the unspecified manner in which the processor handles these bits. Programs that depend upon reserved values risk incompatibility with future processors.
1.3.3 Instruction Operands

When instructions are represented symbolically, a subset of the IA-32 assembly language is used. In this subset, an instruction has the following format:

label: mnemonic argument1, argument2, argument3

where:

• A label is an identifier which is followed by a colon.
• A mnemonic is a reserved name for a class of instruction opcodes which have the same function.
• The operands argument1, argument2, and argument3 are optional. There may be from zero to three operands, depending on the opcode. When present, they take the form of either literals or identifiers for data items. Operand identifiers are either reserved names of registers or are assumed to be assigned to data items declared in another part of the program (which may not be shown in the example).

When two operands are present in an arithmetic or logical instruction, the right operand is the source and the left operand is the destination.

For example:

LOADREG: MOV EAX, SUBTOTAL

In this example, LOADREG is a label, MOV is the mnemonic identifier of an opcode, EAX is the destination operand, and SUBTOTAL is the source operand. Some assembly languages put the source and destination in reverse order.

1.3.4 Hexadecimal and Binary Numbers

Base 16 (hexadecimal) numbers are represented by a string of hexadecimal digits followed by the character H (for example, F82EH). A hexadecimal digit is a character from the following set: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F.

Base 2 (binary) numbers are represented by a string of 1s and 0s, sometimes followed by the character B (for example, 1010B). The "B" designation is only used in situations where confusion as to the type of number might arise.

1.3.5 Segmented Addressing

The processor uses byte addressing. This means memory is organized and accessed as a sequence of bytes. Whether one or more bytes are being accessed, a byte address is used to locate the byte or bytes in memory. The range of memory that can be addressed is called an address space.

The processor also supports segmented addressing. This is a form of addressing where a program may have many independent address spaces, called segments.
For example, a program can keep its code (instructions) and stack in separate segments. Code addresses would always refer to the code space, and stack addresses would always refer to the stack space. The following notation is used to specify a byte address within a segment:

Segment-register:Byte-address

For example, the following segment address identifies the byte at address FF79H in the segment pointed by the DS register:

DS:FF79H

The following segment address identifies an instruction address in the code segment. The CS register points to the code segment and the EIP register contains the address of the instruction.

CS:EIP

1.3.6 Exceptions

An exception is an event that typically occurs when an instruction causes an error. For example, an attempt to divide by zero generates an exception. However, some exceptions, such as breakpoints, occur under other conditions. Some types of exceptions may provide error codes. An error code reports additional information about the error. An example of the notation used to show an exception and error code is shown below:

#PF(fault code)

This example refers to a page-fault exception under conditions where an error code naming a type of fault is reported. Under some conditions, exceptions which produce error codes may not be able to report an accurate code. In this case, the error code is zero, as shown below for a general-protection exception:

#GP(0)

1.3.7 A New Syntax for CPUID, CR, and MSR Values

Obtain feature flags, status, and system information by using the CPUID instruction, by checking control register bits, and by reading model-specific registers. We are moving toward a new syntax to represent this information. See Figure 1-2.
### Related Literature

Literature related to Intel 64 and IA-32 processors is listed on-line at:

Some of the documents listed at this web site can be viewed on-line; others can be ordered. The literature available is listed by Intel processor and then by the following literature types: applications notes, data sheets, manuals, papers, and specification updates.

See also:

- The data sheet for a particular Intel 64 or IA-32 processor
- The specification update for a particular Intel 64 or IA-32 processor
- Intel 64 Architecture Processor Topology Enumeration: http://softwarecommunity.intel.com/articles/eng/3887.htm
- Developing Multi-threaded Applications: A Platform Consistent Approach: http://cache-www.intel.com/cd/00/00/05/15/51534_developing_multithreaded_applications.pdf
ABOUT THIS MANUAL

• Performance Monitoring Unit Sharing Guide
  http://software.intel.com/file/30388

More relevant links are:
• Software network link:
  http://softwarecommunity.intel.com/isn/home/
• Developer centers:
• Processor support general link:
  http://www.intel.com/support/processors/
• Software products and packages:
• Intel 64 and IA-32 processor manuals (printed or PDF downloads):
• Intel® Multi-Core Technology:
  http://software.intel.com/partner/multicore
• Intel® Hyper-Threading Technology (Intel® HT Technology):
This chapter describes the instruction format for all Intel 64 and IA-32 processors. The instruction format for protected mode, real-address mode and virtual-8086 mode is described in Section 2.1. Increments provided for IA-32e mode and its sub-modes are described in Section 2.2.

2.1 INSTRUCTION FORMAT FOR PROTECTED MODE, REAL-ADDRESS MODE, AND VIRTUAL-8086 MODE

The Intel 64 and IA-32 architectures instruction encodings are subsets of the format shown in Figure 2-1. Instructions consist of optional instruction prefixes (in any order), primary opcode bytes (up to three bytes), an addressing-form specifier (if required) consisting of the ModR/M byte and sometimes the SIB (Scale-Index-Base) byte, a displacement (if required), and an immediate data field (if required).

2.1.1 Instruction Prefixes

Instruction prefixes are divided into four groups, each with a set of allowable prefix codes. For each instruction, it is only useful to include up to one prefix code from each of the four groups (Groups 1, 2, 3, 4). Groups 1 through 4 may be placed in any order relative to each other.

- Group 1
  - Lock and repeat prefixes:
INSTRUCTION FORMAT

- LOCK prefix is encoded using F0H
- REPNE/REPNZ prefix is encoded using F2H. Repeat-Not-Zero prefix applies only to string and input/output instructions. (F2H is also used as a mandatory prefix for some instructions)
- REP or REPE/REPZ is encoded using F3H. Repeat prefix applies only to string and input/output instructions. (F3H is also used as a mandatory prefix for some instructions)

- Group 2
  - Segment override prefixes:
    - 2EH—CS segment override (use with any branch instruction is reserved)
    - 36H—SS segment override prefix (use with any branch instruction is reserved)
    - 3EH—DS segment override prefix (use with any branch instruction is reserved)
    - 26H—ES segment override prefix (use with any branch instruction is reserved)
    - 64H—FS segment override prefix (use with any branch instruction is reserved)
    - 65H—GS segment override prefix (use with any branch instruction is reserved)
  - Branch hints:
    - 2EH—Branch not taken (used only with Jcc instructions)
    - 3EH—Branch taken (used only with Jcc instructions)

- Group 3
  - Operand-size override prefix is encoded using 66H (66H is also used as a mandatory prefix for some instructions).

- Group 4
  - 67H—Address-size override prefix

The LOCK prefix (F0H) forces an operation that ensures exclusive use of shared memory in a multiprocessor environment. See "LOCK—Assert LOCK# Signal Prefix" in Chapter 3, "Instruction Set Reference, A-L," for a description of this prefix.

Repeat prefixes (F2H, F3H) cause an instruction to be repeated for each element of a string. Use these prefixes only with string and I/O instructions (MOVS, CMPS, SCAS, LODS, STOS, INS, and OUTS). Use of repeat prefixes and/or undefined opcodes with other Intel 64 or IA-32 instructions is reserved; such use may cause unpredictable behavior.

Some instructions may use F2H, F3H as a mandatory prefix to express distinct functionality. A mandatory prefix generally should be placed after other optional prefixes (exception to this is discussed in Section 2.2.1, "REX Prefixes")
Branch hint prefixes (2EH, 3EH) allow a program to give a hint to the processor about the most likely code path for a branch. Use these prefixes only with conditional branch instructions (Jcc). Other use of branch hint prefixes and/or other undefined opcodes with Intel 64 or IA-32 instructions is reserved; such use may cause unpredictable behavior.

The operand-size override prefix allows a program to switch between 16- and 32-bit operand sizes. Either size can be the default; use of the prefix selects the non-default size.

Some SSE2/SSE3/SSSE3/SSE4 instructions and instructions using a three-byte sequence of primary opcode bytes may use 66H as a mandatory prefix to express distinct functionality. A mandatory prefix generally should be placed after other optional prefixes (exception to this is discussed in Section 2.2.1, “REX Prefixes”).

Other use of the 66H prefix is reserved; such use may cause unpredictable behavior.

The address-size override prefix (67H) allows programs to switch between 16- and 32-bit addressing. Either size can be the default; the prefix selects the non-default size. Using this prefix and/or other undefined opcodes when operands for the instruction do not reside in memory is reserved; such use may cause unpredictable behavior.

### 2.1.2 Opcodes

A primary opcode can be 1, 2, or 3 bytes in length. An additional 3-bit opcode field is sometimes encoded in the ModR/M byte. Smaller fields can be defined within the primary opcode. Such fields define the direction of operation, size of displacements, register encoding, condition codes, or sign extension. Encoding fields used by an opcode vary depending on the class of operation.

Two-byte opcode formats for general-purpose and SIMD instructions consist of:

- An escape opcode byte 0FH as the primary opcode and a second opcode byte, or
- A mandatory prefix (66H, F2H, or F3H), an escape opcode byte, and a second opcode byte (same as previous bullet)

For example, CVTDQ2PD consists of the following sequence: F3 0F E6. The first byte is a mandatory prefix (it is not considered as a repeat prefix).

Three-byte opcode formats for general-purpose and SIMD instructions consist of:

- An escape opcode byte 0FH as the primary opcode, plus two additional opcode bytes, or
- A mandatory prefix (66H, F2H, or F3H), an escape opcode byte, plus two additional opcode bytes (same as previous bullet)

For example, PHADDW for XMM registers consists of the following sequence: 66 0F 38 01. The first byte is the mandatory prefix.

Valid opcode expressions are defined in Appendix A and Appendix B.
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2.1.3 ModR/M and SIB Bytes

Many instructions that refer to an operand in memory have an addressing-form specifier byte (called the ModR/M byte) following the primary opcode. The ModR/M byte contains three fields of information:

- The mod field combines with the r/m field to form 32 possible values: eight registers and 24 addressing modes.
- The reg/opcode field specifies either a register number or three more bits of opcode information. The purpose of the reg/opcode field is specified in the primary opcode.
- The r/m field can specify a register as an operand or it can be combined with the mod field to encode an addressing mode. Sometimes, certain combinations of the mod field and the r/m field is used to express opcode information for some instructions.

Certain encodings of the ModR/M byte require a second addressing byte (the SIB byte). The base-plus-index and scale-plus-index forms of 32-bit addressing require the SIB byte. The SIB byte includes the following fields:

- The scale field specifies the scale factor.
- The index field specifies the register number of the index register.
- The base field specifies the register number of the base register.

See Section 2.1.5 for the encodings of the ModR/M and SIB bytes.

2.1.4 Displacement and Immediate Bytes

Some addressing forms include a displacement immediately following the ModR/M byte (or the SIB byte if one is present). If a displacement is required; it be 1, 2, or 4 bytes.

If an instruction specifies an immediate operand, the operand always follows any displacement bytes. An immediate operand can be 1, 2 or 4 bytes.

2.1.5 Addressing-Mode Encoding of ModR/M and SIB Bytes

The values and corresponding addressing forms of the ModR/M and SIB bytes are shown in Table 2-1 through Table 2-3: 16-bit addressing forms specified by the ModR/M byte are in Table 2-1 and 32-bit addressing forms are in Table 2-2. Table 2-3 shows 32-bit addressing forms specified by the SIB byte. In cases where the reg/opcode field in the ModR/M byte represents an extended opcode, valid encodings are shown in Appendix B.

In Table 2-1 and Table 2-2, the Effective Address column lists 32 effective addresses that can be assigned to the first operand of an instruction by using the Mod and R/M fields of the ModR/M byte. The first 24 options provide ways of specifying a memory...
location; the last eight (Mod = 11B) provide ways of specifying general-purpose, MMX technology and XMM registers.

The Mod and R/M columns in Table 2-1 and Table 2-2 give the binary encodings of the Mod and R/M fields required to obtain the effective address listed in the first column. For example: see the row indicated by Mod = 11B, R/M = 000B. The row identifies the general-purpose registers EAX, AX or AL; MMX technology register MM0; or XMM register XMM0. The register used is determined by the opcode byte and the operand-size attribute.

Now look at the seventh row in either table (labeled “REG =”). This row specifies the use of the 3-bit Reg/Opcode field when the field is used to give the location of a second operand. The second operand must be a general-purpose, MMX technology, or XMM register. Rows one through five list the registers that may correspond to the value in the table. Again, the register used is determined by the opcode byte along with the operand-size attribute.

If the instruction does not require a second operand, then the Reg/Opcode field may be used as an opcode extension. This use is represented by the sixth row in the tables (labeled “/digit (Opcode)”). Note that values in row six are represented in decimal form.

The body of Table 2-1 and Table 2-2 (under the label “Value of ModR/M Byte (in Hexadecimal)”) contains a 32 by 8 array that presents all of 256 values of the ModR/M byte (in hexadecimal). Bits 3, 4 and 5 are specified by the column of the table in which a byte resides. The row specifies bits 0, 1 and 2; and bits 6 and 7. The figure below demonstrates interpretation of one table value.

<table>
<thead>
<tr>
<th>Mod</th>
<th>RM</th>
<th>REG</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>000</td>
<td>001</td>
</tr>
<tr>
<td>C8H</td>
<td>11001000</td>
<td></td>
</tr>
</tbody>
</table>

Figure 2-2. Table Interpretation of ModR/M Byte (C8H)
### Table 2-1. 16-Bit Addressing Forms with the ModR/M Byte

<table>
<thead>
<tr>
<th>Effective Address</th>
<th>Mod R/M</th>
<th>Value of ModR/M Byte (in Hexadecimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[BX+S]</td>
<td>00</td>
<td>00 08 10 18 20 28 30 38</td>
</tr>
<tr>
<td>[BX+D]</td>
<td>00</td>
<td>00 01 09 11 19 21 29 31</td>
</tr>
<tr>
<td>[BP+S]</td>
<td>01</td>
<td>01 02 0A 12 1A 22 2A 32</td>
</tr>
<tr>
<td>[BP+D]</td>
<td>01</td>
<td>01 03 0B 13 1B 23 2B 3B</td>
</tr>
<tr>
<td>[SI]</td>
<td>10</td>
<td>04 0C 14 1C 24 2C 34 3C</td>
</tr>
<tr>
<td>[DI]</td>
<td>10</td>
<td>05 0D 15 1D 25 2D 35 3D</td>
</tr>
<tr>
<td>disp16²</td>
<td>10</td>
<td>06 0E 16 1F 26 2E 36 3F</td>
</tr>
<tr>
<td>[BX]</td>
<td>11</td>
<td>07 0F 17 1F 27 2F 37 3F</td>
</tr>
<tr>
<td>[BX+S]+disp8³</td>
<td>01</td>
<td>00 40 48 50 58 60 68 70</td>
</tr>
<tr>
<td>[BX+D]+disp8</td>
<td>01</td>
<td>01 41 49 51 59 61 69 71</td>
</tr>
<tr>
<td>[BP+S]+disp8</td>
<td>00</td>
<td>02 0A 12 1A 22 2A 32 3A</td>
</tr>
<tr>
<td>[BP+D]+disp8</td>
<td>01</td>
<td>03 0B 13 1B 23 2B 33 3B</td>
</tr>
<tr>
<td>[SI]+disp8</td>
<td>10</td>
<td>04 0C 14 1C 24 2C 34 3C</td>
</tr>
<tr>
<td>[DI]+disp8</td>
<td>10</td>
<td>05 0D 15 1D 25 2D 35 3D</td>
</tr>
<tr>
<td>[BP]+disp8</td>
<td>11</td>
<td>06 0E 16 1F 26 2E 36 3F</td>
</tr>
<tr>
<td>[BX]+disp8</td>
<td>11</td>
<td>07 0F 17 1F 27 2F 37 3F</td>
</tr>
<tr>
<td>[BX+S]+disp16</td>
<td>10</td>
<td>00 80 88 90 98 90 98 90</td>
</tr>
<tr>
<td>[BX+D]+disp16</td>
<td>10</td>
<td>01 81 89 91 99 99 99 99</td>
</tr>
<tr>
<td>[BP+S]+disp16</td>
<td>01</td>
<td>02 82 8A 9A 9A 9A 9A 9A</td>
</tr>
<tr>
<td>[BP+D]+disp16</td>
<td>01</td>
<td>03 83 8B 9B 9B 9B 9B 9B</td>
</tr>
<tr>
<td>[SI]+disp16</td>
<td>10</td>
<td>04 8C 94 9C 94 9C 94 9C</td>
</tr>
<tr>
<td>[DI]+disp16</td>
<td>10</td>
<td>05 8D 95 9D 95 9D 95 9D</td>
</tr>
<tr>
<td>[BP]+disp16</td>
<td>11</td>
<td>06 8E 96 9E 96 9E 96 9E</td>
</tr>
<tr>
<td>[BX]+disp16</td>
<td>11</td>
<td>07 8F 97 9F 97 9F 97 9F</td>
</tr>
</tbody>
</table>

#### NOTES:

1. The default segment register is SS for the effective addresses containing a BP index, DS for other effective addresses.
2. The disp16 nomenclature denotes a 16-bit displacement that follows the ModR/M byte and that is added to the index.
3. The disp8 nomenclature denotes an 8-bit displacement that follows the ModR/M byte and that is sign-extended and added to the index.
The disp8 nomenclature denotes an 8-bit displacement that follows the ModR/M byte (or the SIB byte if one is present) and that is sign-extended and added to the index.

1. The disp32 nomenclature denotes a 32-bit displacement that follows the ModR/M byte (or the SIB byte if one is present) and that is added to the index.

2. The disp8 nomenclature denotes an 8-bit displacement that follows the ModR/M byte (or the SIB byte if one is present) and that is added to the index.

Table 2-3 is organized to give 256 possible values of the SIB byte (in hexadecimal). General purpose registers used as a base are indicated across the top of the table, along with corresponding values for the SIB byte's base field. Table rows in the body
INSTRUCTION FORMAT

of the table indicate the register used as the index (SIB byte bits 3, 4 and 5) and the scaling factor (determined by SIB byte bits 6 and 7).

Table 2-3. 32-Bit Addressing Forms with the SIB Byte

<table>
<thead>
<tr>
<th>Scaled Index</th>
<th>SS</th>
<th>Index</th>
<th>Value of SIB Byte (in Hexadecimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[EAX]</td>
<td>00</td>
<td>00</td>
<td>01 02 03 04 05 06 07</td>
</tr>
<tr>
<td>[ECX]</td>
<td>01</td>
<td>08</td>
<td>09 0A 0B 0C 0D 0E 0F</td>
</tr>
<tr>
<td>[EDX]</td>
<td>01</td>
<td>10</td>
<td>11 12 13 14 15 16 17</td>
</tr>
<tr>
<td>[EBX]</td>
<td>01</td>
<td>11</td>
<td>18 19 1A 1B 1C 1D 1E 1F</td>
</tr>
<tr>
<td>none</td>
<td>00</td>
<td>100</td>
<td>20 21 22 23 24 25 26 27</td>
</tr>
<tr>
<td>[EBP]</td>
<td>01</td>
<td>101</td>
<td>28 29 2A 2B 2C 2D 2E 2F</td>
</tr>
<tr>
<td>[ESI]</td>
<td>01</td>
<td>110</td>
<td>30 31 32 33 34 35 36 37</td>
</tr>
<tr>
<td>[EDI]</td>
<td>01</td>
<td>111</td>
<td>38 39 3A 3B 3C 3D 3E 3F</td>
</tr>
</tbody>
</table>

| [EAX*2]      | 01 | 000   | 40 41 42 43 44 45 46 47          |
| [ECX*2]      | 01 | 001   | 48 49 4A 4B 4C 4D 4E 4F          |
| [EDX*2]      | 01 | 010   | 50 51 52 53 54 55 56 57          |
| [EBX*2]      | 01 | 011   | 58 59 5A 5B 5C 5D 5E 5F          |
| none         | 01 | 100   | 60 61 62 63 64 65 66 67          |
| [EBP*2]      | 01 | 101   | 68 69 6A 6B 6C 6D 6E 6F          |
| [ESI*2]      | 01 | 110   | 70 71 72 73 74 75 76 77          |
| [EDI*2]      | 01 | 111   | 78 79 7A 7B 7C 7D 7E 7F          |

| [EAX*4]      | 10 | 000   | 80 81 82 83 84 85 86 87          |
| [ECX*4]      | 10 | 001   | 88 89 8A 8B 8C 8D 8E 8F          |
| [EDX*4]      | 10 | 010   | 90 91 92 93 94 95 96 97          |
| none         | 10 | 100   | A0 A1 A2 A3 A4 A5 A6 A7          |
| [EBP*4]      | 10 | 101   | A8 A9 AA AB AC AD AE AF          |
| [ESI*4]      | 10 | 110   | B0 B1 B2 B3 B4 B5 B6 B7          |
| [EDI*4]      | 10 | 111   | B8 B9 BA BB BC BD BE BF          |

| [EAX*8]      | 11 | 000   | C0 C1 C2 C3 C4 C5 C6 C7          |
| [ECX*8]      | 11 | 001   | C8 C9 CA CB CC CD CE CF          |
| [EDX*8]      | 11 | 010   | D0 D1 D2 D3 D4 D5 D6 D7          |
| [EBX*8]      | 11 | 011   | D8 DA DB DC DD DE DF            |
| none         | 11 | 100   | E0 E1 E2 E3 E4 E5 E6 E7          |
| [EBP*8]      | 11 | 101   | E8 EA EB EC ED EE EF            |
| [ESI*8]      | 11 | 110   | F0 F1 F2 F3 F4 F5 F6 F7          |
| [EDI*8]      | 11 | 111   | F8 FA FB FC FD FE FF            |

NOTES:
1. The [*] nomenclature means a disp32 with no base if the MOD is 00B. Otherwise, [*] means disp8 or disp32 + [EBP]. This provides the following address modes:

<table>
<thead>
<tr>
<th>MOD bits</th>
<th>Effective Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>[scaled index] + disp32</td>
</tr>
<tr>
<td>01</td>
<td>[scaled index] + disp8 + [EBP]</td>
</tr>
<tr>
<td>10</td>
<td>[scaled index] + disp32 + [EBP]</td>
</tr>
</tbody>
</table>
2.2 IA-32E MODE

IA-32e mode has two sub-modes. These are:

- **Compatibility Mode**. Enables a 64-bit operating system to run most legacy protected mode software unmodified.
- **64-Bit Mode**. Enables a 64-bit operating system to run applications written to access 64-bit address space.

2.2.1 REX Prefixes

REX prefixes are instruction-prefix bytes used in 64-bit mode. They do the following:

- Specify GPRs and SSE registers.
- Specify 64-bit operand size.
- Specify extended control registers.

Not all instructions require a REX prefix in 64-bit mode. A prefix is necessary only if an instruction references one of the extended registers or uses a 64-bit operand. If a REX prefix is used when it has no meaning, it is ignored.

Only one REX prefix is allowed per instruction. If used, the REX prefix byte must immediately precede the opcode byte or the escape opcode byte (0FH). When a REX prefix is used in conjunction with an instruction containing a mandatory prefix, the mandatory prefix must come before the REX so the REX prefix can be immediately preceding the opcode or the escape byte. For example, CVTDQ2PD with a REX prefix should have REX placed between F3 and 0F E6. Other placements are ignored. The instruction-size limit of 15 bytes still applies to instructions with a REX prefix. See Figure 2-3.

<table>
<thead>
<tr>
<th>Legacy Prefixes</th>
<th>REX Prefix</th>
<th>Opcode</th>
<th>ModR/M</th>
<th>SIB</th>
<th>Displacement</th>
<th>Immediate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grp 1, Grp 2, Grp 3, Grp 4 (optional)</td>
<td>(optional)</td>
<td>1-, 2-, or 3-byte opcode</td>
<td>1 byte (if required)</td>
<td>1 byte (if required)</td>
<td>Address displacement of 1, 2, or 4 bytes</td>
<td>Immediate data of 1, 2, or 4 bytes or none</td>
</tr>
</tbody>
</table>

Figure 2-3. Prefix Ordering in 64-bit Mode
2.2.1.1 Encoding

Intel 64 and IA-32 instruction formats specify up to three registers by using 3-bit fields in the encoding, depending on the format:

- ModR/M: the reg and r/m fields of the ModR/M byte
- ModR/M with SIB: the reg field of the ModR/M byte, the base and index fields of the SIB (scale, index, base) byte
- Instructions without ModR/M: the reg field of the opcode

In 64-bit mode, these formats do not change. Bits needed to define fields in the 64-bit context are provided by the addition of REX prefixes.

2.2.1.2 More on REX Prefix Fields

REX prefixes are a set of 16 opcodes that span one row of the opcode map and occupy entries 40H to 4FH. These opcodes represent valid instructions (INC or DEC) in IA-32 operating modes and in compatibility mode. In 64-bit mode, the same opcodes represent the instruction prefix REX and are not treated as individual instructions.

The single-byte-opcode form of INC/DEC instruction not available in 64-bit mode. INC/DEC functionality is still available using ModR/M forms of the same instructions (opcodes FF/0 and FF/1).

See Table 2-4 for a summary of the REX prefix format. Figure 2-4 though Figure 2-7 show examples of REX prefix fields in use. Some combinations of REX prefix fields are invalid. In such cases, the prefix is ignored. Some additional information follows:

- Setting REX.W can be used to determine the operand size but does not solely determine operand width. Like the 66H size prefix, 64-bit operand size override has no effect on byte-specific operations.
- For non-byte operations: if a 66H prefix is used with prefix (REX.W = 1), 66H is ignored.
- If a 66H override is used with REX and REX.W = 0, the operand size is 16 bits.
- REX.R modifies the ModR/M reg field when that field encodes a GPR, SSE, control or debug register. REX.R is ignored when ModR/M specifies other registers or defines an extended opcode.
- REX.X bit modifies the SIB index field.
- REX.B either modifies the base in the ModR/M r/m field or SIB base field; or it modifies the opcode reg field used for accessing GPRs.
Table 2-4. REX Prefix Fields [BITS: 0100WRXB]

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bit Position</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>7:4</td>
<td>0100</td>
</tr>
</tbody>
</table>
| W          | 3            | 0 = Operand size determined by CS.D  
1 = 64 Bit Operand Size |
| R          | 2            | Extension of the ModR/M reg field |
| X          | 1            | Extension of the SIB index field |
| B          | 0            | Extension of the ModR/M r/m field, SIB base field, or Opcode reg field |

Figure 2-4. Memory Addressing Without an SIB Byte; REX.X Not Used

Figure 2-5. Register-Register Addressing (No Memory Operand); REX.X Not Used
In the IA-32 architecture, byte registers (AH, AL, BH, BL, CH, CL, DH, and DL) are encoded in the ModR/M byte's reg field, the r/m field or the opcode reg field as registers 0 through 7. REX prefixes provide an additional addressing capability for byte-registers that makes the least-significant byte of GPRs available for byte operations. Certain combinations of the fields of the ModR/M byte and the SIB byte have special meaning for register encodings. For some combinations, fields expanded by the REX prefix are not decoded. Table 2-5 describes how each case behaves.
### 2.2.1.3 Displacement

Addressing in 64-bit mode uses existing 32-bit ModR/M and SIB encodings. The ModR/M and SIB displacement sizes do not change. They remain 8 bits or 32 bits and are sign-extended to 64 bits.

### 2.2.1.4 Direct Memory-Offset MOVs

In 64-bit mode, direct memory-offset forms of the MOV instruction are extended to specify a 64-bit immediate absolute address. This address is called a moffset. No prefix is needed to specify this 64-bit memory offset. For these MOV instructions, the

---

**Table 2-5. Special Cases of REX Encodings**

<table>
<thead>
<tr>
<th>ModR/M or SIB</th>
<th>Sub-field Encodings</th>
<th>Compatibility Mode Operation</th>
<th>Compatibility Mode Implications</th>
<th>Additional Implications</th>
</tr>
</thead>
<tbody>
<tr>
<td>ModR/M Byte</td>
<td>mod != 11</td>
<td>SIB byte present.</td>
<td>SIB byte required for ESP-based addressing.</td>
<td>REX prefix adds a fourth bit (b) which is not decoded (don’t care). SIB byte also required for R12-based addressing.</td>
</tr>
<tr>
<td></td>
<td>r/m = b*100(ESP)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ModR/M Byte</td>
<td>mod = 0</td>
<td>Base register not used.</td>
<td>EBP without a displacement must be done using mod = 01 with displacement of 0.</td>
<td>REX prefix adds a fourth bit (b) which is not decoded (don’t care). Using RBP or R13 without displacement must be done using mod = 01 with a displacement of 0.</td>
</tr>
<tr>
<td></td>
<td>r/m = b*101(EBP)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SIB Byte</td>
<td>index = 0100(ESP)</td>
<td>Index register not used.</td>
<td>ESP cannot be used as an index register.</td>
<td>REX prefix adds a fourth bit (b) which is decoded. There are no additional implications. The expanded index field allows distinguishing RSP from R12, therefore R12 can be used as an index.</td>
</tr>
<tr>
<td>SIB Byte</td>
<td>base = 0101(EBP)</td>
<td>Base register is unused if mod = 0.</td>
<td>Base register depends on mod encoding.</td>
<td>REX prefix adds a fourth bit (b) which is not decoded. This requires explicit displacement to be used with EBP/RBP or R13.</td>
</tr>
</tbody>
</table>

**NOTES:**

* Don’t care about value of REX.B
size of the memory offset follows the address-size default (64 bits in 64-bit mode). See Table 2-6.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>MOV AL, moffset</td>
</tr>
<tr>
<td>A1</td>
<td>MOV EAX, moffset</td>
</tr>
<tr>
<td>A2</td>
<td>MOV moffset, AL</td>
</tr>
<tr>
<td>A3</td>
<td>MOV moffset, EAX</td>
</tr>
</tbody>
</table>

2.2.1.5  Immediates

In 64-bit mode, the typical size of immediate operands remains 32 bits. When the operand size is 64 bits, the processor sign-extends all immediates to 64 bits prior to their use.

Support for 64-bit immediate operands is accomplished by expanding the semantics of the existing move (MOV reg, imm16/32) instructions. These instructions (opcodes B8H – BFH) move 16-bits or 32-bits of immediate data (depending on the effective operand size) into a GPR. When the effective operand size is 64 bits, these instructions can be used to load an immediate into a GPR. A REX prefix is needed to override the 32-bit default operand size to a 64-bit operand size.

For example:

48 B8 8877665544332211 MOV RAX,1122334455667788H

2.2.1.6  RIP-Relative Addressing

A new addressing form, RIP-relative (relative instruction-pointer) addressing, is implemented in 64-bit mode. An effective address is formed by adding displacement to the 64-bit RIP of the next instruction.

In IA-32 architecture and compatibility mode, addressing relative to the instruction pointer is available only with control-transfer instructions. In 64-bit mode, instructions that use ModR/M addressing can use RIP-relative addressing. Without RIP-relative addressing, all ModR/M instruction modes address memory relative to zero.

RIP-relative addressing allows specific ModR/M modes to address memory relative to the 64-bit RIP using a signed 32-bit displacement. This provides an offset range of ±2GB from the RIP. Table 2-7 shows the ModR/M and SIB encodings for RIP-relative addressing. Redundant forms of 32-bit displacement-addressing exist in the current ModR/M and SIB encodings. There is one ModR/M encoding and there are several SIB encodings. RIP-relative addressing is encoded using a redundant form.

In 64-bit mode, the ModR/M Disp32 (32-bit displacement) encoding is re-defined to be RIP+Disp32 rather than displacement-only. See Table 2-7.
The ModR/M encoding for RIP-relative addressing does not depend on using prefix. Specifically, the r/m bit field encoding of 101B (used to select RIP-relative addressing) is not affected by the REX prefix. For example, selecting R13 (REX.B = 1, r/m = 101B) with mod = 00B still results in RIP-relative addressing. The 4-bit r/m field of REX.B combined with ModR/M is not fully decoded. In order to address R13 with no displacement, software must encode R13 + 0 using a 1-byte displacement of zero.

RIP-relative addressing is enabled by 64-bit mode, not by a 64-bit address-size. The use of the address-size prefix does not disable RIP-relative addressing. The effect of the address-size prefix is to truncate and zero-extend the computed effective address to 32 bits.

### 2.2.1.7 Default 64-Bit Operand Size

In 64-bit mode, two groups of instructions have a default operand size of 64 bits (do not need a REX prefix for this operand size). These are:

- Near branches
- All instructions, except far branches, that implicitly reference the RSP

### 2.2.2 Additional Encodings for Control and Debug Registers

In 64-bit mode, more encodings for control and debug registers are available. The REX.R bit is used to modify the ModR/M reg field when that field encodes a control or debug register (see Table 2-4). These encodings enable the processor to address CR8-CR15 and DR8-DR15. An additional control register (CR8) is defined in 64-bit mode. CR8 becomes the Task Priority Register (TPR).

In the first implementation of IA-32e mode, CR9-CR15 and DR8-DR15 are not implemented. Any attempt to access unimplemented registers results in an invalid-opcode exception (#UD).
2.3 INTEL® ADVANCED VECTOR EXTENSIONS (INTEL® AVX)

Intel AVX instructions are encoded using an encoding scheme that combines prefix bytes, opcode extension field, operand encoding fields, and vector length encoding capability into a new prefix, referred to as VEX. In the VEX encoding scheme, the VEX prefix may be two or three bytes long, depending on the instruction semantics. Despite the two-byte or three-byte length of the VEX prefix, the VEX encoding format provides a more compact representation/packing of the components of encoding an instruction in Intel 64 architecture. The VEX encoding scheme also allows more headroom for future growth of Intel 64 architecture.

2.3.1 Instruction Format

Instruction encoding using VEX prefix provides several advantages:

- Instruction syntax support for three operands and up-to four operands when necessary. For example, the third source register used by VBLENDVPD is encoded using bits 7:4 of the immediate byte.
- Encoding support for vector length of 128 bits (using XMM registers) and 256 bits (using YMM registers).
- Encoding support for instruction syntax of non-destructive source operands.
- Elimination of escape opcode byte (0FH), SIMD prefix byte (66H, F2H, F3H) via a compact bit field representation within the VEX prefix.
- Elimination of the need to use REX prefix to encode the extended half of general-purpose register sets (R8-R15) for direct register access, memory addressing, or accessing XMM8-XMM15 (including YMM8-YMM15).
- Flexible and more compact bit fields are provided in the VEX prefix to retain the full functionality provided by REX prefix. REX.W, REX.X, REX.B functionalities are provided in the three-byte VEX prefix only because only a subset of SIMD instructions need them.
- Extensibility for future instruction extensions without significant instruction length increase.

Figure 2-8 shows the Intel 64 instruction encoding format with VEX prefix support. Legacy instruction without a VEX prefix is fully supported and unchanged. The use of VEX prefix in an Intel 64 instruction is optional, but a VEX prefix is required for Intel 64 instructions that operate on YMM registers or support three and four operand syntax. VEX prefix is not a constant-valued, “single-purpose” byte like 0FH, 66H, F2H, F3H in legacy SSE instructions. VEX prefix provides substantially richer capability than the REX prefix.
2.3.2 VEX and the LOCK prefix
Any VEX-encoded instruction with a LOCK prefix preceding VEX will #UD.

2.3.3 VEX and the 66H, F2H, and F3H prefixes
Any VEX-encoded instruction with a 66H, F2H, or F3H prefix preceding VEX will #UD.

2.3.4 VEX and the REX prefix
Any VEX-encoded instruction with a REX prefix proceeding VEX will #UD.

2.3.5 The VEX Prefix
The VEX prefix is encoded in either the two-byte form (the first byte must be C5H) or in the three-byte form (the first byte must be C4H). The two-byte VEX is used mainly for 128-bit, scalar, and the most common 256-bit AVX instructions; while the three-byte VEX provides a compact replacement of REX and 3-byte opcode instructions (including AVX and FMA instructions). Beyond the first byte of the VEX prefix, it consists of a number of bit fields providing specific capability, they are shown in Figure 2-9.

The bit fields of the VEX prefix can be summarized by its functional purposes:

- Non-destructive source register encoding (applicable to three and four operand syntax): This is the first source operand in the instruction syntax. It is represented by the notation, VEX.vvvv. This field is encoded using 1's complement form (inverted form), i.e. XMM0/YMM0/R0 is encoded as 1111B, XMM15/YMM15/R15 is encoded as 0000B.

- Vector length encoding: This 1-bit field represented by the notation VEX.L. L= 0 means vector length is 128 bits wide, L=1 means 256 bit vector. The value of this field is written as VEX.128 or VEX.256 in this document to distinguish encoded values of other VEX bit fields.
INSTRUCTION FORMAT

• REX prefix functionality: Full REX prefix functionality is provided in the three-byte form of VEX prefix. However the VEX bit fields providing REX functionality are encoded using 1’s complement form, i.e. XMM0/YMM0/R0 is encoded as 1111B, XMM15/YMM15/R15 is encoded as 0000B.
  — Two-byte form of the VEX prefix only provides the equivalent functionality of REX.R, using 1’s complement encoding. This is represented as VEX.R.
  — Three-byte form of the VEX prefix provides REX.R, REX.X, REX.B functionality using 1’s complement encoding and three dedicated bit fields represented as VEX.R, VEX.X, VEX.B.
  — Three-byte form of the VEX prefix provides the functionality of REX.W only to specific instructions that need to override default 32-bit operand size for a general purpose register to 64-bit size in 64-bit mode. For those applicable instructions, VEX.W field provides the same functionality as REX.W. VEX.W field can provide completely different functionality for other instructions. Consequently, the use of REX prefix with VEX encoded instructions is not allowed. However, the intent of the REX prefix for expanding register set is reserved for future instruction set extensions using VEX prefix encoding format.

• Compaction of SIMD prefix: Legacy SSE instructions effectively use SIMD prefixes (66H, F2H, F3H) as an opcode extension field. VEX prefix encoding allows the functional capability of such legacy SSE instructions (operating on XMM registers, bits 255:128 of corresponding YMM unmodified) to be encoded using the VEX.pp field without the presence of any SIMD prefix. The VEX-encoded 128-bit instruction will zero-out bits 255:128 of the destination register. VEX-encoded instruction may have 128 bit vector length or 256 bits length.

• Compaction of two-byte and three-byte opcode: More recently introduced legacy SSE instructions employ two and three-byte opcode. The one or two leading bytes are: 0FH, and 0FH 3AH/0FH 38H. The one-byte escape (0FH) and two-byte escape (0FH 3AH, 0FH 38H) can also be interpreted as an opcode extension field. The VEX.mmmmm field provides compaction to allow many legacy instruction to be encoded without the constant byte sequence, 0FH, 0FH 3AH, 0FH 38H. These VEX-encoded instruction may have 128 bit vector length or 256 bits length.

The VEX prefix is required to be the last prefix and immediately precedes the opcode bytes. It must follow any other prefixes. If VEX prefix is present a REX prefix is not supported.

The 3-byte VEX leaves room for future expansion with 3 reserved bits. REX and the 66h/F2h/F3h prefixes are reclaimed for future use.

VEX prefix has a two-byte form and a three byte form. If an instruction syntax can be encoded using the two-byte form, it can also be encoded using the three byte form of VEX. The latter increases the length of the instruction by one byte. This may be helpful in some situations for code alignment.

The VEX prefix supports 256-bit versions of floating-point SSE, SSE2, SSE3, and SSE4 instructions. Note, certain new instruction functionality can only be encoded with the VEX prefix.
The VEX prefix will #UD on any instruction containing MMX register sources or destinations.

### Figure 2-9. VEX bitfields

- **R**: REX.R in 1’s complement (inverted) form
  - 1: Same as REX.R=0 (must be 1 in 32-bit mode)
  - 0: Same as REX.R=1 (64-bit mode only)
- **X**: REX.X in 1’s complement (inverted) form
  - 1: Same as REX.X=0 (must be 1 in 32-bit mode)
  - 0: Same as REX.X=1 (64-bit mode only)
- **B**: REX.B in 1’s complement (inverted) form
  - 1: Same as REX.B=0 (Ignored in 32-bit mode).
  - 0: Same as REX.B=1 (64-bit mode only)
- **W**: opcode specific (use like REX.W, or used for opcode extension, or ignored, depending on the opcode byte)
- **m-mmmm**: Reserved for future use (will #UD)
  - 00000: implied 0F leading opcode byte
  - 00001: implied 0F 38 leading opcode bytes
  - 00010: implied 0F 3A leading opcode bytes
  - 00011: implied 0F 3E leading opcode bytes
  - 00100-11111: Reserved for future use (will #UD)
- **vvvv**: a register specifier (in 1’s complement form) or 1111 if unused.
- **L**: Vector Length
  - 0: scalar or 128-bit vector
  - 1: 256-bit vector
- **pp**: opcode extension providing equivalent functionality of a SIMD prefix
  - 00: None
  - 01: 66
  - 10: F3
  - 11: F2
INSTRUCTION FORMAT

The following subsections describe the various fields in two or three-byte VEX prefix:

2.3.5.1 VEX Byte 0, bits[7:0]
VEX Byte 0, bits [7:0] must contain the value 11000101b (C5h) or 11000100b (C4h). The 3-byte VEX uses the C4h first byte, while the 2-byte VEX uses the C5h first byte.

2.3.5.2 VEX Byte 1, bit [7] - ‘R’
VEX Byte 1, bit [7] contains a bit analogous to a bit inverted REX.R. In protected and compatibility modes the bit must be set to ‘1’ otherwise the instruction is LES or LDS. This bit is present in both 2- and 3-byte VEX prefixes.
The usage of WRXB bits for legacy instructions is explained in detail section 2.2.1.2 of Intel 64 and IA-32 Architectures Software developer’s manual, Volume 2A.
This bit is stored in bit inverted format.

2.3.5.3 3-byte VEX byte 1, bit[6] - ‘X’
Bit[6] of the 3-byte VEX byte 1 encodes a bit analogous to a bit inverted REX.X. It is an extension of the SIB Index field in 64-bit modes. In 32-bit modes, this bit must be set to ‘1’ otherwise the instruction is LES or LDS.
This bit is available only in the 3-byte VEX prefix.
This bit is stored in bit inverted format.

2.3.5.4 3-byte VEX byte 1, bit[5] - ‘B’
Bit[5] of the 3-byte VEX byte 1 encodes a bit analogous to a bit inverted REX.B. In 64-bit modes, it is an extension of the ModR/M r/m field, or the SIB base field. In 32-bit modes, this bit is ignored.
This bit is available only in the 3-byte VEX prefix.
This bit is stored in bit inverted format.

2.3.5.5 3-byte VEX byte 2, bit[7] - ‘W’
Bit[7] of the 3-byte VEX byte 2 is represented by the notation VEX.W. It can provide following functions, depending on the specific opcode.
- For AVX instructions that have equivalent legacy SSE instructions (typically these SSE instructions have a general-purpose register operand with its operand size attribute promotable by REX.W), if REX.W promotes the operand size attribute of the general-purpose register operand in legacy SSE instruction, VEX.W has same meaning in the corresponding AVX equivalent form. In 32-bit modes, VEX.W is silently ignored.
INSTRUCTION FORMAT

- For AVX instructions that have equivalent legacy SSE instructions (typically these SSE instructions have operands with their operand size attribute fixed and not promotable by REX.W), if REX.W is don’t care in legacy SSE instruction, VEX.W is ignored in the corresponding AVX equivalent form irrespective of mode.

- For new AVX instructions where VEX.W has no defined function (typically these meant the combination of the opcode byte and VEX.mmmmm did not have any equivalent SSE functions), VEX.W is reserved as zero and setting to other than zero will cause instruction to #UD.

2.3.5.6 2-byte VEX Byte 1, bits[6:3] and 3-byte VEX Byte 2, bits [6:3] - ‘vvvv’ the Source or dest Register Specifier

In 32-bit mode the VEX first byte C4 and C5 alias onto the LES and LDS instructions. To maintain compatibility with existing programs the VEX 2nd byte, bits [7:6] must be 11b. To achieve this, the VEX payload bits are selected to place only inverted, 64-bit valid fields (extended register selectors) in these upper bits.

The 2-byte VEX Byte 1, bits [6:3] and the 3-byte VEX, Byte 2, bits [6:3] encode a field (shorthand VEX.vvvv) that for instructions with 2 or more source registers and an XMM or YMM or memory destination encodes the first source register specifier stored in inverted (1’s complement) form.

VEX.vvvv is not used by the instructions with one source (except certain shifts, see below) or on instructions with no XMM or YMM or memory destination. If an instruction does not use VEX.vvvv then it should be set to 1111b otherwise instruction will #UD.

In 64-bit mode all 4 bits may be used. See Table 2-8 for the encoding of the XMM or YMM registers. In 32-bit and 16-bit modes bit 6 must be 1 (if bit 6 is not 1, the 2-byte VEX version will generate LDS instruction and the 3-byte VEX version will ignore this bit).
INSTRUCTION FORMAT

Table 2-8. VEX.vvvv to register name mapping

<table>
<thead>
<tr>
<th>VEX.vvvv</th>
<th>Dest Register</th>
<th>Valid in Legacy/Compatibility 32-bit modes?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111B</td>
<td>XMM0/YMM0</td>
<td>Valid</td>
</tr>
<tr>
<td>1110B</td>
<td>XMM1/YMM1</td>
<td>Valid</td>
</tr>
<tr>
<td>1101B</td>
<td>XMM2/YMM2</td>
<td>Valid</td>
</tr>
<tr>
<td>1100B</td>
<td>XMM3/YMM3</td>
<td>Valid</td>
</tr>
<tr>
<td>1011B</td>
<td>XMM4/YMM4</td>
<td>Valid</td>
</tr>
<tr>
<td>1010B</td>
<td>XMM5/YMM5</td>
<td>Valid</td>
</tr>
<tr>
<td>1001B</td>
<td>XMM6/YMM6</td>
<td>Valid</td>
</tr>
<tr>
<td>1000B</td>
<td>XMM7/YMM7</td>
<td>Valid</td>
</tr>
<tr>
<td>0111B</td>
<td>XMM8/YMM8</td>
<td>Invalid</td>
</tr>
<tr>
<td>0110B</td>
<td>XMM9/YMM9</td>
<td>Invalid</td>
</tr>
<tr>
<td>0101B</td>
<td>XMM10/YMM10</td>
<td>Invalid</td>
</tr>
<tr>
<td>0100B</td>
<td>XMM11/YMM11</td>
<td>Invalid</td>
</tr>
<tr>
<td>0011B</td>
<td>XMM12/YMM12</td>
<td>Invalid</td>
</tr>
<tr>
<td>0010B</td>
<td>XMM13/YMM13</td>
<td>Invalid</td>
</tr>
<tr>
<td>0001B</td>
<td>XMM14/YMM14</td>
<td>Invalid</td>
</tr>
<tr>
<td>0000B</td>
<td>XMM15/YMM15</td>
<td>Invalid</td>
</tr>
</tbody>
</table>

The VEX.vvvv field is encoded in bit inverted format for accessing a register operand.

2.3.6 Instruction Operand Encoding and VEX.vvvv, ModR/M

VEX-encoded instructions support three-operand and four-operand instruction syntax. Some VEX-encoded instructions have syntax with less than three operands, e.g. VEX-encoded pack shift instructions support one source operand and one destination operand).

The roles of VEX.vvvv, reg field of ModR/M byte (ModR/M.reg), r/m field of ModR/M byte (ModR/M.r/m) with respect to encoding destination and source operands vary with different type of instruction syntax.

The role of VEX.vvvv can be summarized to three situations:

- VEX.vvvv encodes the first source register operand, specified in inverted (1's complement) form and is valid for instructions with 2 or more source operands.
- VEX.vvvv encodes the destination register operand, specified in 1's complement form for certain vector shifts. The instructions where VEX.vvvv is used as a destination are listed in Table 2-9. The notation in the “Opcode” column in Table 2-9 is described in detail in section 3.1.1.
• VEX.vvvv does not encode any operand, the field is reserved and should contain 1111b.

Table 2-9. Instructions with a VEX.vvvv destination

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.NDD.128.66.0F 73 /7 ib</td>
<td>VPSLLDQ xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 73 /3 ib</td>
<td>VPSRLDQ xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 71 /2 ib</td>
<td>VPSRLW xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 72 /2 ib</td>
<td>VPSRLD xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 73 /2 ib</td>
<td>VPSRLQ xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 71 /4 ib</td>
<td>VPSRAW xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 72 /4 ib</td>
<td>VPSRAD xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 71 /6 ib</td>
<td>VPSLLW xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 72 /6 ib</td>
<td>VPSLLD xmm1, xmm2, imm8</td>
</tr>
<tr>
<td>VEX.NDD.128.66.0F 73 /6 ib</td>
<td>VPSLLQ xmm1, xmm2, imm8</td>
</tr>
</tbody>
</table>

The role of ModR/M.r/m field can be summarized to two situations:
• ModR/M.r/m encodes the instruction operand that references a memory address.
• For some instructions that do not support memory addressing semantics, ModR/M.r/m encodes either the destination register operand or a source register operand.

The role of ModR/M.reg field can be summarized to two situations:
• ModR/M.reg encodes either the destination register operand or a source register operand.
• For some instructions, ModR/M.reg is treated as an opcode extension and not used to encode any instruction operand.

For instruction syntax that support four operands, VEX.vvvv, ModR/M.r/m, ModR/M.reg encodes three of the four operands. The role of bits 7:4 of the immediate byte serves the following situation:
• Imm8[7:4] encodes the third source register operand.

2.3.6.1 3-byte VEX byte 1, bits[4:0] - “m-mmmm”

Bits[4:0] of the 3-byte VEX byte 1 encode an implied leading opcode byte (0F, 0F 38, or 0F 3A). Several bits are reserved for future use and will #UD unless 0.
INSTRUCTION FORMAT

Table 2-10. VEX.m-mmmm interpretation

<table>
<thead>
<tr>
<th>VEX.m-mmmm</th>
<th>Implied Leading Opcode Bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000B</td>
<td>Reserved</td>
</tr>
<tr>
<td>00001B</td>
<td>0F</td>
</tr>
<tr>
<td>00010B</td>
<td>0F 3B</td>
</tr>
<tr>
<td>00011B</td>
<td>0F 3A</td>
</tr>
<tr>
<td>00100-11111B</td>
<td>Reserved</td>
</tr>
<tr>
<td>(2-byte VEX)</td>
<td>0F</td>
</tr>
</tbody>
</table>

VEX.m-mmmm is only available on the 3-byte VEX. The 2-byte VEX implies a leading 0Fh opcode byte.

2.3.6.2  2-byte VEX byte 1, bit[2], and 3-byte VEX byte 2, bit [2]- “L”

The vector length field, VEX.L, is encoded in bit[2] of either the second byte of 2-byte VEX, or the third byte of 3-byte VEX. If “VEX.L = 1”, it indicates 256-bit vector operation. “VEX.L = 0” indicates scalar and 128-bit vector operations.

The instruction VZEROUPPER is a special case that is encoded with VEX.L = 0, although its operation zero’s bits 255:128 of all YMM registers accessible in the current operating mode.

See the following table.

Table 2-11. VEX.L interpretation

<table>
<thead>
<tr>
<th>VEX.L</th>
<th>Vector Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>128-bit (or 32/64-bit scalar)</td>
</tr>
<tr>
<td>1</td>
<td>256-bit</td>
</tr>
</tbody>
</table>

2.3.6.3  2-byte VEX byte 1, bits[1:0], and 3-byte VEX byte 2, bits [1:0]- “pp”

Up to one implied prefix is encoded by bits[1:0] of either the 2-byte VEX byte 1 or the 3-byte VEX byte 2. The prefix behaves as if it was encoded prior to VEX, but after all other encoded prefixes.

See the following table.
2.3.7 The Opcode Byte

One (and only one) opcode byte follows the 2 or 3 byte VEX. Legal opcodes are specified in Appendix B, in color. Any instruction that uses illegal opcode will #UD.

2.3.8 The MODRM, SIB, and Displacement Bytes

The encodings are unchanged but the interpretation of reg_field or rm_field differs (see above).

2.3.9 The Third Source Operand (Immediate Byte)

VEX-encoded instructions can support instruction with a four operand syntax. VBLENDVPD, VBLENDVPS, and PBLENDVB use imm8[7:4] to encode one of the source registers.

2.3.10 AVX Instructions and the Upper 128-bits of YMM registers

If an instruction with a destination XMM register is encoded with a VEX prefix, the processor zeroes the upper bits (above bit 128) of the equivalent YMM register. Legacy SSE instructions without VEX preserve the upper bits.

2.3.10.1 Vector Length Transition and Programming Considerations

An instruction encoded with a VEX.128 prefix that loads a YMM register operand operates as follows:

- Data is loaded into bits 127:0 of the register
- Bits above bit 127 in the register are cleared.

Thus, such an instruction clears bits 255:128 of a destination YMM register on processors with a maximum vector-register width of 256 bits. In the event that future processors extend the vector registers to greater widths, an instruction encoded with a VEX.128 or VEX.256 prefix will also clear any bits beyond bit 255.

---

<table>
<thead>
<tr>
<th>pp</th>
<th>Implies this prefix after other prefixes but before VEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>00B</td>
<td>None</td>
</tr>
<tr>
<td>01B</td>
<td>66</td>
</tr>
<tr>
<td>10B</td>
<td>F3</td>
</tr>
<tr>
<td>11B</td>
<td>F2</td>
</tr>
</tbody>
</table>
INSTRUCTION FORMAT

(This is in contrast with legacy SSE instructions, which have no VEX prefix; these modify only bits 127:0 of any destination register operand.) Programmers should bear in mind that instructions encoded with VEX.128 and VEX.256 prefixes will clear any future extensions to the vector registers. A calling function that uses such extensions should save their state before calling legacy functions. This is not possible for involuntary calls (e.g., into an interrupt-service routine). It is recommended that software handling involuntary calls accommodate this by not executing instructions encoded with VEX.128 and VEX.256 prefixes. In the event that it is not possible or desirable to restrict these instructions, then software must take special care to avoid actions that would, on future processors, zero the upper bits of vector registers.

Processors that support further vector-register extensions (defining bits beyond bit 255) will also extend the XSAVE and XRSTOR instructions to save and restore these extensions. To ensure forward compatibility, software that handles involuntary calls and that uses instructions encoded with VEX.128 and VEX.256 prefixes should first save and then restore the vector registers (with any extensions) using the XSAVE and XRSTOR instructions with save/restore masks that set bits that correspond to all vector-register extensions. Ideally, software should rely on a mechanism that is cognizant of which bits to set. (E.g., an OS mechanism that sets the save/restore mask bits for all vector-register extensions that are enabled in XCR0.) Saving and restoring state with instructions other than XSAVE and XRSTOR will, on future processors with wider vector registers, corrupt the extended state of the vector registers - even if doing so functions correctly on processors supporting 256-bit vector registers. (The same is true if XSAVE and XRSTOR are used with a save/restore mask that does not set bits corresponding to all supported extensions to the vector registers.)

2.3.11 AVX Instruction Length

The AVX instructions described in this document (including VEX and ignoring other prefixes) do not exceed 11 bytes in length, but may increase in the future. The maximum length of an Intel 64 and IA-32 instruction remains 15 bytes.

2.4 INSTRUCTION EXCEPTION SPECIFICATION

To look up the exceptions of legacy 128-bit SIMD instruction, 128-bit VEX-encoded instructions, and 256-bit VEX-encoded instruction, Table 2-13 summarizes the exception behavior into separate classes, with detailed exception conditions defined in sub-sections 2.4.1 through 2.4.8. For example, ADDPS contains the entry:

"See Exceptions Type 2"  
In this entry, "Type2" can be looked up in Table 2-13. The instruction’s corresponding CPUID feature flag can be identified in the fourth column of the Instruction summary table.
Note: #UD on CPUID feature flags=0 is not guaranteed in a virtualized environment if the hardware supports the feature flag.

NOTE

Instructions that operate only with MMX, X87, or general-purpose registers are not covered by the exception classes defined in this section. For instructions that operate on MMX registers, see Section 22.25.3, “Exception Conditions of Legacy SIMD Instructions Operating on MMX Registers” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B.

Table 2-13. Exception class description

<table>
<thead>
<tr>
<th>Exception Class</th>
<th>Instruction set</th>
<th>Mem arg</th>
<th>Floating-Point Exceptions (#XM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type 1</td>
<td>AVX, Legacy SSE</td>
<td>16/32 byte explicitly aligned</td>
<td>none</td>
</tr>
<tr>
<td>Type 2</td>
<td>AVX, Legacy SSE</td>
<td>16/32 byte not explicitly aligned</td>
<td>yes</td>
</tr>
<tr>
<td>Type 3</td>
<td>AVX, Legacy SSE</td>
<td>&lt; 16 byte</td>
<td>yes</td>
</tr>
<tr>
<td>Type 4</td>
<td>AVX, Legacy SSE</td>
<td>16/32 byte not explicitly aligned</td>
<td>no</td>
</tr>
<tr>
<td>Type 5</td>
<td>AVX, Legacy SSE</td>
<td>&lt; 16 byte</td>
<td>no</td>
</tr>
<tr>
<td>Type 6</td>
<td>AVX (no Legacy SSE)</td>
<td>Varies</td>
<td>(At present, none do)</td>
</tr>
<tr>
<td>Type 7</td>
<td>AVX, Legacy SSE</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>Type 8</td>
<td>AVX</td>
<td>none</td>
<td>none</td>
</tr>
</tbody>
</table>

See Table 2-14 for lists of instructions in each exception class.
## Table 2-14. Instructions in each Exception Class

<table>
<thead>
<tr>
<th>Exception Class</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type 1</strong></td>
<td>(V)MOVAPD, (V)MOVAPS, (V)MOVDQA, (V)MOVNTDQ, (V)MOVNTDQA, (V)MOVNTPD, (V)MOVNTPS</td>
</tr>
<tr>
<td><strong>Type 2</strong></td>
<td>(V)ADDPD, (V)ADDPS, (V)ADDSUBPD, (V)ADDSUBPS, (V)CMPFPD, (V)CMFPS, (V)CVTQ2PS, (V)CVTQ2PD, (V)CVTPD2Q, (V)CVTPD2PS, (V)CVTPS2Q, (V)CVTPS2PD, (V)DIVPD, (V)DIVPS, (V)DDPD*, (V)DDPS*, (V)HADDPD, (V)HADDP, (V)HSUBPD, (V)HSUBPS, (V)MAXPD, (V)MAXPS, (V)MINPD, (V)MINPS, (V)MULPD, (V)MULPS, (V)ROUNDPD, (V)ROUNDPS, (V)SQRTPD, (V)SQRTPS, (V)SUBPD, (V)SUBPS</td>
</tr>
<tr>
<td><strong>Type 3</strong></td>
<td>(V)ADDSD, (V)ADDSX, (V)CMPSD, (V)CMPSX, (V)CMISSD, (V)CMISSX, (V)CVTSD2PD, (V)CVTSD2X, (V)CVTS2SD, (V)CVTS2X, (V)CVTSD2SI, (V)CVTSD2SI, (V)CVTS2SD, (V)CVTSD2SI, (V)DIVSD, (V)DIVSS, (V)MAXSD, (V)MAXSS, (V)MINSD, (V)MINSX, (V)MULSD, (V)MULSS, (V)ROUNDSD, (V)ROUNDSS, (V)SQRTSD, (V)SQRTSS, (V)SUBSD, (V)SUBSS, (V)UCOMISSD, (V)UCOMISSX</td>
</tr>
</tbody>
</table>
| **Type 4**      | (V)AESDEC, (V)AESDECLAST, (V)AESENC, (V)AESENCLAST, (V)AESIMC, (V)AESKEYGENASSIST, (V)ANDPD, (V)ANDPS, (V)ANDNPD, (V)ANDNPS, (V)BLENDPD, (V)BLENDPS, (V)BLENDVPD, (V)BLENDVPS, (V)LDDQU, (V)MASKMOVDQU, (V)PTEST, (V)TESTPS, (V)TESTPD, (V)MOVDQU*, (V)MOVSHPDUP, (V)MOVSHPDUP, (V)MOVSHPDUP*, (V)MOVSHPDUP*, (V)IMPSADBw, (V)IMPSADSw, (V)IMPSASHw, (V)IMPSASHw, (V)IMPSASHw, (V)LDDQU, (V)LDDQU, (V)LDDQU, (V)LDDQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQU, (V)SINGLEQ}
INSTRUCTION FORMAT

Table 2-14 classifies exception behaviors for AVX instructions. Within each class of exception conditions that are listed in Table 2-17 through Table 2-24, certain subsets of AVX instructions may be subject to #UD exception depending on the encoded value of the VEX.L field. Table 2-16 provides supplemental information of AVX instructions that may be subject to #UD exception if encoded with incorrect values in the VEX.W or VEX.L field.

### Table 2-15. #UD Exception and VEX.W=1 Encoding

<table>
<thead>
<tr>
<th>Exception Class</th>
<th>#UD If VEX.W = 1 in all modes</th>
<th>#UD If VEX.W = 1 in non-64-bit modes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type 4</td>
<td>VBLENDVDP, VBLENDVPS, VPBLENDVB, VTESTPD, VTESTPS</td>
<td></td>
</tr>
<tr>
<td>Type 5</td>
<td>VPEXTRQ, VPINSRQ,</td>
<td></td>
</tr>
<tr>
<td>Type 6</td>
<td>VEXTRACTF128, VPERMILPD, VPERMILPS, VPERM2F128, VBROADCASTSS, VBROADCASTSD, VBROADCASTF128, VINSERTF128, VMASKMOVPS**, VMASKMOVPD**</td>
<td></td>
</tr>
<tr>
<td>Type 7</td>
<td>(V)MOVHLPS, (V)MOVHLPD, (V)MOVMSKPD, (V)MOVMSKPS, (V)PMOVMSKB, (V)PSLLDQ, (V)PSRLDQ, (V)PSLLD, (V)PSLLQ, (V)PSRAW, (V)PSRAD, (V)PSRLW, (V)PSRLD, (V)PSRLQ</td>
<td></td>
</tr>
<tr>
<td>Type 8</td>
<td>VZEROALL, VZEROUPPER</td>
<td></td>
</tr>
</tbody>
</table>
### Table 2-16. #UD Exception and VEX.L Field Encoding

<table>
<thead>
<tr>
<th>Exception Class</th>
<th>#UD if VEX.L = 0</th>
<th>#UD if VEX.L = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type 1</td>
<td>VMOVNTDQA</td>
<td></td>
</tr>
<tr>
<td>Type 2</td>
<td>VDPPD</td>
<td></td>
</tr>
<tr>
<td>Type 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type 4</td>
<td>VMASKMOVDQU, VMPSADBw, VPABSB/w/D, VPACKSSwB/Dw, VPACKUSwB/Dw, VPADDDB/w/D, VPADDQ, VPADDSB/w, VPADDUSB/w, VPALIGNR, VPAND, VPANDN, VPVGB/w, VPBLNDVQB, VPBLNDW, VPCMP(E)/I/STRI/M, VPCMPEQB/w/D/Q, VPCMPGTB/w/D/Q, VPHADDW/D, VPHADDSW, VPHMINPOSUw, VPHSUBD/w, VPHSUBSW, VPMADDWD, VPMADDSUBw, VPMAXSB/w/D, VPMAXUB/w/D, VPMINSB/w/D, VPMINUB/w/D, VPMULHUw, VPMULHRSW, VPMULhw/Lw, VPMULLD, VPMULUDQ, VPMULDQ, VPOR, VPSADBw, VPSHUFB/D, VPSHUFW/hw/lw, VPSIGNB/w/D, VPSLLw/D/Q, VPSRAw/D, VPSRLw/D/Q, VPSUBB/w/D/Q, VPSUBSB/w, VPUNPCKHBw/w/D/Q, VPUNPCKHWDQ, VPUNPCKLBw/w/D/Q, VPUNPCKLWDQ, VPXOR, VEXTRACTPS, VINSERTPS, VMOVd, VMOVq, VMOVLD, VMOVLPd, VMOVhP, VMOVHP, VPEXTRB, VPEXTRD, VPEXTRw, VPEXTRq, VPINSRB, VPINSRD, VPINSRW, VPINSRq, VPMOVSX/ZX, VLDMXCSR, VSTMXCSR, VEXTRACTF128, VPERM2F128, VBROADCASTSD, VBROADCASTF128, VINSERTF128,</td>
<td></td>
</tr>
<tr>
<td>Type 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type 6</td>
<td>VMOVhPS, VMOVSX/ZX, VPSLLDq, VPSRLDQ, VPSLLw, VPSLLD, VPSLLq, VPSRAw, VPSRAD, VPSRLw, VPSRLD, VPSRLq</td>
<td></td>
</tr>
<tr>
<td>Type 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type 8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 2.4.1 Exceptions Type 1 (Aligned memory reference)

#### Table 2-17. Type 1 Class Exception Conditions

<table>
<thead>
<tr>
<th>Exception</th>
<th>Real</th>
<th>Virtual 80x86</th>
<th>Protected and Compatibility</th>
<th>64-bit</th>
<th>Cause of Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid Opcode, #UD</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td>VEX prefix.</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X X</td>
<td></td>
<td></td>
<td>VEX prefix: If XCR0[2:1] = ‘11b’.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If CR4.OSXSAVE[bit 18] = 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X X X</td>
<td></td>
<td></td>
<td>Legacy SSE instruction: If CR0.EM[bit 2] = 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If CR4.OSFXSR[bit 9] = 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X X X</td>
<td></td>
<td></td>
<td>If preceded by a LOCK prefix (F0H).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If any REX, F2, F3, or 66 prefixes precede a VEX prefix.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X X X</td>
<td></td>
<td></td>
<td>If any corresponding CPUID feature flag is ‘0’.</td>
</tr>
<tr>
<td>Device Not Available, #NM</td>
<td>X</td>
<td>X X</td>
<td></td>
<td></td>
<td>If CR0.TS[bit 3] = 1.</td>
</tr>
<tr>
<td>Stack, SS(0)</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td>For an illegal address in the SS segment.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If a memory address referencing the SS segment is in a non-canonical form.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>General Protection, #GP(0)</td>
<td>X</td>
<td>X X</td>
<td></td>
<td></td>
<td>VEX.256: Memory operand is not 32-byte aligned.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VEX.128: Memory operand is not 16-byte aligned.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X X X</td>
<td></td>
<td></td>
<td>Legacy SSE: Memory operand is not 16-byte aligned.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>X</td>
<td></td>
<td>If the memory address is in a non-canonical form.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>X</td>
<td></td>
<td>If any part of the operand lies outside the effective address space from 0 to FFFFH.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Page Fault #PF(fault-code)</td>
<td>X</td>
<td>X X</td>
<td></td>
<td></td>
<td>For a page fault.</td>
</tr>
</tbody>
</table>
### 2.4.2 Exceptions Type 2 (>=16 Byte Memory Reference, Unaligned)

#### Table 2-18. Type 2 Class Exception Conditions

<table>
<thead>
<tr>
<th>Exception</th>
<th>Real</th>
<th>Virtual 8086</th>
<th>Protected and Compatibility</th>
<th>64-bit</th>
<th>Cause of Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid Opcode, #UD</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VEX prefix: If CR0.TS[bit 3]=1.</td>
</tr>
<tr>
<td>Device Not Available, #NM</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10]=0.</td>
</tr>
<tr>
<td>Stack, SS(0)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If preceded by a LOCK prefix (F0H).</td>
</tr>
<tr>
<td>General Protection, #GP(0)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If any corresponding CPUID feature flag is '0'.</td>
</tr>
<tr>
<td>Page Fault #PF(fault-code)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>For a page fault.</td>
</tr>
<tr>
<td>SIMD Floating-point Exception, #XM</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If any part of the operand lies outside the effective address space from 0 to FFFFH.</td>
</tr>
</tbody>
</table>
### 2.4.3 Exceptions Type 3 (<16 Byte memory argument)

Table 2-19. Type 3 Class Exception Conditions

<table>
<thead>
<tr>
<th>Exception</th>
<th>Real</th>
<th>Virtual 80x86</th>
<th>Protected and Compatibility</th>
<th>64-bit</th>
<th>Cause of Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid Opcode, #UD</td>
<td>X X</td>
<td></td>
<td></td>
<td></td>
<td>VEX prefix.</td>
</tr>
<tr>
<td></td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 0.</td>
</tr>
<tr>
<td></td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>VEX prefix:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If XCR0[2:1] != '11b'.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If CR4.OSXSAVE[bit 18]=0.</td>
</tr>
<tr>
<td></td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>Legacy SSE instruction:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If CR0.EM[bit 2] = 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If CR4.OSFXSR[bit 9] = 0.</td>
</tr>
<tr>
<td></td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>If preceded by a LOCK prefix (F0H).</td>
</tr>
<tr>
<td></td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>If any REX, F2, F3, or 66 prefixes precede a VEX prefix.</td>
</tr>
<tr>
<td></td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>If any corresponding CPUID feature flag is '0'.</td>
</tr>
<tr>
<td>Device Not Available, #NM</td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>If CR0.TS[bit 3]=1.</td>
</tr>
<tr>
<td>Stack, SS(0)</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td>For an illegal address in the SS segment.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If a memory address referencing the SS segment is in a non-canonical form.</td>
</tr>
<tr>
<td>General Protection, #GP(0)</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td>For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the memory address is in a non-canonical form.</td>
</tr>
<tr>
<td></td>
<td>X X</td>
<td></td>
<td></td>
<td></td>
<td>If any part of the operand lies outside the effective address space from 0 to FFFFH.</td>
</tr>
<tr>
<td>Page Fault #PF(fault-code)</td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>For a page fault.</td>
</tr>
<tr>
<td>Alignment Check #AC(0)</td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.</td>
</tr>
<tr>
<td>SIMD Floating-point Exception, #XM</td>
<td>X X</td>
<td>X X</td>
<td></td>
<td></td>
<td>If an unmasked SIMD floating-point exception and CR4.OSXMMEXCPT[bit 10] = 1.</td>
</tr>
</tbody>
</table>
# Exceptions Type 4 (>16 Byte mem arg no alignment, no floating-point exceptions)

## Table 2-20. Type 4 Class Exception Conditions

<table>
<thead>
<tr>
<th>Exception</th>
<th>Real</th>
<th>Virtual 80x86</th>
<th>Protected and Compatibility 64-bit</th>
<th>Cause of Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid Opcode, #UD</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VEX prefix.</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X X</td>
<td>X</td>
<td>Legacy SSE instruction:</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X X</td>
<td>X</td>
<td>If preceded by a LOCK prefix (F0H).</td>
</tr>
<tr>
<td>Device Not Available, #NM</td>
<td>X</td>
<td>X X</td>
<td>X</td>
<td>If any corresponding CPUID feature flag is '0'.</td>
</tr>
<tr>
<td>Stack, SS(0)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>For an illegal address in the SS segment.</td>
</tr>
<tr>
<td>General Protection, #GP(0)</td>
<td>X</td>
<td>X X</td>
<td>X</td>
<td>Legacy SSE: Memory operand is not 16-byte aligned.</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If the memory address is in a non-canonical form.</td>
</tr>
<tr>
<td>Page Fault #PF(fault-code)</td>
<td>X</td>
<td>X X</td>
<td>X</td>
<td>For a page fault.</td>
</tr>
</tbody>
</table>
### Exceptions Type 5 (<16 Byte mem arg and no FP exceptions)

**Table 2-21. Type 5 Class Exception Conditions**

<table>
<thead>
<tr>
<th>Exception</th>
<th>Real</th>
<th>Protected and Compatibility</th>
<th>64-bit</th>
<th>Cause of Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid Opcode, #UD</td>
<td>X</td>
<td>X</td>
<td></td>
<td>VEX prefix:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>VEX prefix: if XCR0[2:1] = ‘11b’. If CR4.OSXSAVE(bit 18) = 0.</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If preceded by a LOCK prefix (F0H).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If any REX, F2, F3, or 66 prefixes precede a VEX prefix.</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If any corresponding CPUID feature flag is ‘0’.</td>
</tr>
<tr>
<td>Device Not Available, #NM</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If CR0.TS[bit 3] = 1.</td>
</tr>
<tr>
<td>Stack, SS(0)</td>
<td></td>
<td></td>
<td>X</td>
<td>For an illegal address in the SS segment.</td>
</tr>
<tr>
<td>General Protection, #GP(0)</td>
<td></td>
<td></td>
<td>X</td>
<td>For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the memory address is in a non-canonical form.</td>
</tr>
<tr>
<td>Page Fault #PF(fault-code)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>For a page fault.</td>
</tr>
<tr>
<td>Alignment Check #AC(0)</td>
<td></td>
<td></td>
<td></td>
<td>If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.</td>
</tr>
</tbody>
</table>
2.4.6 Exceptions Type 6 (VEX-Encoded Instructions Without Legacy SSE Analogues)

Note: At present, the AVX instructions in this category do not generate floating-point exceptions.

Table 2-22. Type 6 Class Exception Conditions

<table>
<thead>
<tr>
<th>Exception</th>
<th>Real</th>
<th>Virtual 80x86</th>
<th>Protected and Compatibility</th>
<th>64-bit</th>
<th>Cause of Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid Opcode, #UD</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td>VEX prefix.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If XCR0[2:1]!=&quot;11b&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If CR4.OSXSAVE[bit 18]=0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If preceded by a LOCK prefix (F0H).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If any REX, F2, F3, or 66 prefixes precede a VEX prefix.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If any corresponding CPUID feature flag is '0'.</td>
</tr>
<tr>
<td>Device Not Available, #NM</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td>If CR0.TS[bit 3]=1.</td>
</tr>
<tr>
<td>Stack, SS(0)</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>For an illegal address in the SS segment.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If a memory address referencing the SS segment is in a non-canonical form.</td>
</tr>
<tr>
<td>General Protection, #GP(0)</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the memory address is in a non-canonical form.</td>
</tr>
<tr>
<td>Page Fault #PF(fault-code)</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td>For a page fault.</td>
</tr>
<tr>
<td>Alignment Check #AC(0)</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td>For 4 or 8 byte memory references if alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.</td>
</tr>
</tbody>
</table>
### 2.4.7 Exceptions Type 7 (No FP exceptions, no memory arg)

**Table 2-23. Type 7 Class Exception Conditions**

<table>
<thead>
<tr>
<th>Exception</th>
<th>Real</th>
<th>Virtual 80x86</th>
<th>Protected and Compatibility</th>
<th>64-bit</th>
<th>Cause of Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid Opcode, #UD</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td>VEX prefix.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device Not Available, #NM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Real**
- **Virtual 80x86**
- **Protected and Compatibility**
- **64-bit**
- **Cause of Exception**

- VEX prefix:
  - If XCR0[2:1] \(\neq \) ‘11b’.
  - If CR4.OSXSAVE[bit 18]=0.
  - XXX X
  - Legacy SSE instruction:
    - If CR0.EM[bit 2] = 1.
    - If CR4.OSFXSR[bit 9] = 0.
  - XXX X
  - If preceded by a LOCK prefix (F0H).
  - XXX X
  - If any REX, F2, F3, or 66 prefixes precede a VEX prefix.
  - XXX X
  - If any corresponding CPUID feature flag is ‘0’. 
  - XXX X
  - If CR0.TS[bit 3]=1.
### 2.4.8 Exceptions Type 8 (AVX and no memory argument)

**Table 2-24. Type 8 Class Exception Conditions**

<table>
<thead>
<tr>
<th>Exception</th>
<th>Real</th>
<th>Virtual 80x86</th>
<th>Protected and Compatibility 64-bit</th>
<th>Cause of Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid Opcode, #UD</td>
<td>X</td>
<td>X</td>
<td></td>
<td>Always in Real or Virtual 80x86 mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>If XCR0[2:1] = ‘11b’.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>If CR4.OSXSAVE[bit 18]=0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>If CPUID.01H.ECX.AVX[bit 28]=0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>If VEX.vvvv != 1111B.</td>
</tr>
<tr>
<td>Device Not Available, #NM</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>If proceeded by a LOCK prefix (F0H).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If CR0.TS[bit 3]=1.</td>
</tr>
</tbody>
</table>
This chapter describes the instruction set for the Intel 64 and IA-32 architectures (A-L) in IA-32e, protected, virtual-8086, and real-address modes of operation. The set includes general-purpose, x87 FPU, MMX, SSE/SSE2/SSE3/SSSE3/SSE4, AESNI/PCLMULQDQ, AVX and system instructions. See also Chapter 4, “Instruction Set Reference, M-Z,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B.

For each instruction, each operand combination is described. A description of the instruction and its operand, an operational description, a description of the effect of the instructions on flags in the EFLAGS register, and a summary of exceptions that can be generated are also provided.

3.1 INTERPRETING THE INSTRUCTION REFERENCE PAGES

This section describes the format of information contained in the instruction reference pages in this chapter. It explains notational conventions and abbreviations used in these sections.

3.1.1 Instruction Format

The following is an example of the format used for each instruction description in this chapter. The heading below introduces the example. The table below provides an example summary table.

CMC—Complement Carry Flag [this is an example]

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F5</td>
<td>CMC</td>
<td>A</td>
<td>V/V</td>
<td>NP</td>
<td>Complement carry flag.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
3.1.1.1 Opcode Column in the Instruction Summary Table (Instructions without VEX prefix)

The "Opcode" column in the table above shows the object code produced for each form of the instruction. When possible, codes are given as hexadecimal bytes in the same order in which they appear in memory. Definitions of entries other than hexadecimal bytes are as follows:

- **REX.W** — Indicates the use of a REX prefix that affects operand size or instruction semantics. The ordering of the REX prefix and other optional/mandatory instruction prefixes are discussed Chapter 2. Note that REX prefixes that promote legacy instructions to 64-bit behavior are not listed explicitly in the opcode column.

- **/digit** — A digit between 0 and 7 indicates that the ModR/M byte of the instruction uses only the r/m (register or memory) operand. The reg field contains the digit that provides an extension to the instruction's opcode.

- **/r** — Indicates that the ModR/M byte of the instruction contains a register operand and an r/m operand.

- **cb, cw, cd, cp, co, ct** — A 1-byte (cb), 2-byte (cw), 4-byte (cd), 6-byte (cp), 8-byte (co) or 10-byte (ct) value following the opcode. This value is used to specify a code offset and possibly a new value for the code segment register.

- **ib, iw, id, io** — A 1-byte (ib), 2-byte (iw), 4-byte (id) or 8-byte (io) immediate operand to the instruction that follows the opcode, ModR/M bytes or scale-indexing bytes. The opcode determines if the operand is a signed value. All words, doublewords and quadwords are given with the low-order byte first.

- **+rb, +rw, +rd, +ro** — A register code, from 0 through 7, added to the hexadecimal byte given at the left of the plus sign to form a single opcode byte. See Table 3-1 for the codes. The +ro columns in the table are applicable only in 64-bit mode.

- **+i** — A number used in floating-point instructions when one of the operands is ST(i) from the FPU register stack. The number i (which can range from 0 to 7) is added to the hexadecimal byte given at the left of the plus sign to form a single opcode byte.
### Table 3-1. Register Codes Associated With +rb, +rw, +rd, +ro

<table>
<thead>
<tr>
<th>byte register</th>
<th>word register</th>
<th>dword register</th>
<th>quadword register (64-Bit Mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td>REX.B</td>
<td>Reg Field</td>
<td>Register</td>
</tr>
<tr>
<td>AL</td>
<td>None</td>
<td>0</td>
<td>AX</td>
</tr>
<tr>
<td>CL</td>
<td>None</td>
<td>1</td>
<td>CX</td>
</tr>
<tr>
<td>DL</td>
<td>None</td>
<td>2</td>
<td>DX</td>
</tr>
<tr>
<td>BL</td>
<td>None</td>
<td>3</td>
<td>BX</td>
</tr>
<tr>
<td>AH</td>
<td>Not encod</td>
<td>4</td>
<td>SP</td>
</tr>
<tr>
<td></td>
<td>able (N.E.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH</td>
<td>N.E.</td>
<td>5</td>
<td>BP</td>
</tr>
<tr>
<td>DH</td>
<td>N.E.</td>
<td>6</td>
<td>SI</td>
</tr>
<tr>
<td>BH</td>
<td>N.E.</td>
<td>7</td>
<td>DI</td>
</tr>
<tr>
<td>SPL</td>
<td>Yes</td>
<td>4</td>
<td>SP</td>
</tr>
<tr>
<td>BPL</td>
<td>Yes</td>
<td>5</td>
<td>BP</td>
</tr>
<tr>
<td>SIL</td>
<td>Yes</td>
<td>6</td>
<td>SI</td>
</tr>
<tr>
<td>DIL</td>
<td>Yes</td>
<td>7</td>
<td>DI</td>
</tr>
<tr>
<td>Registers R8 - R15 (see below): Available in 64-Bit Mode Only</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R8L</td>
<td>Yes</td>
<td>0</td>
<td>R8W</td>
</tr>
<tr>
<td>R9L</td>
<td>Yes</td>
<td>1</td>
<td>R9W</td>
</tr>
<tr>
<td>RTOL</td>
<td>Yes</td>
<td>2</td>
<td>RT10W</td>
</tr>
<tr>
<td>RT1L</td>
<td>Yes</td>
<td>3</td>
<td>RT11W</td>
</tr>
<tr>
<td>R12L</td>
<td>Yes</td>
<td>4</td>
<td>RT2W</td>
</tr>
<tr>
<td>R13L</td>
<td>Yes</td>
<td>5</td>
<td>RT3W</td>
</tr>
<tr>
<td>R14L</td>
<td>Yes</td>
<td>6</td>
<td>RT4W</td>
</tr>
<tr>
<td>R15L</td>
<td>Yes</td>
<td>7</td>
<td>RT5W</td>
</tr>
</tbody>
</table>
3.1.1.2 Opcode Column in the Instruction Summary Table (Instructions with VEX prefix)

In the Instruction Summary Table, the Opcode column presents each instruction encoded using the VEX prefix in following form (including the modR/M byte if applicable, the immediate byte if applicable):

\[ \text{VEX.[NDS].[128,256].[66,F2,F3].0F/0F3A/0F38.[W0,W1] opcode [/r] [/ib,/is4]} \]

- **VEX:** indicates the presence of the VEX prefix is required. The VEX prefix can be encoded using the three-byte form (the first byte is C4H), or using the two-byte form (the first byte is C5H). The two-byte form of VEX only applies to those instructions that do not require the following fields to be encoded: VEX.mmmmm, VEX.W, VEX.X, VEX.B. Refer to Section 2.3 for more detail on the VEX prefix.

The encoding of various sub-fields of the VEX prefix is described using the following notations:

— **NDS, NDD, DDS:** specifies that VEX.vvvv field is valid for the encoding of a register operand:
  - VEX.NDS: VEX.vvvv encodes the first source register in an instruction syntax where the content of source registers will be preserved.
  - VEX.NDD: VEX.vvvv encodes the destination register that cannot be encoded by ModR/M:reg field.
  - VEX.DDS: VEX.vvvv encodes the second source register in a three-operand instruction syntax where the content of first source register will be overwritten by the result.
  - If none of NDS, NDD, and DDS is present, VEX.vvvv must be 1111b (i.e. VEX.vvvv does not encode an operand). The VEX.vvvv field can be encoded using either the 2-byte or 3-byte form of the VEX prefix.

— **128,256:** VEX.L field can be 0 (denoted by VEX.128 or VEX.LZ) or 1 (denoted by VEX.256). The VEX.L field can be encoded using either the 2-byte or 3-byte form of the VEX prefix. The presence of the notation VEX.256 or VEX.128 in the opcode column should be interpreted as follows:
  - If VEX.256 is present in the opcode column: The semantics of the instruction must be encoded with VEX.L = 1. An attempt to encode this instruction with VEX.L= 0 can result in one of two situations: (a) if VEX.128 version is defined, the processor will behave according to the defined VEX.128 behavior; (b) an #UD occurs if there is no VEX.128 version defined.
  - If VEX.128 is present in the opcode column but there is no VEX.256 version defined for the same opcode byte: Two situations apply: (a) For VEX-encoded, 128-bit SIMD integer instructions, software must encode the instruction with VEX.L = 0. The processor will treat the opcode byte encoded with VEX.L= 1 by causing an #UD exception; (b) For VEX-
encoded, 128-bit packed floating-point instructions, software must encode the instruction with VEX.L = 0. The processor will treat the opcode byte encoded with VEX.L= 1 by causing an #UD exception (e.g. VMOVLPs).

- If VEX.LIG is present in the opcode column: The VEX.L value is ignored. This generally applies to VEX-encoded scalar SIMD floating-point instructions. Scalar SIMD floating-point instruction can be distinguished from the mnemonic of the instruction. Generally, the last two letters of the instruction mnemonic would be either "SS", "SD", or "SI" for SIMD floating-point conversion instructions.

- If VEX.LZ is present in the opcode column: The VEX.L must be encoded to be 0B, an #UD occurs if VEX.L is not zero.

- **66,F2,F3:** The presence or absence of these values map to the VEX.pp field encodings. If absent, this corresponds to VEX.pp=00B. If present, the corresponding VEX.pp value affects the "opcode" byte in the same way as if a SIMD prefix (66H, F2H or F3H) does to the ensuing opcode byte. Thus a non-zero encoding of VEX.pp may be considered as an implied 66H/F2H/F3H prefix. The VEX.pp field may be encoded using either the 2-byte or 3-byte form of the VEX prefix.

- **0F,0F3A,0F38:** The presence maps to a valid encoding of the VEX.mmmmm field. Only three encoded values of VEX.mmmmm are defined as valid, corresponding to the escape byte sequence of 0FH, 0F3AH and 0F38H. The effect of a valid VEX.mmmmm encoding on the ensuing opcode byte is same as if the corresponding escape byte sequence on the ensuing opcode byte for non-VEX encoded instructions. Thus a valid encoding of VEX.mmmmm may be consider as an implies escape byte sequence of either 0FH, 0F3AH or 0F38H. The VEX.mmmmm field must be encoded using the 3-byte form of VEX prefix.

- **0F,0F3A,0F38 and 2-byte/3-byte VEX.** The presence of 0F3A and 0F38 in the opcode column implies that opcode can only be encoded by the three-byte form of VEX. The presence of 0F in the opcode column does not preclude the opcode to be encoded by the two-byte of VEX if the semantics of the opcode does not require any subfield of VEX not present in the two-byte form of the VEX prefix.

- **W0:** VEX.W=0.

- **W1:** VEX.W=1.

- The presence of W0/W1 in the opcode column applies to two situations: (a) it is treated as an extended opcode bit, (b) the instruction semantics support an operand size promotion to 64-bit of a general-purpose register operand or a 32-bit memory operand. The presence of W1 in the opcode column implies the opcode must be encoded using the 3-byte form of the VEX prefix. The presence of W0 in the opcode column does not preclude the opcode to be encoded using the CSH form of the VEX prefix, if the semantics of the opcode
does not require other VEX subfields not present in the two-byte form of the VEX prefix. Please see Section 2.3 on the subfield definitions within VEX.

— **WIG:** can use C5H form (if not requiring VEX.mmmmm) or VEX.W value is ignored in the C4H form of VEX prefix.

— If WIG is present, the instruction may be encoded using either the two-byte form or the three-byte form of VEX. When encoding the instruction using the three-byte form of VEX, the value of VEX.W is ignored.

- **opcode:** Instruction opcode.
- **/is4:** An 8-bit immediate byte is present containing a source register specifier in imm[7:4] and instruction-specific payload in imm[3:0].
- In general, the encoding of VEX.R, VEX.X, VEX.B field are not shown explicitly in the opcode column. The encoding scheme of VEX.R, VEX.X, VEX.B fields must follow the rules defined in Section 2.3.

### 3.1.1.3 Instruction Column in the Opcode Summary Table

The "Instruction" column gives the syntax of the instruction statement as it would appear in an ASM386 program. The following is a list of the symbols used to represent operands in the instruction statements:

- **rel8** — A relative address in the range from 128 bytes before the end of the instruction to 127 bytes after the end of the instruction.
- **rel16, rel32** — A relative address within the same code segment as the instruction assembled. The rel16 symbol applies to instructions with an operand-size attribute of 16 bits; the rel32 symbol applies to instructions with an operand-size attribute of 32 bits.
- **ptr16:16, ptr16:32** — A far pointer, typically to a code segment different from that of the instruction. The notation 16:16 indicates that the value of the pointer has two parts. The value to the left of the colon is a 16-bit selector or value destined for the code segment register. The value to the right corresponds to the offset within the destination segment. The ptr16:16 symbol is used when the instruction's operand-size attribute is 16 bits; the ptr16:32 symbol is used when the operand-size attribute is 32 bits.
- **r8** — One of the byte general-purpose registers: AL, CL, DL, BL, AH, CH, DH, BH, BPL, SPL, DIL and SIL; or one of the byte registers (R8L - R15L) available when using REX.R and 64-bit mode.
- **r16** — One of the word general-purpose registers: AX, CX, DX, BX, SP, BP, SI, DI; or one of the word registers (R8-R15) available when using REX.R and 64-bit mode.
- **r32** — One of the doubleword general-purpose registers: EAX, ECX, EDX, EBX, ESP, EBP, ESI,EDI; or one of the doubleword registers (R8D - R15D) available when using REX.R in 64-bit mode.
• **r64** — One of the quadword general-purpose registers: RAX, RBX, RCX, RDX, RDI, RSI, RBP, RSP, R8–R15. These are available when using REX.R and 64-bit mode.

• **imm8** — An immediate byte value. The imm8 symbol is a signed number between –128 and +127 inclusive. For instructions in which imm8 is combined with a word or doubleword operand, the immediate value is sign-extended to form a word or doubleword. The upper byte of the word is filled with the topmost bit of the immediate value.

• **imm16** — An immediate word value used for instructions whose operand-size attribute is 16 bits. This is a number between –32,768 and +32,767 inclusive.

• **imm32** — An immediate doubleword value used for instructions whose operand-size attribute is 32 bits. It allows the use of a number between +2,147,483,647 and –2,147,483,648 inclusive.

• **imm64** — An immediate quadword value used for instructions whose operand-size attribute is 64 bits. The value allows the use of a number between +9,223,372,036,854,775,807 and –9,223,372,036,854,775,808 inclusive.

• **r/m8** — A byte operand that is either the contents of a byte general-purpose register (AL, CL, DL, BL, AH, CH, DH, BH, BPL, SPL, DIL and SIL) or a byte from memory. Byte registers R8L - R15L are available using REX.R in 64-bit mode.

• **r/m16** — A word general-purpose register or memory operand used for instructions whose operand-size attribute is 16 bits. The word general-purpose registers are: AX, CX, DX, BX, SP, BP, SI, DI. The contents of memory are found at the address provided by the effective address computation. Word registers R8W - R15W are available using REX.R in 64-bit mode.

• **r/m32** — A doubleword general-purpose register or memory operand used for instructions whose operand-size attribute is 32 bits. The doubleword general-purpose registers are: EAX, ECX, EDX, EBX, ESP, EBP, ESI, EDI. The contents of memory are found at the address provided by the effective address computation. Doubleword registers R8D - R15D are available when using REX.R in 64-bit mode.

• **r/m64** — A quadword general-purpose register or memory operand used for instructions whose operand-size attribute is 64 bits when using REX.W. Quadword general-purpose registers are: RAX, RBX, RCX, RDX, RDI, RSI, RBP, RSP, R8–R15; these are available only in 64-bit mode. The contents of memory are found at the address provided by the effective address computation.

• **m** — A 16-, 32- or 64-bit operand in memory.

• **m8** — A byte operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. In 64-bit mode, it is pointed to by the RSI or RDI registers.

• **m16** — A word operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. This nomenclature is used only with the string instructions.
• **m32** — A doubleword operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. This nomenclature is used only with the string instructions.

• **m64** — A memory quadword operand in memory.

• **m128** — A memory double quadword operand in memory.

• **m16:16, m16:32 & m16:64** — A memory operand containing a far pointer composed of two numbers. The number to the left of the colon corresponds to the pointer's segment selector. The number to the right corresponds to its offset.

• **m16&32, m16&16, m32&32, m16&64** — A memory operand consisting of data item pairs whose sizes are indicated on the left and the right side of the ampersand. All memory addressing modes are allowed. The m16&16 and m32&32 operands are used by the BOUND instruction to provide an operand containing an upper and lower bounds for array indices. The m16&32 operand is used by LIDT and LGDT to provide a word with which to load the limit field, and a doubleword with which to load the base field of the corresponding GDTR and IDTR registers. The m16&64 operand is used by LIDT and LGDT in 64-bit mode to provide a word with which to load the limit field, and a quadword with which to load the base field of the corresponding GDTR and IDTR registers.

• **moffs8, moffs16, moffs32, moffs64** — A simple memory variable (memory offset) of type byte, word, or doubleword used by some variants of the MOV instruction. The actual address is given by a simple offset relative to the segment base. No ModR/M byte is used in the instruction. The number shown with moffs indicates its size, which is determined by the address-size attribute of the instruction.

• **Sreg** — A segment register. The segment register bit assignments are ES = 0, CS = 1, SS = 2, DS = 3, FS = 4, and GS = 5.

• **m32fp, m64fp, m80fp** — A single-precision, double-precision, and double extended-precision (respectively) floating-point operand in memory. These symbols designate floating-point values that are used as operands for x87 FPU floating-point instructions.

• **m16int, m32int, m64int** — A word, doubleword, and quadword integer (respectively) operand in memory. These symbols designate integers that are used as operands for x87 FPU integer instructions.

• **ST or ST(0)** — The top element of the FPU register stack.

• **ST(i)** — The i\textsuperscript{th} element from the top of the FPU register stack (i ← 0 through 7).

• **mm** — An MMX register. The 64-bit MMX registers are: MM0 through MM7.

• **mm/m32** — The low order 32 bits of an MMX register or a 32-bit memory operand. The 64-bit MMX registers are: MM0 through MM7. The contents of memory are found at the address provided by the effective address computation.

• **mm/m64** — An MMX register or a 64-bit memory operand. The 64-bit MMX registers are: MM0 through MM7. The contents of memory are found at the address provided by the effective address computation.
• **xmm** — An XMM register. The 128-bit XMM registers are: XMM0 through XMM7; XMM8 through XMM15 are available using REX.R in 64-bit mode.

• **xmm/m32** — An XMM register or a 32-bit memory operand. The 128-bit XMM registers are XMM0 through XMM7; XMM8 through XMM15 are available using REX.R in 64-bit mode. The contents of memory are found at the address provided by the effective address computation.

• **xmm/m64** — An XMM register or a 64-bit memory operand. The 128-bit SIMD floating-point registers are XMM0 through XMM7; XMM8 through XMM15 are available using REX.R in 64-bit mode. The contents of memory are found at the address provided by the effective address computation.

• **xmm/m128** — An XMM register or a 128-bit memory operand. The 128-bit XMM registers are XMM0 through XMM7; XMM8 through XMM15 are available using REX.R in 64-bit mode. The contents of memory are found at the address provided by the effective address computation.

• **<XMM0>** — indicates implied use of the XMM0 register. When there is ambiguity, xmm1 indicates the first source operand using an XMM register and xmm2 the second source operand using an XMM register.

Some instructions use the XMM0 register as the third source operand, indicated by **<XMM0>**. The use of the third XMM register operand is implicit in the instruction encoding and does not affect the ModR/M encoding.

• **ymm** — a YMM register. The 256-bit YMM registers are: YMM0 through YMM7; YMM8 through YMM15 are available in 64-bit mode.

• **m256** — A 32-byte operand in memory. This nomenclature is used only with AVX instructions.

• **ymm/m256** — a YMM register or 256-bit memory operand.

• **<YMM0>** — indicates use of the YMM0 register as an implicit argument.

• **SRC1** — Denotes the first source operand in the instruction syntax of an instruction encoded with the VEX prefix and having two or more source operands.

• **SRC2** — Denotes the second source operand in the instruction syntax of an instruction encoded with the VEX prefix and having two or more source operands.

• **SRC3** — Denotes the third source operand in the instruction syntax of an instruction encoded with the VEX prefix and having three source operands.

• **SRC** — The source in a AVX single-source instruction or the source in a Legacy SSE instruction.

• **DST** — the destination in a AVX instruction. In Legacy SSE instructions can be either the destination, first source, or both. This field is encoded by reg_field.

### 3.1.1.4 Operand Encoding Column in the Instruction Summary Table

The “operand encoding” column is abbreviated as Op/En in the Instruction Summary table heading. Instruction operand encoding information is provided for each
assembly instruction syntax using a letter to cross reference to a row entry in the operand encoding definition table that follows the instruction summary table. The operand encoding table in each instruction reference page lists each instruction operand (according to each instruction syntax and operand ordering shown in the instruction column) relative to the ModRM byte, VEX.vvvv field or additional operand encoding placement.

**NOTES**

- The letters in the Op/En column of an instruction apply ONLY to the encoding definition table immediately following the instruction summary table.
- In the encoding definition table, the letter ‘r’ within a pair of parenthesis denotes the content of the operand will be read by the processor. The letter ‘w’ within a pair of parenthesis denotes the content of the operand will be updated by the processor.

### 3.1.1.5 64/32-bit Mode Column in the Instruction Summary Table

The "64/32-bit Mode" column indicates whether the opcode sequence is supported in (a) 64-bit mode or (b) the Compatibility mode and other IA-32 modes that apply in conjunction with the CPUID feature flag associated specific instruction extensions.

The 64-bit mode support is to the left of the 'slash' and has the following notation:

- **V** — Supported.
- **I** — Not supported.
- **N.E.** — Indicates an instruction syntax is not encodable in 64-bit mode (it may represent part of a sequence of valid instructions in other modes).
- **N.P.** — Indicates the REX prefix does not affect the legacy instruction in 64-bit mode.
- **N.I.** — Indicates the opcode is treated as a new instruction in 64-bit mode.
- **N.S.** — Indicates an instruction syntax that requires an address override prefix in 64-bit mode and is not supported. Using an address override prefix in 64-bit mode may result in model-specific execution behavior.

The Compatibility/Legacy Mode support is to the right of the 'slash' and has the following notation:

- **V** — Supported.
- **I** — Not supported.
- **N.E.** — Indicates an Intel 64 instruction mnemonics/syntax that is not encodable; the opcode sequence is not applicable as an individual instruction in compatibility mode or IA-32 mode. The opcode may represent a valid sequence of legacy IA-32 instructions.
3.1.1.6 CPUID Support Column in the Instruction Summary Table
The fourth column holds abbreviated CPUID feature flags (e.g. appropriate bit in CPUID.1.ECX, CPUID.1.EDX for SSE/SSE2/SSE3/SSSE3/SSE4.1/SSE4.2/AES-NI/PCLMULQDQ/AVX/RDRAND support) that indicate processor support for the instruction. If the corresponding flag is '0', the instruction will #UD.

3.1.1.7 Description Column in the Instruction Summary Table
The “Description” column briefly explains forms of the instruction.

3.1.1.8 Description Section
Each instruction is then described by number of information sections. The “Description” section describes the purpose of the instructions and required operands in more detail.

Summary of terms that may be used in the description section:
• **Legacy SSE**: Refers to SSE, SSE2, SSE3, SSSE3, SSE4, AESNI, PCLMULQDQ and any future instruction sets referencing XMM registers and encoded without a VEX prefix.
• **VEX.vvvv**. The VEX bitfield specifying a source or destination register (in 1’s complement form).
• **rm_field**: shorthand for the ModR/M r/m field and any REX.B
• **reg_field**: shorthand for the ModR/M reg field and any REX.R

3.1.1.9 Operation Section
The “Operation” section contains an algorithm description (frequently written in pseudo-code) for the instruction. Algorithms are composed of the following elements:
• Comments are enclosed within the symbol pairs "(*) and "(*)."
• Compound statements are enclosed in keywords, such as: IF, THEN, ELSE and FI for an if statement; DO and OD for a do statement; or CASE... OF for a case statement.
• A register name implies the contents of the register. A register name enclosed in brackets implies the contents of the location whose address is contained in that register. For example, ES:[DI] indicates the contents of the location whose ES segment relative address is in register DI. [SI] indicates the contents of the address contained in register SI relative to the SI register's default segment (DS) or the overridden segment.
• Parentheses around the “E” in a general-purpose register name, such as (E)SI, indicates that the offset is read from the SI register if the address-size attribute is 16, from the ESI register if the address-size attribute is 32. Parentheses
around the "R" in a general-purpose register name, (R)SI, in the presence of a 64-bit register definition such as (R)SI, indicates that the offset is read from the 64-bit RSI register if the address-size attribute is 64.

• Brackets are used for memory operands where they mean that the contents of the memory location is a segment-relative offset. For example, [SRC] indicates that the content of the source operand is a segment-relative offset.

• A ← B indicates that the value of B is assigned to A.

• The symbols =, ≠, >, <, ≥, and ≤ are relational operators used to compare two values: meaning equal, not equal, greater or equal, less or equal, respectively. A relational expression such as A ← B is TRUE if the value of A is equal to B; otherwise it is FALSE.

• The expression "« COUNT" and "» COUNT" indicates that the destination operand should be shifted left or right by the number of bits indicated by the count operand.

The following identifiers are used in the algorithmic descriptions:

• **OperandSize** and **AddressSize** — The OperandSize identifier represents the operand-size attribute of the instruction, which is 16, 32 or 64-bits. The AddressSize identifier represents the address-size attribute, which is 16, 32 or 64-bits. For example, the following pseudo-code indicates that the operand-size attribute depends on the form of the MOV instruction used.

  IF Instruction ← MOVW
  THEN OperandSize = 16;
  ELSE
    IF Instruction ← MOVD
    THEN OperandSize = 32;
    ELSE
      IF Instruction ← MOVQ
      THEN OperandSize = 64;
      FI;
    FI;
  FI;

  See “Operand-Size and Address-Size Attributes” in Chapter 3 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for guidelines on how these attributes are determined.

• **StackAddrSize** — Represents the stack address-size attribute associated with the instruction, which has a value of 16, 32 or 64-bits. See "Address-Size Attribute for Stack" in Chapter 6, “Procedure Calls, Interrupts, and Exceptions,” of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*.

• **SRC** — Represents the source operand.

• **DEST** — Represents the destination operand.

• **VLMAX** — The maximum vector register width pertaining to the instruction. This is not the vector-length encoding in the instruction’s prefix but is instead
determined by the current value of XCR0. For existing processors, VLMAX is 256 whenever XCR0.YMM[bit 2] is 1. Future processors may define new bits in XCR0 whose setting may imply other values for VLMAX.

**VLMAX Definition**

<table>
<thead>
<tr>
<th>XCR0 Component</th>
<th>VLMAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCR0.YMM</td>
<td>256</td>
</tr>
</tbody>
</table>

The following functions are used in the algorithmic descriptions:

- **ZeroExtend(value)** — Returns a value zero-extended to the operand-size attribute of the instruction. For example, if the operand-size attribute is 32, zero extending a byte value of –10 converts the byte from F6H to a doubleword value of 000000F6H. If the value passed to the ZeroExtend function and the operand-size attribute are the same size, ZeroExtend returns the value unaltered.

- **SignExtend(value)** — Returns a value sign-extended to the operand-size attribute of the instruction. For example, if the operand-size attribute is 32, sign extending a byte containing the value –10 converts the byte from F6H to a doubleword value of FFFFFFF6H. If the value passed to the SignExtend function and the operand-size attribute are the same size, SignExtend returns the value unaltered.

- **SaturateSignedWordToSignedByte** — Converts a signed 16-bit value to a signed 8-bit value. If the signed 16-bit value is less than –128, it is represented by the saturated value -128 (80H); if it is greater than 127, it is represented by the saturated value 127 (7FH).

- **SaturateSignedDwordToSignedWord** — Converts a signed 32-bit value to a signed 16-bit value. If the signed 32-bit value is less than –32768, it is represented by the saturated value –32768 (8000H); if it is greater than 32767, it is represented by the saturated value 32767 (7FFFH).

- **SaturateSignedWordToUnsignedByte** — Converts a signed 16-bit value to an unsigned 8-bit value. If the signed 16-bit value is less than zero, it is represented by the saturated value zero (00H); if it is greater than 255, it is represented by the saturated value 255 (FFH).

- **SaturateToSignedByte** — Represents the result of an operation as a signed 8-bit value. If the result is less than –128, it is represented by the saturated value –128 (80H); if it is greater than 127, it is represented by the saturated value 127 (7FH).

- **SaturateToSignedWord** — Represents the result of an operation as a signed 16-bit value. If the result is less than –32768, it is represented by the saturated value –32768 (8000H); if it is greater than 32767, it is represented by the saturated value 32767 (7FFFH).

- **SaturateToUnsignedByte** — Represents the result of an operation as a signed 8-bit value. If the result is less than zero it is represented by the saturated value
zero (00H); if it is greater than 255, it is represented by the saturated value 255 (FFH).

- **SaturateToUnsignedWord** — Represents the result of an operation as a signed 16-bit value. If the result is less than zero it is represented by the saturated value zero (00H); if it is greater than 65535, it is represented by the saturated value 65535 (FFFFH).

- **LowOrderWord(DEST * SRC)** — Multiplies a word operand by a word operand and stores the least significant word of the doubleword result in the destination operand.

- **HighOrderWord(DEST * SRC)** — Multiplies a word operand by a word operand and stores the most significant word of the doubleword result in the destination operand.

- **Push(value)** — Pushes a value onto the stack. The number of bytes pushed is determined by the operand-size attribute of the instruction. See the “Operation” subsection of the “PUSH—Push Word, Doubleword or Quadword Onto the Stack” section in Chapter 4 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*.

- **Pop()** removes the value from the top of the stack and returns it. The statement EAX ← Pop(); assigns to EAX the 32-bit value from the top of the stack. Pop will return either a word, a doubleword or a quadword depending on the operand-size attribute. See the “Operation” subsection in the “POP—Pop a Value from the Stack” section of Chapter 4 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*.

- **PopRegisterStack** — Marks the FPU ST(0) register as empty and increments the FPU register stack pointer (TOP) by 1.

- **Switch-Tasks** — Performs a task switch.

- **Bit(BitBase, BitOffset)** — Returns the value of a bit within a bit string. The bit string is a sequence of bits in memory or a register. Bits are numbered from low-order to high-order within registers and within memory bytes. If the BitBase is a register, the BitOffset can be in the range 0 to [15, 31, 63] depending on the mode and register size. See Figure 3-1: the function Bit[RAX, 21] is illustrated.

![Figure 3-1. Bit Offset for BIT[RAX, 21]](image-url)
If BitBase is a memory address, the BitOffset can range has different ranges depending on the operand size (see Table 3-2).

### Table 3-2. Range of Bit Positions Specified by Bit Offset Operands

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Immediate BitOffset</th>
<th>Register BitOffset</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>0 to 15</td>
<td>$-2^{15}$ to $2^{15} - 1$</td>
</tr>
<tr>
<td>32</td>
<td>0 to 31</td>
<td>$-2^{31}$ to $2^{31} - 1$</td>
</tr>
<tr>
<td>64</td>
<td>0 to 63</td>
<td>$-2^{63}$ to $2^{63} - 1$</td>
</tr>
</tbody>
</table>

The addressed bit is numbered (Offset MOD 8) within the byte at address (BitBase + (BitOffset DIV 8)) where DIV is signed division with rounding towards negative infinity and MOD returns a positive number (see Figure 3-2).

![Figure 3-2. Memory Bit Indexing](image)

### 3.1.1.10 Intel® C/C++ Compiler Intrinsics Equivalents Section

The Intel C/C++ compiler intrinsics equivalents are special C/C++ coding extensions that allow using the syntax of C function calls and C variables instead of hardware registers. Using these intrinsics frees programmers from having to manage registers and assembly programming. Further, the compiler optimizes the instruction scheduling so that executable run faster.

The following sections discuss the intrinsics API and the MMX technology and SIMD floating-point intrinsics. Each intrinsic equivalent is listed with the instruction description. There may be additional intrinsics that do not have an instruction equiv-

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It is strongly recommended that the reader reference the compiler documentation for the complete list of supported intrinsics.


**Intrinsics API**

The benefit of coding with MMX technology intrinsics and the SSE/SSE2/SSE3 intrinsics is that you can use the syntax of C function calls and C variables instead of hardware registers. This frees you from managing registers and programming assembly. Further, the compiler optimizes the instruction scheduling so that your executable runs faster. For each computational and data manipulation instruction in the new instruction set, there is a corresponding C intrinsic that implements it directly. The intrinsics allow you to specify the underlying implementation (instruction selection) of an algorithm yet leave instruction scheduling and register allocation to the compiler.

**MMX™ Technology Intrinsics**

The MMX technology intrinsics are based on a __m64 data type that represents the specific contents of an MMX technology register. You can specify values in bytes, short integers, 32-bit values, or a 64-bit object. The __m64 data type, however, is not a basic ANSI C data type, and therefore you must observe the following usage restrictions:

- Use __m64 data only on the left-hand side of an assignment, as a return value, or as a parameter. You cannot use it with other arithmetic expressions ("+", ">>", and so on).
- Use __m64 objects in aggregates, such as unions to access the byte elements and structures; the address of an __m64 object may be taken.
- Use __m64 data only with the MMX technology intrinsics described in this manual and Intel® C/C++ compiler documentation.
- See:
  - SSE/SSE2/SSE3 Intrinsics
  - SSE/SSE2/SSE3 intrinsics all make use of the XMM registers of the Pentium III, Pentium 4, and Intel Xeon processors. There are three data types supported by these intrinsics: __m128, __m128d, and __m128i.
• The __m128 data type is used to represent the contents of an XMM register used by an SSE intrinsic. This is either four packed single-precision floating-point values or a scalar single-precision floating-point value.
• The __m128d data type holds two packed double-precision floating-point values or a scalar double-precision floating-point value.
• The __m128i data type can hold sixteen byte, eight word, or four doubleword, or two quadword integer values.

The compiler aligns __m128, __m128d, and __m128i local and global data to 16-byte boundaries on the stack. To align integer, float, or double arrays, use thedeclspec statement as described in Intel C/C++ compiler documentation. See http://www.intel.com/support/performancetools/.

The __m128, __m128d, and __m128i data types are not basic ANSI C data types and therefore some restrictions are placed on its usage:
• Use __m128, __m128d, and __m128i only on the left-hand side of an assignment, as a return value, or as a parameter. Do not use it in other arithmetic expressions such as “+” and “>>.”
• Do not initialize __m128, __m128d, and __m128i with literals; there is no way to express 128-bit constants.
• Use __m128, __m128d, and __m128i objects in aggregates, such as unions (for example, to access the float elements) and structures. The address of these objects may be taken.
• Use __m128, __m128d, and __m128i data only with the intrinsics described in this user’s guide. See Appendix C, “Intel® C/C++ Compiler Intrinsics and Functional Equivalents,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2C, for more information on using intrinsics.

The compiler aligns __m128, __m128d, and __m128i local data to 16-byte boundaries on the stack. Global __m128 data is also aligned on 16-byte boundaries. (To align float arrays, you can use the alignmentdeclspec described in the following section.) Because the new instruction set treats the SIMD floating-point registers in the same way whether you are using packed or scalar data, there is no __m32 data type to represent scalar data as you might expect. For scalar operations, you should use the __m128 objects and the “scalar” forms of the intrinsics; the compiler and the processor implement these operations with 32-bit memory references.

The suffixes ps and ss are used to denote “packed single” and “scalar single” precision operations. The packed floats are represented in right-to-left order, with the lowest word (right-most) being used for scalar operations: [z, y, x, w]. To explain how memory storage reflects this, consider the following example.

The operation:

```c
float a[4] ← [ 1.0, 2.0, 3.0, 4.0 ];
__m128 t ← _mm_load_ps(a);
```

Produces the same result as follows:
INSTRUCTION SET REFERENCE, A-L

__m128 t ← _mm_set_ps(4.0, 3.0, 2.0, 1.0);

In other words:

\[ t ← [4.0, 3.0, 2.0, 1.0] \]

Where the “scalar” element is 1.0.

Some intrinsics are “composites” because they require more than one instruction to implement them. You should be familiar with the hardware features provided by the SSE, SSE2, SSE3, and MMX technology when writing programs with the intrinsics.

Keep the following important issues in mind:

- Certain intrinsics, such as _mm_loadr_ps and _mm_cmpgt_ss, are not directly supported by the instruction set. While these intrinsics are convenient programming aids, be mindful of their implementation cost.
- Data loaded or stored as __m128 objects must generally be 16-byte-aligned.
- Some intrinsics require that their argument be immediates, that is, constant integers (literals), due to the nature of the instruction.
- The result of arithmetic operations acting on two NaN (Not a Number) arguments is undefined. Therefore, floating-point operations using NaN arguments may not match the expected behavior of the corresponding assembly instructions.

For a more detailed description of each intrinsic and additional information related to its usage, refer to Intel C/C++ compiler documentation. See:

— http://www.intel.com/support/performancetools/


3.1.1.11  Flags Affected Section

The “Flags Affected” section lists the flags in the EFLAGS register that are affected by the instruction. When a flag is cleared, it is equal to 0; when it is set, it is equal to 1. The arithmetic and logical instructions usually assign values to the status flags in a uniform manner (see Appendix A, “EFLAGS Cross-Reference,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). Non-conventional assignments are described in the “Operation” section. The values of flags listed as undefined may be changed by the instruction in an indeterminate manner. Flags that are not listed are unchanged by the instruction.

3.1.1.12  FPU Flags Affected Section

The floating-point instructions have an “FPU Flags Affected” section that describes how each instruction can affect the four condition code flags of the FPU status word.
### Protected Mode Exceptions Section

The "Protected Mode Exceptions" section lists the exceptions that can occur when the instruction is executed in protected mode and the reasons for the exceptions. Each exception is given a mnemonic that consists of a pound sign (#) followed by two letters and an optional error code in parentheses. For example, #GP(0) denotes a general protection exception with an error code of 0. Table 3-3 associates each two-letter mnemonic with the corresponding interrupt vector number and exception name. See Chapter 6, "Interrupt and Exception Handling," in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for a detailed description of the exceptions.

Application programmers should consult the documentation provided with their operating systems to determine the actions taken when exceptions occur.

#### Table 3-3. Intel 64 and IA-32 General Exceptions

<table>
<thead>
<tr>
<th>Vector No.</th>
<th>Name</th>
<th>Source</th>
<th>Protected Mode</th>
<th>Real Address Mode</th>
<th>Virtual 8086 Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>#DE—Divide Error</td>
<td>DIV and IDIV instructions.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>1</td>
<td>#DB—Debug</td>
<td>Any code or data reference.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>#BP—Breakpoint</td>
<td>INT 3 instruction.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>#OF—Overflow</td>
<td>INTO instruction.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>#BR—BOUND Range Exceeded</td>
<td>BOUND instruction.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>6</td>
<td>#UD—Invalid Opcode (Undefined Opcode)</td>
<td>UD2 instruction or reserved opcode.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>7</td>
<td>#NM—Device Not Available (No Math Coprocessor)</td>
<td>Floating-point or WAIT/FWAIT instruction.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>8</td>
<td>#DF—Double Fault</td>
<td>Any instruction that can generate an exception, an NMI, or an INTR.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>10</td>
<td>#TS—Invalid TSS</td>
<td>Task switch or TSS access.</td>
<td>Yes</td>
<td>Reserved</td>
<td>Yes</td>
</tr>
<tr>
<td>11</td>
<td>#NP—Segment Not Present</td>
<td>Loading segment registers or accessing system segments.</td>
<td>Yes</td>
<td>Reserved</td>
<td>Yes</td>
</tr>
<tr>
<td>12</td>
<td>#SS—Stack Segment Fault</td>
<td>Stack operations and SS register loads.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>13</td>
<td>#GP—General Protection²</td>
<td>Any memory reference and other protection checks.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-L

Table 3-3. Intel 64 and IA-32 General Exceptions (Contd.)

<table>
<thead>
<tr>
<th>Vector No.</th>
<th>Name</th>
<th>Source</th>
<th>Protected Mode</th>
<th>Real Address Mode</th>
<th>Virtual 8086 Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>#PF—Page Fault</td>
<td>Any memory reference.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>16</td>
<td>#MF—Floating-Point Error (Math Fault)</td>
<td>Floating-point or WAIT/FWAIT</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>17</td>
<td>#AC—Alignment Check</td>
<td>Any data reference in memory.</td>
<td>Yes</td>
<td>Reserved</td>
<td>Yes</td>
</tr>
<tr>
<td>18</td>
<td>#MC—Machine Check</td>
<td>Model dependent machine</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>19</td>
<td>#XM—SIMD Floating-Point Numeric Error</td>
<td>SSE/SSE2/SSE3 floating-point</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

NOTES:
1. Apply to protected mode, compatibility mode, and 64-bit mode.
2. In the real-address mode, vector 13 is the segment overrun exception.

3.1.1.14 Real-Address Mode Exceptions Section

The "Real-Address Mode Exceptions" section lists the exceptions that can occur when the instruction is executed in real-address mode (see Table 3-3).

3.1.1.15 Virtual-8086 Mode Exceptions Section

The "Virtual-8086 Mode Exceptions" section lists the exceptions that can occur when the instruction is executed in virtual-8086 mode (see Table 3-3).

3.1.1.16 Floating-Point Exceptions Section

The "Floating-Point Exceptions" section lists exceptions that can occur when an x87 FPU floating-point instruction is executed. All of these exception conditions result in a floating-point error exception (#MF, vector number 16) being generated. Table 3-4 associates a one- or two-letter mnemonic with the corresponding exception name. See "Floating-Point Exception Conditions" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for a detailed description of these exceptions.
3.1.1.17  SIMD Floating-Point Exceptions Section

The “SIMD Floating-Point Exceptions” section lists exceptions that can occur when an SSE/SSE2/SSE3 floating-point instruction is executed. All of these exception conditions result in a SIMD floating-point error exception (#XM, vector number 19) being generated. Table 3-5 associates a one-letter mnemonic with the corresponding exception name. For a detailed description of these exceptions, refer to “SSE and SSE2 Exceptions”, in Chapter 11 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

Table 3-5. SIMD Floating-Point Exceptions

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Name</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>#I</td>
<td>Floating-point invalid operation</td>
<td>Invalid arithmetic operation or source operand</td>
</tr>
<tr>
<td>#Z</td>
<td>Floating-point divide-by-zero</td>
<td>Divide-by-zero</td>
</tr>
<tr>
<td>#D</td>
<td>Floating-point denormal operand</td>
<td>Source operand that is a denormal number</td>
</tr>
<tr>
<td>#O</td>
<td>Floating-point numeric overflow</td>
<td>Overflow in result</td>
</tr>
<tr>
<td>#U</td>
<td>Floating-point numeric underflow</td>
<td>Underflow in result</td>
</tr>
<tr>
<td>#P</td>
<td>Floating-point inexact result (precision)</td>
<td>Inexact result (precision)</td>
</tr>
</tbody>
</table>

3.1.1.18  Compatibility Mode Exceptions Section

This section lists exceptions that occur within compatibility mode.

3.1.1.19  64-Bit Mode Exceptions Section

This section lists exceptions that occur within 64-bit mode.
3.2 INSTRUCTIONS (A-L)

The remainder of this chapter provides descriptions of Intel 64 and IA-32 instructions (A-L). See also: Chapter 4, “Instruction Set Reference, M-Z,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B.
AAA—ASCII Adjust After Addition

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>37</td>
<td>AAA</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>ASCII adjust AL after addition.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Adjusts the sum of two unpacked BCD values to create an unpacked BCD result. The AL register is the implied source and destination operand for this instruction. The AAA instruction is only useful when it follows an ADD instruction that adds (binary addition) two unpacked BCD values and stores a byte result in the AL register. The AAA instruction then adjusts the contents of the AL register to contain the correct 1-digit unpacked BCD result.

If the addition produces a decimal carry, the AH register increments by 1, and the CF and AF flags are set. If there was no decimal carry, the CF and AF flags are cleared and the AH register is unchanged. In either case, bits 4 through 7 of the AL register are set to 0.

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

**Operation**

IF 64-Bit Mode
THEN
   #UD;
ELSE
   IF ((AL AND 0FH) > 9) or (AF = 1)
   THEN
      AL ← AL + 6;
      AH ← AH + 1;
      AF ← 1;
      CF ← 1;
      AL ← AL AND 0FH;
   ELSE
      AF ← 0;
      CF ← 0;
      AL ← AL AND 0FH;
   FI;
Flags Affected
The AF and CF flags are set to 1 if the adjustment results in a decimal carry; otherwise they are set to 0. The OF, SF, ZF, and PF flags are undefined.

Protected Mode Exceptions
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as protected mode.

Compatibility Mode Exceptions
Same exceptions as protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
AAD—ASCII Adjust AX Before Division

**Description**

Adjusts two unpacked BCD digits (the least-significant digit in the AL register and the most-significant digit in the AH register) so that a division operation performed on the result will yield a correct unpacked BCD value. The AAD instruction is only useful when it precedes a DIV instruction that divides (binary division) the adjusted value in the AX register by an unpacked BCD value.

The AAD instruction sets the value in the AL register to \((AL + (10 \times AH))\), and then clears the AH register to 00H. The value in the AX register is then equal to the binary equivalent of the original unpacked two-digit (base 10) number in registers AH and AL.

The generalized version of this instruction allows adjustment of two unpacked digits of any number base (see the “Operation” section below), by setting the \(imm8\) byte to the selected number base (for example, 08H for octal, 0AH for decimal, or 0CH for base 12 numbers). The AAD mnemonic is interpreted by all assemblers to mean adjust ASCII (base 10) values. To adjust values in another number base, the instruction must be hand coded in machine code (D5 \(imm8\)).

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

**Operation**

IF 64-Bit Mode
  THEN
    #UD;
  ELSE
    tempAL ← AL;
    tempAH ← AH;
    AL ← (tempAL + (tempAH \times imm8)) AND FFH;
    (* \(imm8\) is set to 0AH for the AAD mnemonic.*)

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D5 0A</td>
<td>AAD</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>ASCII adjust AX before division.</td>
</tr>
<tr>
<td>D5 (ib)</td>
<td>(No mnemonic)</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Adjust AX before division to number base (imm8).</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**
The immediate value \((imm8)\) is taken from the second byte of the instruction.

**Flags Affected**

The SF, ZF, and PF flags are set according to the resulting binary value in the AL register; the OF, AF, and CF flags are undefined.

**Protected Mode Exceptions**

#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as protected mode.

**Compatibility Mode Exceptions**

Same exceptions as protected mode.

**64-Bit Mode Exceptions**

#UD If in 64-bit mode.
AAM—ASCII Adjust AX After Multiply

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D4 0A</td>
<td>AAM</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>ASCII adjust AX after multiply.</td>
</tr>
<tr>
<td>D4 ib</td>
<td>(No mnemonic)</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Adjust AX after multiply to number base imm8.</td>
</tr>
</tbody>
</table>

**Description**

Adjusts the result of the multiplication of two unpacked BCD values to create a pair of unpacked (base 10) BCD values. The AX register is the implied source and destination operand for this instruction. The AAM instruction is only useful when it follows an MUL instruction that multiplies (binary multiplication) two unpacked BCD values and stores a word result in the AX register. The AAM instruction then adjusts the contents of the AX register to contain the correct 2-digit unpacked (base 10) BCD result.

The generalized version of this instruction allows adjustment of the contents of the AX to create two unpacked digits of any number base (see the "Operation" section below). Here, the imm8 byte is set to the selected number base (for example, 08H for octal, 0AH for decimal, or 0CH for base 12 numbers). The AAM mnemonic is interpreted by all assemblers to mean adjust to ASCII (base 10) values. To adjust to values in another number base, the instruction must be hand coded in machine code (D4 imm8).

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

**Operation**

IF 64-Bit Mode
THEN
   #UD;
ELSE
   tempAL ← AL;
   AH ← tempAL / imm8 (* imm8 is set to 0AH for the AAM mnemonic *)
   AL ← tempAL MOD imm8;
Fi;

The immediate value \(imm8\) is taken from the second byte of the instruction.
INSTRUCTION SET REFERENCE, A-L

Flags Affected
The SF, ZF, and PF flags are set according to the resulting binary value in the AL register. The OF, AF, and CF flags are undefined.

Protected Mode Exceptions
#DE If an immediate value of 0 is used.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as protected mode.

Compatibility Mode Exceptions
Same exceptions as protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
**AAS—ASCII Adjust AL After Subtraction**

Adjusts the result of the subtraction of two unpacked BCD values to create a unpacked BCD result. The AL register is the implied source and destination operand for this instruction. The AAS instruction is only useful when it follows a SUB instruction that subtracts (binary subtraction) one unpacked BCD value from another and stores a byte result in the AL register. The AAA instruction then adjusts the contents of the AL register to contain the correct 1-digit unpacked BCD result.

If the subtraction produced a decimal carry, the AH register decrements by 1, and the CF and AF flags are set. If no decimal carry occurred, the CF and AF flags are cleared, and the AH register is unchanged. In either case, the AL register is left with its top four bits set to 0.

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

**Operation**

```
IF 64-bit mode
    THEN
        #UD;
    ELSE
        IF ((AL AND 0FH) > 9) or (AF = 1)
            THEN
                AL ← AL - 6;
                AH ← AH - 1;
                AF ← 1;
                CF ← 1;
                AL ← AL AND 0FH;
            ELSE
                CF ← 0;
                AF ← 0;
                AL ← AL AND 0FH;
```
INSTRUCTION SET REFERENCE, A-L

          Fl;
          Fl;

Flags Affected
The AF and CF flags are set to 1 if there is a decimal borrow; otherwise, they are cleared to 0. The OF, SF, ZF, and PF flags are undefined.

Protected Mode Exceptions
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as protected mode.

Compatibility Mode Exceptions
Same exceptions as protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
## ADC—Add with Carry

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 ib</td>
<td>ADC AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm8 to AL.</td>
</tr>
<tr>
<td>15 iw</td>
<td>ADC AX, imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm16 to AX.</td>
</tr>
<tr>
<td>15 id</td>
<td>ADC EAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm32 to EAX.</td>
</tr>
<tr>
<td>REX.W + 15 id</td>
<td>ADC RAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with carry imm32 sign extended to 64-bits to RAX.</td>
</tr>
<tr>
<td>80 /2 ib</td>
<td>ADC r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm8 to r/m8.</td>
</tr>
<tr>
<td>REX + 80 /2 ib</td>
<td>ADC r/m8,*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with carry imm8 to r/m8.</td>
</tr>
<tr>
<td>81 /2 iw</td>
<td>ADC r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry imm16 to r/m16.</td>
</tr>
<tr>
<td>REX.W + 81 /2 id</td>
<td>ADC r/m64, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with CF imm32 sign extended to 64-bits to r/m64.</td>
</tr>
<tr>
<td>83 /2 ib</td>
<td>ADC r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with CF sign-extended imm8 to r/m16.</td>
</tr>
<tr>
<td>REX.W + 83 /2 ib</td>
<td>ADC r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with CF sign-extended imm8 into r/m64.</td>
</tr>
<tr>
<td>10 /r</td>
<td>ADC r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry byte register to r/m8.</td>
</tr>
<tr>
<td>REX + 10 /r</td>
<td>ADC r/m8*, r8</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with carry byte register to r/m64.</td>
</tr>
<tr>
<td>11 /r</td>
<td>ADC r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry r16 to r/m16.</td>
</tr>
<tr>
<td>REX.W + 11 /r</td>
<td>ADC r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with CF r64 to r/m64.</td>
</tr>
<tr>
<td>12 /r</td>
<td>ADC r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry r/m8 to byte register.</td>
</tr>
<tr>
<td>REX + 12 /r</td>
<td>ADC r8*, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with carry r/m64 to byte register.</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-L

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 ( r )</td>
<td>ADC ( r16, r/m16 )</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with carry ( r/m16 ) to ( r16 ).</td>
</tr>
<tr>
<td>13 ( r )</td>
<td>ADC ( r32, r/m32 )</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Add with CF ( r/m32 ) to ( r32 ).</td>
</tr>
<tr>
<td>REX.W + 13 ( r )</td>
<td>ADC ( r64, r/m64 )</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add with CF ( r/m64 ) to ( r64 ).</td>
</tr>
</tbody>
</table>

NOTES:
*In 64-bit mode, \( r/m8 \) can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Instruction Operand Encoding**

```
<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRMr/m (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRMr/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>I</td>
<td>AL/AX/EAX/RAX</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
```

**Description**

Add the destination operand (first operand), the source operand (second operand), and the carry (CF) flag and stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. (However, two memory operands cannot be used in one instruction.) The state of the CF flag represents a carry from a previous addition. When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The ADC instruction does not distinguish between signed or unsigned operands. Instead, the processor evaluates the result for both data types and sets the OF and CF flags to indicate a carry in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

The ADC instruction is usually executed as part of a multibyte or multiword addition in which an ADD instruction is followed by an ADC instruction.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.
Operation
DEST ← DEST + SRC + CF;

Flags Affected
The OF, SF, ZF, AF, CF, and PF flags are set according to the result.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used but the destination is not a memory operand.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used but the destination is not a memory operand.
### ADD—Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op</th>
<th>64-bit Mode</th>
<th>Compait/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04 ib</td>
<td>ADD AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm8 to AL.</td>
</tr>
<tr>
<td>05 iw</td>
<td>ADD AX, imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm16 to AX.</td>
</tr>
<tr>
<td>05 id</td>
<td>ADD EAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm32 to EAX.</td>
</tr>
<tr>
<td>REX.W + 05 id</td>
<td>ADD RAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add imm32 sign-extended to 64-bits to RAX.</td>
</tr>
<tr>
<td>80 /0 ib</td>
<td>ADD r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm8 to r/m8.</td>
</tr>
<tr>
<td>REX + 80 /0 ib</td>
<td>ADD r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add sign-extended imm8 to r/m64.</td>
</tr>
<tr>
<td>81 /0 iw</td>
<td>ADD r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm16 to r/m16.</td>
</tr>
<tr>
<td>81 /0 id</td>
<td>ADD r/m32, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Add imm32 to r/m32.</td>
</tr>
<tr>
<td>REX.W + 81 /0 id</td>
<td>ADD r/m64, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add imm32 sign-extended to 64-bits to r/m64.</td>
</tr>
<tr>
<td>83 /0 ib</td>
<td>ADD r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Add sign-extended imm8 to r/m16.</td>
</tr>
<tr>
<td>83 /0 ib</td>
<td>ADD r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Add sign-extended imm8 to r/m32.</td>
</tr>
<tr>
<td>REX.W + 83 /0 ib</td>
<td>ADD r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add sign-extended imm8 to r/m64.</td>
</tr>
<tr>
<td>00 /r</td>
<td>ADD r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r8 to r/m8.</td>
</tr>
<tr>
<td>REX + 00 /r</td>
<td>ADD r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add r8 to r/m8.</td>
</tr>
<tr>
<td>01 /r</td>
<td>ADD r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r16 to r/m16.</td>
</tr>
<tr>
<td>01 /r</td>
<td>ADD r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r32 to r/m32.</td>
</tr>
<tr>
<td>REX.W + 01 /r</td>
<td>ADD r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add r64 to r/m64.</td>
</tr>
<tr>
<td>02 /r</td>
<td>ADD r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r/m8 to r8.</td>
</tr>
<tr>
<td>REX + 02 /r</td>
<td>ADD r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add r/m8 to r8.</td>
</tr>
<tr>
<td>03 /r</td>
<td>ADD r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r/m16 to r16.</td>
</tr>
<tr>
<td>03 /r</td>
<td>ADD r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Add r/m32 to r32.</td>
</tr>
<tr>
<td>REX.W + 03 /r</td>
<td>ADD r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Add r/m64 to r64.</td>
</tr>
</tbody>
</table>

### NOTES:

*In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.*
Description

Adds the destination operand (first operand) and the source operand (second operand) and then stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. (However, two memory operands cannot be used in one instruction.) When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The ADD instruction performs integer addition. It evaluates the result for both signed and unsigned integer operands and sets the OF and CF flags to indicate a carry (overflow) in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

\[
\text{DEST} \leftarrow \text{DEST} + \text{SRC};
\]

Flags Affected

The OF, SF, ZF, AF, CF, and PF flags are set according to the result.

Protected Mode Exceptions

#GP(0)  If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
ADD—Add

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.
INSTRUCTION SET REFERENCE, A-L

ADDPD—Add Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 58 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>ADDPD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 58 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed double-precision floating-point values from xmm3/mem to xmm2 and stores result in xmm1.</td>
</tr>
<tr>
<td>VADDPD xmm1,xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 58 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed double-precision floating-point values from xmm3/mem to ymm2 and stores result in ymm1.</td>
</tr>
<tr>
<td>VADDPD ymm1, ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD add of the two packed double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the packed double-precision floating-point results in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified. See Chapter 11 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of SIMD double-precision floating-point operation.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.
Operation

**ADDPD (128-bit Legacy SSE version)**
DEST[63:0] ← DEST[63:0] + SRC[63:0];
DEST[127:64] ← DEST[127:64] + SRC[127:64];
DEST[VLMAX-1:128] (Unmodified)

**VADDPD (VEX.128 encoded version)**
DEST[63:0] ← SRC1[63:0] + SRC2[63:0]
DEST[127:64] ← SRC1[127:64] + SRC2[127:64]
DEST[VLMAX-1:128] ← 0

**VADDPD (VEX.256 encoded version)**
DEST[63:0] ← SRC1[63:0] + SRC2[63:0]
DEST[127:64] ← SRC1[127:64] + SRC2[127:64]

**Intel C/C++ Compiler Intrinsic Equivalent**
ADDPD:  __m128d _mm_add_pd (__m128d a, __m128d b)
VADDPD:  __m256d _mm256_add_pd (__m256d a, __m256d b)

**SIMD Floating-Point Exceptions**
Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**
See Exceptions Type 2.
ADDPS—Add Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 58 /r ADDPS xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Add packed single-precision floating-point values from xmm2/m128 to xmm1 and stores result in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 58 /r VADDPS xmm1,xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Add packed single-precision floating-point values from xmm3/mem to xmm2 and stores result in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 58 /r VADDPS ymm1, ymm2, ymm3/m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Add packed single-precision floating-point values from ymm3/mem to ymm2 and stores result in ymm1.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD add of the four packed single-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the packed single-precision floating-point results in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified. See Chapter 10 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an overview of SIMD single-precision floating-point operation.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.
Operation

**ADDPS (128-bit Legacy SSE version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{DEST}[31:0] + \text{SRC}[31:0]; \\
\text{DEST}[63:32] & \leftarrow \text{DEST}[63:32] + \text{SRC}[63:32]; \\
\text{DEST}[95:64] & \leftarrow \text{DEST}[95:64] + \text{SRC}[95:64]; \\
\text{DEST}[127:96] & \leftarrow \text{DEST}[127:96] + \text{SRC}[127:96]; \\
\text{DEST}[\text{VLMAX}-1:128] & \text{(Unmodified)}
\end{align*}
\]

**VADDPS (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{SRC1}[31:0] + \text{SRC2}[31:0] \\
\text{DEST}[95:64] & \leftarrow \text{SRC1}[95:64] + \text{SRC2}[95:64] \\
\text{DEST}[127:96] & \leftarrow \text{SRC1}[127:96] + \text{SRC2}[127:96] \\
\text{DEST}[\text{VLMAX}-1:128] & \leftarrow 0
\end{align*}
\]

**VADDPS (VEX.256 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{SRC1}[31:0] + \text{SRC2}[31:0] \\
\text{DEST}[63:32] & \leftarrow \text{SRC1}[63:32] + \text{SRC2}[63:32] \\
\text{DEST}[95:64] & \leftarrow \text{SRC1}[95:64] + \text{SRC2}[95:64] \\
\text{DEST}[127:96] & \leftarrow \text{SRC1}[127:96] + \text{SRC2}[127:96] \\
\text{DEST}[159:128] & \leftarrow \text{SRC1}[159:128] + \text{SRC2}[159:128] \\
\text{DEST}[191:160] & \leftarrow \text{SRC1}[191:160] + \text{SRC2}[191:160] \\
\text{DEST}[223:192] & \leftarrow \text{SRC1}[223:192] + \text{SRC2}[223:192] \\
\text{DEST}[255:224] & \leftarrow \text{SRC1}[255:224] + \text{SRC2}[255:224]
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

ADDPS:  `__m128 _mm_add_ps(__m128 a, __m128 b)`
VADDPS: `__m256 _mm256_add_ps (__m256 a, __m256 b)`

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**

See Exceptions Type 2.
ADDSD—Add Scalar Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 58 /r ADDSD xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Add the low double-precision floating-point value from xmm2/m64 to xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F.WIG 58 /r VADDSD xmm1, xmm2, xmm3/m64</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Add the low double-precision floating-point value from xmm3/mem to xmm2 and store the result in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Adds the low double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the double-precision floating-point result in the destination operand.

The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. See Chapter 11 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of a scalar double-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:64) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

**ADDSD (128-bit Legacy SSE version)**

\[
\text{DEST}[63:0] \leftarrow \text{DEST}[63:0] + \text{SRC}[63:0]
\]

\[
\text{DEST}[\text{VLMAX}-1:64] \text{ (Unmodified)}
\]
**VADDSD (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[63:0] & \leftarrow \text{SRC1}[63:0] + \text{SRC2}[63:0] \\
\text{DEST}[127:64] & \leftarrow \text{SRC1}[127:64] \\
\text{DEST}[\text{VLMAX}-1:128] & \leftarrow 0
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

```
ADDSD: __m128d _mm_add_sd (m128d a, m128d b)
```

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**

See Exceptions Type 3.
ADDSS—Add Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 58 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Add the low single-precision floating-point value from xmm2/m32 to xmm1.</td>
</tr>
<tr>
<td>ADDSS xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.WIG 58 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add the low single-precision floating-point value from xmm3/mem to xmm2 and store the result in xmm1.</td>
</tr>
<tr>
<td>VADDSS xmm1,xmm2, xmm3/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Adds the low single-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the single-precision floating-point result in the destination operand.

The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. See Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of a scalar single-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:32) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Operation

ADDSS DEST, SRC (128-bit Legacy SSE version)
DEST[31:0] ← DEST[31:0] + SRC[31:0];
DEST[VLMAX-1:32] (Unmodified)

VADDSS DEST, SRC1, SRC2 (VEX.128 encoded version)
ADDSS—Add Scalar Single-Precision Floating-Point Values

DEST[31:0] ← SRC1[31:0] + SRC2[31:0]
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**
ADDSS: __m128 _mm_add_ss(__m128 a, __m128 b)

**SIMD Floating-Point Exceptions**
Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**
See Exceptions Type 3.
ADDSUBPD—Packed Double-FP Add/Subtract

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F D0 /r ADDSUBPD xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE3</td>
<td>Add/subtract double-precision floating-point values from xmm2/m128 to xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG D0 /r VADDSUBPD xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Add/subtract packed double-precision floating-point values from xmm3/mem to xmm2 and stores result in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG D0 /r VADDSUBPD ymm1, ymm2, ymm3/m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Add/subtract packed double-precision floating-point values from ymm3/mem to ymm2 and stores result in ymm1.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX:vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

 Adds odd-numbered double-precision floating-point values of the first source operand (second operand) with the corresponding double-precision floating-point values from the second source operand (third operand); stores the result in the odd-numbered values of the destination operand (first operand). Subtracts the even-numbered double-precision floating-point values from the second source operand from the corresponding double-precision floating values in the first source operand; stores the result into the even-numbered values of the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified. See Figure 3-3.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Figure 3-3. ADDSUBPD—Packed Double-FP Add/Subtract**

**Operation**

**ADDSUBPD (128-bit Legacy SSE version)**
DEST[63:0] ← DEST[63:0] - SRC[63:0]
DEST[127:64] ← DEST[127:64] + SRC[127:64]
DEST[VLMAX-1:128] (Unmodified)

**VADDSUBPD (VEX.128 encoded version)**
DEST[63:0] ← SRC1[63:0] - SRC2[63:0]
DEST[127:64] ← SRC1[127:64] + SRC2[127:64]
DEST[VLMAX-1:128] ← 0

**VADDSUBPD (VEX.256 encoded version)**
DEST[63:0] ← SRC1[63:0] - SRC2[63:0]
DEST[127:64] ← SRC1[127:64] + SRC2[127:64]
**Intel C/C++ Compiler Intrinsic Equivalent**

ADDSUBPD: __m128d _mm_addsub_pd(__m128d a, __m128d b)

VADDSUBPD: __m256d _mm256_addsub_pd (__m256d a, __m256d b)

**Exceptions**

When the source operand is a memory operand, it must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**

See Exceptions Type 2.
ADDSUBPS—Packed Single-FP Add/Subtract

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F D0 /r ADDSUBPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE3</td>
<td>Add/subtract single-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.F2.0F:WIG D0 /r VADDSUBPS xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add/subtract single-precision floating-point values from xmm3/mem to xmm2 and stores result in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.256.F2.0F:WIG D0 /r VADDSUBPS ymm1, ymm2, ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add/subtract single-precision floating-point values from ymm3/mem to ymm2 and stores result in ymm1.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Adds odd-numbered single-precision floating-point values of the first source operand (second operand) with the corresponding single-precision floating-point values from the second source operand (third operand); stores the result in the odd-numbered values of the destination operand (first operand). Subtracts the even-numbered single-precision floating-point values from the second source operand from the corresponding single-precision floating values in the first source operand; stores the result into the even-numbered values of the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified. See Figure 3-4.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**ADDSUBPS (128-bit Legacy SSE version)**
- \( \text{DEST}[31:0] \leftarrow \text{DEST}[31:0] - \text{SRC}[31:0] \)
- \( \text{DEST}[95:64] \leftarrow \text{DEST}[95:64] - \text{SRC}[95:64] \)
- \( \text{DEST}[127:96] \leftarrow \text{DEST}[127:96] + \text{SRC}[127:96] \)
- \( \text{DEST}[\text{VLMAX}-1:128] \) (Unmodified)

**VADDSUBPS (VEX.128 encoded version)**
- \( \text{DEST}[31:0] \leftarrow \text{SRC1}[31:0] - \text{SRC2}[31:0] \)
- \( \text{DEST}[95:64] \leftarrow \text{SRC1}[95:64] - \text{SRC2}[95:64] \)
- \( \text{DEST}[127:96] \leftarrow \text{SRC1}[127:96] + \text{SRC2}[127:96] \)
- \( \text{DEST}[\text{VLMAX}-1:128] \leftarrow 0 \)

**VADDSUBPS (VEX.256 encoded version)**
- \( \text{DEST}[31:0] \leftarrow \text{SRC1}[31:0] - \text{SRC2}[31:0] \)
- \( \text{DEST}[63:32] \leftarrow \text{SRC1}[63:32] + \text{SRC2}[63:32] \)
- \( \text{DEST}[95:64] \leftarrow \text{SRC1}[95:64] - \text{SRC2}[95:64] \)
ADDSUBPS—Packed Single-FP Add/Subtract

\[ \text{DEST}[127:96] \leftarrow \text{SRC1}[127:96] + \text{SRC2}[127:96] \]
\[ \text{DEST}[159:128] \leftarrow \text{SRC1}[159:128] - \text{SRC2}[159:128] \]
\[ \text{DEST}[191:160] \leftarrow \text{SRC1}[191:160] + \text{SRC2}[191:160] \]
\[ \text{DEST}[223:192] \leftarrow \text{SRC1}[223:192] - \text{SRC2}[223:192] \]
\[ \text{DEST}[255:224] \leftarrow \text{SRC1}[255:224] + \text{SRC2}[255:224] \]

**Intel C/C++ Compiler Intrinsic Equivalent**

ADDSUBPS: \text{__m128 } \text{_mm_addsub_ps(__m128 a, __m128 b)}

VADDSUBPS: \text{__m256 } \text{_mm256_addsub_ps(__m256 a, __m256 b)}

**Exceptions**

When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**

See Exceptions Type 2.
AESDEC—Perform One Round of an AES Decryption Flow

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 DE /r AESDEC xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>AES</td>
<td>Perform one round of an AES decryption flow, using the Equivalent Inverse Cipher, operating on a 128-bit data (state) from xmm1 with a 128-bit round key from xmm2/m128.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG DE /r VAESDEC xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>Both AES and AVX flags</td>
<td>Perform one round of an AES decryption flow, using the Equivalent Inverse Cipher, operating on a 128-bit data (state) from xmm2 with a 128-bit round key from xmm3/m128; store the result in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand2</th>
<th>Operand3</th>
<th>Operand4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

This instruction performs a single round of the AES decryption flow using the Equivalent Inverse Cipher, with the round key from the second source operand, operating on a 128-bit data (state) from the first source operand, and store the result in the destination operand.

Use the AESDEC instruction for all but the last decryption round. For the last decryption round, use the AESDECCLAST instruction.

128-bit Legacy SSE version: The first source operand and the destination operand are the same and must be an XMM register. The second source operand can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: The first source operand and the destination operand are XMM registers. The second source operand can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the destination YMM register are zeroed.
**AESDEC—Perform One Round of an AES Decryption Flow**

**Operation**

**AESDEC**

STATE ← SRC1;
RoundKey ← SRC2;
STATE ← InvShiftRows( STATE );
STATE ← InvSubBytes( STATE );
STATE ← InvMixColumns( STATE );
DEST[127:0] ← STATE XOR RoundKey;
DEST[VLMAX-1:128] (Unmodified)

**VAESDEC**

STATE ← SRC1;
RoundKey ← SRC2;
STATE ← InvShiftRows( STATE );
STATE ← InvSubBytes( STATE );
STATE ← InvMixColumns( STATE );
DEST[127:0] ← STATE XOR RoundKey;
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

(V)AESDEC: __m128i _mm_aesdec (__m128i, __m128i)

**SIMD Floating-Point Exceptions**

None

**Other Exceptions**

See Exceptions Type 4.
AESDECLAST—Perform Last Round of an AES Decryption Flow

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 DF /r</td>
<td>AESDECLAST xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>AES</td>
<td>Perform the last round of an AES decryption flow, using the Equivalent Inverse Cipher, operating on a 128-bit data (state) from xmm1 with a 128-bit round key from xmm2/m128.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG DF /r</td>
<td>VAESDECLAST xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>Both AES and AVX flags</td>
<td>Perform the last round of an AES decryption flow, using the Equivalent Inverse Cipher, operating on a 128-bit data (state) from xmm2 with a 128-bit round key from xmm3/m128; store the result in xmm1.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand2</th>
<th>Operand3</th>
<th>Operand4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

This instruction performs the last round of the AES decryption flow using the Equivalent Inverse Cipher, with the round key from the second source operand, operating on a 128-bit data (state) from the first source operand, and store the result in the destination operand.

128-bit Legacy SSE version: The first source operand and the destination operand are the same and must be an XMM register. The second source operand can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: The first source operand and the destination operand are XMM registers. The second source operand can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

AESDECLAST
AESDECLAST—Perform Last Round of an AES Decryption Flow

STATE ← SRC1;
RoundKey ← SRC2;
STATE ← InvShiftRows( STATE );
STATE ← InvSubBytes( STATE );
DEST[127:0] ← STATE XOR RoundKey;
DEST[VLMAX-1:128] (Unmodified)

VAESDECLAST
STATE ← SRC1;
RoundKey ← SRC2;
STATE ← InvShiftRows( STATE );
STATE ← InvSubBytes( STATE );
DEST[127:0] ← STATE XOR RoundKey;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
(V)AESDECLAST: __m128i _mm_aesdeclast (__m128i, __m128i)

SIMD Floating-Point Exceptions
None

Other Exceptions
See Exceptions Type 4.
AESENC—Perform One Round of an AES Encryption Flow

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 DC /r</td>
<td>AESENC xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>AES</td>
<td>Perform one round of an AES encryption flow, operating on a 128-bit data (state) from xmm1 with a 128-bit round key from xmm2/m128.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG DC /r</td>
<td>VAESNC xmm1, xmm2, xmm3/m128</td>
<td>V/RM</td>
<td>V/V</td>
<td>Both AES and AVX flags</td>
<td>Perform one round of an AES encryption flow, operating on a 128-bit data (state) from xmm2 with a 128-bit round key from the xmm3/m128; store the result in xmm1.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand2</th>
<th>Operand3</th>
<th>Operand4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

This instruction performs a single round of an AES encryption flow using a round key from the second source operand, operating on 128-bit data (state) from the first source operand, and store the result in the destination operand.

Use the AESENC instruction for all but the last encryption rounds. For the last encryption round, use the AESENCCLAST instruction.

128-bit Legacy SSE version: The first source operand and the destination operand are the same and must be an XMM register. The second source operand can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: The first source operand and the destination operand are XMM registers. The second source operand can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

AESENC
STATE ← SRC1;
RoundKey ← SRC2;
STATE ← ShiftRows(STATE);
STATE ← SubBytes(STATE);
STATE ← MixColumns(STATE);
DEST[127:0] ← STATE XOR RoundKey;
DEST[VLMAX-1:128] (Unmodified)

**VAESENC**
STATE ← SRC1;
RoundKey ← SRC2;
STATE ← ShiftRows(STATE);
STATE ← SubBytes(STATE);
STATE ← MixColumns(STATE);
DEST[127:0] ← STATE XOR RoundKey;
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**
(V)VAESENC: __m128i _mm_aesenc (__m128i, __m128i)

**SIMD Floating-Point Exceptions**
None

**Other Exceptions**
See Exceptions Type 4.
### AESENCLAST—Perform Last Round of an AES Encryption Flow

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 DD /r AESENCLAST xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>AES</td>
<td>Perform the last round of an AES encryption flow, operating on a 128-bit data (state) from xmm1 with a 128-bit round key from xmm2/m128.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG DD /r VAESENCLAST xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>Both AES and AVX flags</td>
<td>Perform the last round of an AES encryption flow, operating on a 128-bit data (state) from xmm2 with a 128 bit round key from xmm3/m128; store the result in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand2</th>
<th>Operand3</th>
<th>Operand4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMrm/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMrm/r (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

This instruction performs the last round of an AES encryption flow using a round key from the second source operand, operating on 128-bit data (state) from the first source operand, and store the result in the destination operand.

128-bit Legacy SSE version: The first source operand and the destination operand are the same and must be an XMM register. The second source operand can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: The first source operand and the destination operand are XMM registers. The second source operand can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

### Operation

**AESENCLAST**

\[
\text{STATE} \leftarrow \text{SRC1}; \\
\text{RoundKey} \leftarrow \text{SRC2};
\]
STATE ← ShiftRows( STATE );
STATE ← SubBytes( STATE );
DEST[127:0] ← STATE XOR RoundKey;
DEST[VLMAX-1:128] (Unmodified)

VAESENCLAST
STATE ← SRC1;
RoundKey ← SRC2;
STATE ← ShiftRows( STATE );
STATE ← SubBytes( STATE );
DEST[127:0] ← STATE XOR RoundKey;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
(V)AESENCLAST: __m128i _mm_aesenclast (__m128i, __m128i)

SIMD Floating-Point Exceptions
None

Other Exceptions
See Exceptions Type 4.
AESIMC—Perform the AES InvMixColumn Transformation

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 DB /r AESIMC xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>AES</td>
<td>Perform the InvMixColumn transformation on a 128-bit round key from xmm2/m128 and store the result in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG DB /r VAESIMC xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>Both AES and AVX flags</td>
<td>Perform the InvMixColumn transformation on a 128-bit round key from xmm2/m128 and store the result in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Perform the InvMixColumns transformation on the source operand and store the result in the destination operand. The destination operand is an XMM register. The source operand can be an XMM register or a 128-bit memory location.

Note: the AESIMC instruction should be applied to the expanded AES round keys (except for the first and last round key) in order to prepare them for decryption using the “Equivalent Inverse Cipher” (defined in FIPS 197).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

Operation

AESIMC
DEST[127:0] ← InvMixColumns( SRC );
DEST[VLMAX-1:128] (Unmodified)

VAESIMC
DEST[127:0] ← InvMixColumns( SRC );
AESIMC—Perform the AES InvMixColumn Transformation

DEST[VLMAX-1:128] ← 0;

**Intel C/C++ Compiler Intrinsic Equivalent**

(V)AESIMC: __m128i _mm_aesimc(__m128i)

**SIMD Floating-Point Exceptions**

None

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.vvvv != 1111B.
AESKEYGENASSIST—AES Round Key Generation Assist

<table>
<thead>
<tr>
<th>Opcode/</th>
<th>Op/</th>
<th>64/32-bit</th>
<th>CPUID</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction</td>
<td>En</td>
<td>Mode</td>
<td>Feature Flag</td>
<td></td>
</tr>
<tr>
<td>66 0F 3A DF /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AES</td>
<td>Assist in AES round key generation using an 8 bits Round Constant (RCON) specified in the immediate byte, operating on 128 bits of data specified in xmm2/m128 and stores the result in xmm1.</td>
</tr>
<tr>
<td>VEX.128.66.0F3A.WIG DF /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>Both AES and AVX flags</td>
<td>Assist in AES round key generation using 8 bits Round Constant (RCON) specified in the immediate byte, operating on 128 bits of data specified in xmm2/m128 and stores the result in xmm1.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand2</th>
<th>Operand3</th>
<th>Operand4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Assist in expanding the AES cipher key, by computing steps towards generating a round key for encryption, using 128-bit data specified in the source operand and an 8-bit round constant specified as an immediate, store the result in the destination operand.

The destination operand is an XMM register. The source operand can be an XMM register or a 128-bit memory location.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

Operation

AESKEYGENASSIST
X3[31:0] ← SRC [127: 96];
X2[31:0] ← SRC [95: 64];
X1[31:0] ← SRC [63: 32];
X0[31:0] ← SRC [31: 0];
RCON[31:0] ← ZeroExtend(Imm8[7:0]);
DEST[31:0] ← SubWord(X1);
DEST[63:32 ] ← RotWord( SubWord(X1) ) XOR RCON;
DEST[95:64] ← SubWord(X3);
DEST[127:96] ← RotWord( SubWord(X3) ) XOR RCON;
DEST[VLMAX-1:128] (Unmodified)

VAESKEYGENASSIST
X3[31:0] ← SRC [127: 96];
X2[31:0] ← SRC [95: 64];
X1[31:0] ← SRC [63: 32];
X0[31:0] ← SRC [31: 0];
RCON[31:0] ← ZeroExtend(Imm8[7:0]);
DEST[31:0] ← SubWord(X1);
DEST[63:32 ] ← RotWord( SubWord(X1) ) XOR RCON;
DEST[95:64] ← SubWord(X3);
DEST[127:96] ← RotWord( SubWord(X3) ) XOR RCON;
DEST[VLMAX-1:128] ← 0;

Intel C/C++ Compiler Intrinsic Equivalent
(V)AESKEYGENASSIST: __m128i _mm_aesimc (__m128i, const int)

SIMD Floating-Point Exceptions
None

Other Exceptions
See Exceptions Type 4; additionally
  #UD If VEX.vvvv != 1111B.
### AND—Logical AND

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24 ib</td>
<td>AND AL, imm8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>AL AND imm8.</td>
</tr>
<tr>
<td>25 iw</td>
<td>AND AX, imm16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>AX AND imm16.</td>
</tr>
<tr>
<td>25 id</td>
<td>AND EAX, imm32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>EAX AND imm32.</td>
</tr>
<tr>
<td>REX.W + 25 id</td>
<td>AND RAX, imm32</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>RAX AND imm32 sign-extended to 64-bits.</td>
</tr>
<tr>
<td>80 /4 ib</td>
<td>AND r/m8, imm8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m8 AND imm8.</td>
</tr>
<tr>
<td>REX + 80 /4 ib</td>
<td>AND r/m8, imm8</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m8 AND imm8.</td>
</tr>
<tr>
<td>81 /4 iw</td>
<td>AND r/m16, imm16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 AND imm16.</td>
</tr>
<tr>
<td>81 /4 id</td>
<td>AND r/m32, imm16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 AND imm32.</td>
</tr>
<tr>
<td>REX.W + 81 /4 id</td>
<td>AND r/m64, imm32</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND imm32 sign extended to 64-bits.</td>
</tr>
<tr>
<td>83 /4 ib</td>
<td>AND r/m16, imm8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 AND imm8 (sign-extended).</td>
</tr>
<tr>
<td>83 /4 ib</td>
<td>AND r/m32, imm8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 AND imm8 (sign-extended).</td>
</tr>
<tr>
<td>REX.W + 83 /4 ib</td>
<td>AND r/m64, imm8</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND imm8 (sign-extended).</td>
</tr>
<tr>
<td>20 /r</td>
<td>AND r/m8, r8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m8 AND r8.</td>
</tr>
<tr>
<td>REX + 20 /r</td>
<td>AND r/m8, r8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m8 AND r8 (sign-extended).</td>
</tr>
<tr>
<td>21 /r</td>
<td>AND r/m16, r16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 AND r16.</td>
</tr>
<tr>
<td>21 /r</td>
<td>AND r/m32, r32</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 AND r32.</td>
</tr>
<tr>
<td>REX.W + 21 /r</td>
<td>AND r/m64, r64</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 AND r32.</td>
</tr>
<tr>
<td>22 /r</td>
<td>AND r8, r/m8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>r8 AND r/m8.</td>
</tr>
<tr>
<td>REX + 22 /r</td>
<td>AND r8, r/m8</td>
<td>I</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m8 AND r/m8 (sign-extended).</td>
</tr>
<tr>
<td>23 /r</td>
<td>AND r16, r/m16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>r16 AND r/m16.</td>
</tr>
<tr>
<td>23 /r</td>
<td>AND r32, r/m32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>r32 AND r/m32.</td>
</tr>
<tr>
<td>REX.W + 23 /r</td>
<td>AND r64, r/m64</td>
<td>I</td>
<td>Valid</td>
<td>N.E.</td>
<td>r64 AND r/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**

*In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.*

---

3-64 Vol. 2A AND—Logical AND
Description
Performs a bitwise AND operation on the destination (first) and source (second) operands and stores the result in the destination operand location. The source operand can be an immediate, a register, or a memory location; the destination operand can be a register or a memory location. (However, two memory operands cannot be used in one instruction.) Each bit of the result is set to 1 if both corresponding bits of the first and second operands are 1; otherwise, it is set to 0.
This instruction can be used with a LOCK prefix to allow the it to be executed atomically.
In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation
DEST ← DEST AND SRC;

Flags Affected
The OF and CF flags are cleared; the SF, ZF, and PF flags are set according to the result. The state of the AF flag is undefined.

Protected Mode Exceptions
#GP(0) If the destination operand points to a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
ANDPD—Bitwise Logical AND of Packed Double-Precision Floating-Point Values

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 54 /r ANDPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Return the bitwise logical AND of packed double-precision floating-point values in xmm1 and xmm2/m128.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 54 /r VANDPD xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical AND of packed double-precision floating-point values in xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 54 /r VANDPD ymm1, ymm2, ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical AND of packed double-precision floating-point values in ymm2 and ymm3/mem.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical AND of the two packed double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the result in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**ANDPD (128-bit Legacy SSE version)**  
DEST[63:0] ← DEST[63:0] BITWISE AND SRC[63:0]  
DEST[VLMAX-1:128] (Unmodified)

**VANDPD (VEX.128 encoded version)**  
DEST[63:0] ← SRC1[63:0] BITWISE AND SRC2[63:0]  
DEST[VLMAX-1:128] ← 0

**VANDPD (VEX.256 encoded version)**  
DEST[63:0] ← SRC1[63:0] BITWISE AND SRC2[63:0]  

**Intel C/C++ Compiler Intrinsic Equivalent**  
ANDPD: __m128d _mm_and_pd(__m128d a, __m128d b)  
VANDPD: __m256d _mm256_and_pd (__m256d a, __m256d b)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4.
### ANDPS—Bitwise Logical AND of Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 54 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Bitwise logical AND of xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>ANDPS xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 54 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical AND of packed single-precision floating-point values in xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VANDPS xmm1,xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 54 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical AND of packed single-precision floating-point values in ymm2 and ymm3/mem.</td>
</tr>
<tr>
<td>VANDPS ymm1, ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Description

Performs a bitwise logical AND of the four or eight packed single-precision floating-point values from the first source operand and the second source operand, and stores the result in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.
INSTRUCTION SET REFERENCE, A-L

Operation

ANDPS (128-bit Legacy SSE version)
DEST[31:0] ← DEST[31:0] BITWISE AND SRC[31:0]
DEST[95:64] ← DEST[95:64] BITWISE AND SRC[95:64]
DEST[VLMAX-1:128] (Unmodified)

VANDPS (VEX.128 encoded version)
DEST[31:0] ← SRC1[31:0] BITWISE AND SRC2[31:0]
DEST[95:64] ← SRC1[95:64] BITWISE AND SRC2[95:64]
DEST[VLMAX-1:128] ← 0

VANDPS (VEX.256 encoded version)
DEST[31:0] ← SRC1[31:0] BITWISE AND SRC2[31:0]
DEST[95:64] ← SRC1[95:64] BITWISE AND SRC2[95:64]

Intel C/C++ Compiler Intrinsic Equivalent
ANDPS: __m128 _mm_and_ps(__m128 a, __m128 b)
VANDPS: __m256 _mm256_and_ps (__m256 a, __m256 b)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4.
ANDNPD—Bitwise Logical AND NOT of Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 55 /r ANDNPD xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Bitwise logical AND NOT of xmm2/m128 and xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 55 /r VANDNPD xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Return the bitwise logical AND NOT of packed double-precision floating-point values in xmm2 and xmm3/mem.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 55/r VANDNPD ymm1, ymm2, ymm3/m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Return the bitwise logical AND NOT of packed double-precision floating-point values in ymm2 and ymm3/mem.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a bitwise logical AND NOT of the two or four packed double-precision floating-point values from the first source operand and the second source operand, and stores the result in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VMLAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VMLAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.
**Operation**

**ANDNPD (128-bit Legacy SSE version)**

DEST[63:0] ← (NOT(DEST[63:0])) BITWISE AND SRC[63:0]
DEST[127:64] ← (NOT(DEST[127:64])) BITWISE AND SRC[127:64]
DEST[VLMAX-1:128] (Unmodified)

**VANDNPD (VEX.128 encoded version)**

DEST[63:0] ← (NOT(SRC1[63:0])) BITWISE AND SRC2[63:0]
DEST[127:64] ← (NOT(SRC1[127:64])) BITWISE AND SRC2[127:64]

**VANDNPD (VEX.256 encoded version)**

DEST[63:0] ← (NOT(SRC1[63:0])) BITWISE AND SRC2[63:0]
DEST[127:64] ← (NOT(SRC1[127:64])) BITWISE AND SRC2[127:64]
DEST[255:192] ← (NOT(SRC1[255:192])) BITWISE AND SRC2[255:192]

**Intel C/C++ Compiler Intrinsic Equivalent**

ANDNPD: __m128d _mm_andnot_pd(__m128d a, __m128d b)
VANDNPD: __m256d _mm256_andnot_pd (__m256d a, __m256d b)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4.
**ANDNPS—Bitwise Logical AND NOT of Packed Single-Precision Floating-Point Values**

### Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 55 /r ANDNPS xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Bitwise logical AND NOT of xmm2/m128 and xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 55 /r VANDNPS xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Return the bitwise logical AND NOT of packed single-precision floating-point values in xmm2 and xmm3/mem.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 55 /r VANDNPS ymm1, ymm2, ymm3/m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Return the bitwise logical AND NOT of packed single-precision floating-point values in ymm2 and ymm3/mem.</td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (w)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (w)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Inverts the bits of the four packed single-precision floating-point values in the destination operand (first operand), performs a bitwise logical AND of the four packed single-precision floating-point values in the source operand (second operand) and the temporary inverted result, and stores the result in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.
Operation

**ANDNPS (128-bit Legacy SSE version)**

DEST[31:0] ← (NOT(DEST[31:0])) BITWISE AND SRC[31:0]
DEST[95:64] ← (NOT(DEST[95:64])) BITWISE AND SRC[95:64]
DEST[127:96] ← (NOT(DEST[127:96])) BITWISE AND SRC[127:96]
DEST[VLMAX-1:128] (Unmodified)

**VANDNPS (VEX.128 encoded version)**

DEST[31:0] ← (NOT(SRC1[31:0])) BITWISE AND SRC2[31:0]
DEST[95:64] ← (NOT(SRC1[95:64])) BITWISE AND SRC2[95:64]
DEST[127:96] ← (NOT(SRC1[127:96])) BITWISE AND SRC2[127:96]
DEST[VLMAX-1:128] ← 0

**VANDNPS (VEX.256 encoded version)**

DEST[31:0] ← (NOT(SRC1[31:0])) BITWISE AND SRC2[31:0]
DEST[95:64] ← (NOT(SRC1[95:64])) BITWISE AND SRC2[95:64]
DEST[127:96] ← (NOT(SRC1[127:96])) BITWISE AND SRC2[127:96]
DEST[159:128] ← (NOT(SRC1[159:128])) BITWISE AND SRC2[159:128]

**Intel C/C++ Compiler Intrinsic Equivalent**

ANDNPS: __m128 _mm_andnot_ps(__m128 a, __m128 b)
VANDNPS: __m256 _mm256_andnot_ps (__m256 a, __m256 b)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4.
ARPL—Adjust RPL Field of Segment Selector

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 /r</td>
<td>ARPL r/m16, r16</td>
<td>NP</td>
<td>N. E.</td>
<td>Valid</td>
<td>Adjust RPL of r/m16 to not less than RPL of r16.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>ModRMr/m (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Compares the RPL fields of two segment selectors. The first operand (the destination operand) contains one segment selector and the second operand (source operand) contains the other. (The RPL field is located in bits 0 and 1 of each operand.) If the RPL field of the destination operand is less than the RPL field of the source operand, the ZF flag is set and the RPL field of the destination operand is increased to match that of the source operand. Otherwise, the ZF flag is cleared and no change is made to the destination operand. (The destination operand can be a word register or a memory location; the source operand must be a word register.)

The ARPL instruction is provided for use by operating-system procedures (however, it can also be used by applications). It is generally used to adjust the RPL of a segment selector that has been passed to the operating system by an application program to match the privilege level of the application program. Here the segment selector passed to the operating system is placed in the destination operand and segment selector for the application program’s code segment is placed in the source operand. (The RPL field in the source operand represents the privilege level of the application program.) Execution of the ARPL instruction then ensures that the RPL of the segment selector received by the operating system is no lower (does not have a higher privilege) than the privilege level of the application program (the segment selector for the application program’s code segment can be read from the stack following a procedure call).

This instruction executes as described in compatibility mode and legacy mode. It is not encodable in 64-bit mode.

INSTRUCTION SET REFERENCE, A-L

Operation
IF 64-BIT MODE
THEN
See MOVSXD;
ELSE
IF DEST[RPL) < SRC[RPL)
THEN
ZF ← 1;
DEST(RPL) ← SRC(RPL); 
ELSE
ZF ← 0;
FI;
FI;

Flags Affected
The ZF flag is set to 1 if the RPL field of the destination operand is less than that of the source operand; otherwise, it is set to 0.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD The ARPL instruction is not recognized in real-address mode.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#UD The ARPL instruction is not recognized in virtual-8086 mode.
If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Not applicable.
BLENDPD — Blend Packed Double Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 0D /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Select packed DP-FP values from xmm1 and xmm2/m128 from mask specified in imm8 and store the values into xmm1.</td>
</tr>
</tbody>
</table>

VEX.NDS.128.66.0F3A.WIG 0D /r ib
VBLENDPD xmm1, xmm2, xmm3/m128, imm8

VEX.NDS.256.66.0F3A.WIG 0D /r ib
VBLENDPD ymm1, ymm2, ymm3/m256, imm8

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8[3:0]</td>
</tr>
</tbody>
</table>

Description

Double-precision floating-point values from the second source operand (third operand) are conditionally merged with values from the first source operand (second operand) and written to the destination operand (first operand). The immediate bits [3:0] determine whether the corresponding double-precision floating-point value in the destination is copied from the second source or first source. If a bit in the mask, corresponding to a word, is "1", then the double-precision floating-point value in the second source operand is copied, else the value in the first source operand is copied.

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register. The second source operand is an XMM register or 128-bit memory location. The destination
operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**BLENDPD (128-bit Legacy SSE version)**

IF (IMM8[0] = 0) THEN DEST[63:0]  DEST[63:0]
ELSE DEST [63:0]  SRC[63:0] FI

IF (IMM8[1] = 0) THEN DEST[127:64]  DEST[127:64]
ELSE DEST [127:64]  SRC[127:64] FI

DEST[VLMAX-1:128] (Unmodified)

**VBLENDPD (VEX.128 encoded version)**

IF (IMM8[0] = 0) THEN DEST[63:0]  SRC1[63:0]
ELSE DEST [63:0]  SRC2[63:0] FI

IF (IMM8[1] = 0) THEN DEST[127:64]  SRC1[127:64]
ELSE DEST [127:64]  SRC2[127:64] FI

DEST[VLMAX-1:128]  0

**VBLENDPD (VEX.256 encoded version)**

IF (IMM8[0] = 0) THEN DEST[63:0]  SRC1[63:0]
ELSE DEST [63:0]  SRC2[63:0] FI

IF (IMM8[1] = 0) THEN DEST[127:64]  SRC1[127:64]
ELSE DEST [127:64]  SRC2[127:64] FI


**Intel C/C++ Compiler Intrinsic Equivalent**

BLENDPD: __m128d _mm_blend_pd (__m128d v1, __m128d v2, const int mask);

VBLENDPD: __m256d _mm256_blend_pd (__m256d a, __m256d b, const int mask);

**SIMD Floating-Point Exceptions**

None

**Other Exceptions**

See Exceptions Type 4.
### BLENDPS — Blend Packed Single Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 0C /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Select packed single precision floating-point values from xmm1 and xmm2/m128 from mask specified in imm8 and store the values into xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.WIG 0C /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Select packed single-precision floating-point values from xmm2 and xmm3/m128 from mask in imm8 and store the values in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F3A.WIG 0C /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Select packed single-precision floating-point values from ymm2 and ymm3/m256 from mask in imm8 and store the values in ymm1.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

### Description

Packed single-precision floating-point values from the second source operand (third operand) are conditionally merged with values from the first source operand (second operand) and written to the destination operand (first operand). The immediate bits [7:0] determine whether the corresponding single precision floating-point value in the destination is copied from the second source or first source. If a bit in the mask, corresponding to a word, is “1”, then the single-precision floating-point value in the second source operand is copied, else the value in the first source operand is copied.

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: The first source operand an XMM register. The second source operand is an XMM register or 128-bit memory location. The destination
operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Operation

**BLENDPS (128-bit Legacy SSE version)**

IF (IMM8[0] = 0) THEN DEST[31:0] ← DEST[31:0]
ELSE DEST[31:0] ← SRC[31:0] FI
IF (IMM8[2] = 0) THEN DEST[95:64] ← DEST[95:64]
ELSE DEST[95:64] ← SRC[95:64] FI
DEST[VLMAX-1:128] (Unmodified)

**VBLENDPS (VEX.128 encoded version)**

IF (IMM8[0] = 0) THEN DEST[31:0] ← SRC1[31:0]
ELSE DEST[31:0] ← SRC2[31:0] FI
IF (IMM8[2] = 0) THEN DEST[95:64] ← SRC1[95:64]
ELSE DEST[95:64] ← SRC2[95:64] FI
DEST[VLMAX-1:128] ← 0

**VBLENDPS (VEX.256 encoded version)**

IF (IMM8[0] = 0) THEN DEST[31:0] ← SRC1[31:0]
ELSE DEST[31:0] ← SRC2[31:0] FI
IF (IMM8[2] = 0) THEN DEST[95:64] ← SRC1[95:64]
ELSE DEST[95:64] ← SRC2[95:64] FI
INSTRUCTION SET REFERENCE, A-L


Intel C/C++ Compiler Intrinsic Equivalent
BLENDPS: __m128 _mm_blend_ps (__m128 v1, __m128 v2, const int mask);
VBLENDPS: __m256 _mm256_blend_ps (__m256 a, __m256 b, const int mask);

SIMD Floating-Point Exceptions
None

Other Exceptions
See Exceptions Type 4.
BLENDVPD — Variable Blend Packed Double Precision Floating-Point Values

### Opcode/Instruction

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<th>CPUID Feature Flag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 15 /r</td>
<td>RM0</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Select packed DP FP values from xmm1 and xmm2 from mask specified in XMM0 and store the values in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.W0 4B /is4</td>
<td>RVRM</td>
<td>V/V</td>
<td>AVX</td>
<td>Conditionally copy double-precision floating-point values from xmm2 or xmm3/m128 to xmm1, based on mask bits in the mask operand, xmm4.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F3A.W0 4B /is4</td>
<td>RVRM</td>
<td>V/V</td>
<td>AVX</td>
<td>Conditionally copy double-precision floating-point values from ymm2 or ymm3/m256 to ymm1, based on mask bits in the mask operand, ymm4.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

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<tr>
<td>RM0</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:reg (r)</td>
<td>implicit XMM0</td>
<td>NA</td>
</tr>
<tr>
<td>RVRM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:reg (r)</td>
<td>imm8[7:4]</td>
</tr>
</tbody>
</table>

### Description

Conditionally copy each quadword data element of double-precision floating-point value from the second source operand and the first source operand depending on mask bits defined in the mask register operand. The mask bits are the most significant bit in each quadword element of the mask register.

Each quadword element of the destination operand is copied from:

- the corresponding quadword element in the second source operand, If a mask bit is “1”; or
- the corresponding quadword element in the first source operand, If a mask bit is “0”

The register assignment of the implicit mask operand for BLENDVPD is defined to be the architectural register XMM0.
128-bit Legacy SSE version: The first source operand and the destination operand is the same. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged. The mask register operand is implicitly defined to be the architectural register XMM0. An attempt to execute BLENDVPD with a VEX prefix will cause #UD.

VEX.128 encoded version: The first source operand and the destination operand are XMM registers. The second source operand is an XMM register or 128-bit memory location. The mask operand is the third source register, and encoded in bits[7:4] of the immediate byte(imm8). The bits[3:0] of imm8 are ignored. In 32-bit mode, imm8[7] is ignored. The upper bits (VLMAX-1:128) of the corresponding YMM register (destination register) are zeroed. VEX.W must be 0, otherwise, the instruction will #UD.

VEX.256 encoded version: The first source operand and destination operand are YMM registers. The second source operand can be a YMM register or a 256-bit memory location. The mask operand is the third source register, and encoded in bits[7:4] of the immediate byte(imm8). The bits[3:0] of imm8 are ignored. In 32-bit mode, imm8[7] is ignored. VEX.W must be 0, otherwise, the instruction will #UD.

VBLENDVPD permits the mask to be any XMM or YMM register. In contrast, BLENDVPD treats XMM0 implicitly as the mask and do not support non-destructive destination operation.

**Operation**

**BLENDVPD (128-bit Legacy SSE version)**

MASK ← XMM0
IF (MASK[63] = 0) THEN DEST[63:0] ← DEST[63:0]
ELSE DEST[63:0] ← SRC[63:0] FI
IF (MASK[127] = 0) THEN DEST[127:64] ← DEST[127:64]
ELSE DEST[127:64] ← SRC[127:64] FI

**VBLENDVPD (VEX.128 encoded version)**

MASK ← SRC3
IF (MASK[63] = 0) THEN DEST[63:0] ← SRC1[63:0]
ELSE DEST[63:0] ← SRC2[63:0] FI
IF (MASK[127] = 0) THEN DEST[127:64] ← SRC1[127:64]
ELSE DEST[127:64] ← SRC2[127:64] FI

**VBLENDVPD (VEX.256 encoded version)**

MASK ← SRC3
IF (MASK[63] = 0) THEN DEST[63:0] ← SRC1[63:0]
ELSE DEST[63:0] ← SRC2[63:0] FI
IF (MASK[127] = 0) THEN DEST[127:64] ← SRC1[127:64]
ELSE DEST[127:64] ← SRC2[127:64] FI
IF (MASK[255] = 0) THEN DEST[255:192] ← SRC1[255:192]  

**Intel C/C++ Compiler Intrinsic Equivalent**

BLENDVPD: __m128d _mm_blendv_pd(__m128d v1, __m128d v2, __m128d v3);

VBLENDVPD: __m128 _mm_blendv_pd (__m128d a, __m128d b, __m128d mask);

VBLENDVPD: __m256 _mm256_blendv_pd (__m256d a, __m256d b, __m256d mask);

**SIMD Floating-Point Exceptions**

None

**Other Exceptions**

See Exceptions Type 4; additionally

#UD  If VEX.W = 1.
BLENDVPS — Variable Blend Packed Single Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 14 /r</td>
<td>RM0</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Select packed single precision floating-point values from xmm1 and xmm2/m128 from mask specified in XMM0 and store the values into xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.W0 4A /r /is4</td>
<td>RVMR</td>
<td>V/V</td>
<td>AVX</td>
<td>Conditionally copy single-precision floating-point values from xmm2 or xmm3/m128 to xmm1, based on mask bits in the specified mask operand, xmm4.</td>
</tr>
<tr>
<td>VBLENDVPS xmm1, xmm2, xmm3/m128, xmm4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F3A.W0 4A /r /is4</td>
<td>RVMR</td>
<td>V/V</td>
<td>AVX</td>
<td>Conditionally copy single-precision floating-point values from ymm2 or ymm3/m256 to ymm1, based on mask bits in the specified mask register, ymm4.</td>
</tr>
<tr>
<td>VBLENDVPS ymm1, ymm2, ymm3/m256, ymm4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM0</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>implicit XMM0</td>
<td>NA</td>
</tr>
<tr>
<td>RVMR</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>imm8[7:4]</td>
</tr>
</tbody>
</table>

### Description

Conditionally copy each dword data element of single-precision floating-point value from the second source operand and the first source operand depending on mask bits defined in the mask register operand. The mask bits are the most significant bit in each dword element of the mask register.

Each quadword element of the destination operand is copied from:

- the corresponding dword element in the second source operand, If a mask bit is "1"; or
- the corresponding dword element in the first source operand, If a mask bit is "0"
The register assignment of the implicit mask operand for BLENDVPS is defined to be the architectural register XMM0.

128-bit Legacy SSE version: The first source operand and the destination operand is the same. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged. The mask register operand is implicitly defined to be the architectural register XMM0. An attempt to execute BLENDVPS with a VEX prefix will cause #UD.

VEX.128 encoded version: The first source operand and the destination operand are XMM registers. The second source operand is an XMM register or 128-bit memory location. The mask operand is the third source register, and encoded in bits[7:4] of the immediate byte(imm8). The bits[3:0] of imm8 are ignored. In 32-bit mode, imm8[7] is ignored. The upper bits (VLMAX-1:128) of the corresponding YMM register (destination register) are zeroed. VEX.W must be 0, otherwise, the instruction will #UD.

VEX.256 encoded version: The first source operand and destination operand are YMM registers. The second source operand can be a YMM register or a 256-bit memory location. The mask operand is the third source register, and encoded in bits[7:4] of the immediate byte(imm8). The bits[3:0] of imm8 are ignored. In 32-bit mode, imm8[7] is ignored. VEX.W must be 0, otherwise, the instruction will #UD.

VBLENDVPS permits the mask to be any XMM or YMM register. In contrast, BLENDVPS treats XMM0 implicitly as the mask and do not support non-destructive destination operation.

**Operation**

**BLENDVPS (128-bit Legacy SSE version)**

```
MASK ← XMM0
IF (MASK[31] = 0) THEN DEST[31:0] ← DEST[31:0]
  ELSE DEST[31:0] ← SRC[31:0] FI
IF (MASK[63] = 0) THEN DEST[63:32] ← DEST[63:32]
IF (MASK[95] = 0) THEN DEST[95:64] ← DEST[95:64]
  ELSE DEST[95:64] ← SRC[95:64] FI
IF (MASK[127] = 0) THEN DEST[127:96] ← DEST[127:96]
DEST[VLMAX-1:128] (Unmodified)
```

**VBLENDVPS (VEX.128 encoded version)**

```
MASK ← SRC3
IF (MASK[31] = 0) THEN DEST[31:0] ← SRC1[31:0]
  ELSE DEST[31:0] ← SRC2[31:0] FI
IF (MASK[63] = 0) THEN DEST[63:32] ← SRC1[63:32]
IF (MASK[95] = 0) THEN DEST[95:64] ← SRC1[95:64]
  ELSE DEST[95:64] ← SRC2[95:64] FI
```
BLENDVPS — Variable Blend Packed Single Precision Floating-Point Values

IF (MASK[127] = 0) THEN DEST[127:96] ← SRC1[127:96]
DEST[VLMAX-1:128] ← 0

VBLENDVPS (VEX.256 encoded version)
MASK ← SRC3
IF (MASK[31] = 0) THEN DEST[31:0] ← SRC1[31:0]
ELSE DEST [31:0] ← SRC2[31:0] FI
IF (MASK[63] = 0) THEN DEST[63:32] ← SRC1[63:32]
IF (MASK[95] = 0) THEN DEST[95:64] ← SRC1[95:64]
ELSE DEST [95:64] ← SRC2[95:64] FI
IF (MASK[127] = 0) THEN DEST[127:96] ← SRC1[127:96]
IF (MASK[159] = 0) THEN DEST[159:128] ← SRC1[159:128]
IF (MASK[255] = 0) THEN DEST[255:224] ← SRC1[255:224]

Intel C/C++ Compiler Intrinsic Equivalent
BLENDVPS: __m128 _mm_blendv_ps(__m128 v1, __m128 v2, __m128 v3);
VBLENDVPS: __m128 _mm_blendv_ps (__m128 a, __m128 b, __m128 mask);
VBLENDVPS: __m256 _mm256_blendv_ps (__m256 a, __m256 b, __m256 mask);

SIMD Floating-Point Exceptions
None

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.W = 1.
BOUND—Check Array Index Against Bounds

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>62 /r</td>
<td>BOUND r16,</td>
<td>RM</td>
<td>Invalid</td>
<td>Valid</td>
<td>Check if r16 (array index) is within bounds specified by m16&amp;16.</td>
</tr>
<tr>
<td></td>
<td>m16&amp;16</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>62 /r</td>
<td>BOUND r32,</td>
<td>RM</td>
<td>Invalid</td>
<td>Valid</td>
<td>Check if r32 (array index) is within bounds specified by m16&amp;16.</td>
</tr>
<tr>
<td></td>
<td>m32&amp;32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Description**

BOUND determines if the first operand (array index) is within the bounds of an array specified the second operand (bounds operand). The array index is a signed integer located in a register. The bounds operand is a memory location that contains a pair of signed doubleword-integers (when the operand-size attribute is 32) or a pair of signed word-integers (when the operand-size attribute is 16). The first doubleword (or word) is the lower bound of the array and the second doubleword (or word) is the upper bound of the array. The array index must be greater than or equal to the lower bound and less than or equal to the upper bound plus the operand size in bytes. If the index is not within bounds, a BOUND range exceeded exception (#BR) is signaled. When this exception is generated, the saved return instruction pointer points to the BOUND instruction.

The bounds limit data structure (two words or doublewords containing the lower and upper limits of the array) is usually placed just before the array itself, making the limits addressable via a constant offset from the beginning of the array. Because the address of the array already will be present in a register, this practice avoids extra bus cycles to obtain the effective address of the array bounds.

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

**Operation**

IF 64bit Mode
THEN
   #UD;
ELSE
   IF (ArrayIndex < LowerBound OR ArrayIndex > UpperBound)
   (* Below lower bound or above upper bound *)

BOUND—Check Array Index Against Bounds
THEN #BR; Fl;
Fl;

Flags Affected
None.

Protected Mode Exceptions
#BR If the bounds test fails.
#UD If second operand is not a memory location.
    If the LOCK prefix is used.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
#BR If the bounds test fails.
#UD If second operand is not a memory location.
    If the LOCK prefix is used.
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual-8086 Mode Exceptions
#BR If the bounds test fails.
#UD If second operand is not a memory location.
    If the LOCK prefix is used.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
BSF—Bit Scan Forward

**Opcode** | **Instruction** | **Op/En** | **64-bit Mode** | **Compat/Leg Mode** | **Description**
---|---|---|---|---|---
0F BC /r | BSF r16, r/m16 | RM | Valid | Valid | Bit scan forward on r/m16.
0F BC /r | BSF r32, r/m32 | RM | Valid | Valid | Bit scan forward on r/m32.
REX.W + 0F BC | BSF r64, r/m64 | RM | Valid | N.E. | Bit scan forward on r/m64.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**
Searches the source operand (second operand) for the least significant set bit (1 bit). If a least significant 1 bit is found, its bit index is stored in the destination operand (first operand). The source operand can be a register or a memory location; the destination operand is a register. The bit index is an unsigned offset from bit 0 of the source operand. If the content of the source operand is 0, the content of the destination operand is undefined.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF SRC = 0 THEN
  ZF ← 1;
  DEST is undefined;
ELSE
  ZF ← 0;
  temp ← 0;
  WHILE Bit(SRC, temp) = 0 DO
    temp ← temp + 1;
    DEST ← temp;
  OD;
FI;
Flags Affected
The ZF flag is set to 1 if all the source operand is 0; otherwise, the ZF flag is cleared. The CF, OF, SF, AF, and PF, flags are undefined.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
     If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
INSTRUCTION SET REFERENCE, A-L

#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.
BSR—Bit Scan Reverse

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BD /r</td>
<td>BSR r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Bit scan reverse on r/m16.</td>
</tr>
<tr>
<td>0F BD /r</td>
<td>BSR r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Bit scan reverse on r/m32.</td>
</tr>
<tr>
<td>REX.W + 0F BD</td>
<td>BSR r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Bit scan reverse on r/m64.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Searches the source operand (second operand) for the most significant set bit (1 bit). If a most significant 1 bit is found, its bit index is stored in the destination operand (first operand). The source operand can be a register or a memory location; the destination operand is a register. The bit index is an unsigned offset from bit 0 of the source operand. If the content source operand is 0, the content of the destination operand is undefined.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

IF SRC = 0
    THEN
        ZF ← 1;
        DEST is undefined;
    ELSE
        ZF ← 0;
        temp ← OperandSize - 1;
        WHILE Bit(SRC, temp) = 0 DO
            temp ← temp - 1;
            DEST ← temp;
        OD;
    FI;
Flags Affected
The ZF flag is set to 1 if all the source operand is 0; otherwise, the ZF flag is cleared. The CF, OF, SF, AF, and PF, flags are undefined.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)          If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD              If the LOCK prefix is used.
BSWAP—Byte Swap

**Description**

Reverses the byte order of a 32-bit or 64-bit (destination) register. This instruction is provided for converting little-endian values to big-endian format and vice versa. To swap bytes in a word value (16-bit register), use the XCHG instruction. When the BSWAP instruction references a 16-bit register, the result is undefined.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**IA-32 Architecture Legacy Compatibility**

The BSWAP instruction is not supported on IA-32 processors earlier than the Intel486™ processor family. For compatibility with this instruction, software should include functionally equivalent code for execution on Intel processors earlier than the Intel486 processor family.

**Operation**

TEMP ← DEST
IF 64-bit mode AND OperandSize = 64
THEN
  DEST[7:0] ← TEMP[63:56];
  DEST[15:8] ← TEMP[55:48];
  DEST[23:16] ← TEMP[47:40];
  DEST[39:32] ← TEMP[31:24];
BSWAP—Byte Swap

DEST[47:40] ← TEMP[23:16];
DEST[55:48] ← TEMP[15:8];
DEST[63:56] ← TEMP[7:0];
ELSE
  DEST[7:0] ← TEMP[31:24];
  DEST[15:8] ← TEMP[23:16];
  DEST[23:16] ← TEMP[15:8];
  DEST[31:24] ← TEMP[7:0];
FI;

Flags Affected
None.

Exceptions (All Operating Modes)
#UD If the LOCK prefix is used.
BT—Bit Test

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F A3</td>
<td>BT r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>0F A3</td>
<td>BT r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>REX.W + 0F A3</td>
<td>BT r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>0F BA /4 ib</td>
<td>BT r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>0F BA /4 ib</td>
<td>BT r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag.</td>
</tr>
<tr>
<td>REX.W + 0F BA /4 ib</td>
<td>BT r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM:r/m (r)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset (specified by the second operand) and stores the value of the bit in the CF flag. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value:

- If the bit base operand specifies a register, the instruction takes the modulo 16, 32, or 64 of the bit offset operand (modulo size depends on the mode and register size; 64-bit operands are available only in 64-bit mode).
- If the bit base operand specifies a memory location, the operand represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The range of the bit position that can be referenced by the offset operand depends on the operand size.

See also: **Bit(BitBase, BitOffset)** on page 3-14.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. In this case, the low-order 3 or 5 bits (3 for 16-bit operands, 5 for 32-bit operands) of the immediate bit offset are stored in the immediate bit offset field, and the high-order bits are shifted and combined with the byte displacement in the addressing mode by the assembler. The processor will ignore the high order bits if they are not zero.

When accessing a bit in memory, the processor may access 4 bytes starting from the memory address for a 32-bit operand size, using by the following relationship:
Effective Address + (4 \times \text{BitOffset Div 32})

Or, it may access 2 bytes starting from the memory address for a 16-bit operand, using this relationship:

Effective Address + (2 \times \text{BitOffset Div 16})

It may do so even when only a single byte needs to be accessed to reach the given bit. When using this bit addressing mechanism, software should avoid referencing areas of memory close to address space holes. In particular, it should avoid references to memory-mapped I/O registers. Instead, software should use the MOV instructions to load from or store to these addresses, and use the register form of these instructions to manipulate the data.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bit operands. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\text{CF} \leftarrow \text{Bit(BitBase, BitOffset)};
\]

**Flags Affected**

The CF flag contains the value of the selected bit. The ZF flag is unaffected. The OF, SF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
- #UD If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
BTC—Bit Test and Complement

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BB</td>
<td>BTC r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and complement.</td>
</tr>
<tr>
<td>0F BB</td>
<td>BTC r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and complement.</td>
</tr>
<tr>
<td>REX.W + 0F BB</td>
<td>BTC r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag and complement.</td>
</tr>
<tr>
<td>OF BA /7 ib</td>
<td>BTC r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and complement.</td>
</tr>
<tr>
<td>OF BA /7 ib</td>
<td>BTC r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and complement.</td>
</tr>
<tr>
<td>REX.W + 0F BA /7 ib</td>
<td>BTC r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag and complement.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
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</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM:r/m (r, w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM:r/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and complements the selected bit in the bit string. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value:

- If the bit base operand specifies a register, the instruction takes the modulo 16, 32, or 64 of the bit offset operand (modulo size depends on the mode and register size; 64-bit operands are available only in 64-bit mode). This allows any bit position to be selected.
- If the bit base operand specifies a memory location, the operand represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The range of the bit position that can be referenced by the offset operand depends on the operand size.

See also: Bit(BitBase, BitOffset) on page 3-14.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See “BT—Bit Test” in this chapter for more information on this addressing mechanism.
This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[ CF \leftarrow \text{Bit(BitBase, BitOffset)}; \]
\[ \text{Bit(BitBase, BitOffset)} \leftarrow \text{NOT Bit(BitBase, BitOffset)}; \]

**Flags Affected**

The CF flag contains the value of the selected bit before it is complemented. The ZF flag is unaffected. The OF, SF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

- #GP(0) If the destination operand points to a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register contains a NULL segment selector.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
- #UD If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
BTR—Bit Test and Reset

Description
Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and clears the selected bit in the bit string to 0. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value:

- If the bit base operand specifies a register, the instruction takes the modulo 16, 32, or 64 of the bit offset operand (modulo size depends on the mode and register size; 64-bit operands are available only in 64-bit mode). This allows any bit position to be selected.
- If the bit base operand specifies a memory location, the operand represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The range of the bit position that can be referenced by the offset operand depends on the operand size.

See also: **Bit(BitBase, BitOffset)** on page 3-14.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See "BT—Bit Test" in this chapter for more information on this addressing mechanism.

---

### Opcode Instruction Op/En | 64-bit Mode | Comp/Log Mode | Description
---|---|---|---
0F B3 BTR r/m16, r16 | MR Valid | Valid | Store selected bit in CF flag and clear.
0F B3 BTR r/m32, r32 | MR Valid | Valid | Store selected bit in CF flag and clear.
REX.W + 0F B3 BTR r/m64, r64 | MR Valid | N.E. | Store selected bit in CF flag and clear.
0F BA /6 ib BTR r/m16, imm8 | MI Valid | Valid | Store selected bit in CF flag and clear.
0F BA /6 ib BTR r/m32, imm8 | MI Valid | Valid | Store selected bit in CF flag and clear.
REX.W + 0F BA /6 ib BTR r/m64, imm8 | MI Valid | N.E. | Store selected bit in CF flag and clear.

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
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</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM</td>
<td>sr/m (r, w) ModRM</td>
<td>reg (r)</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM</td>
<td>sr/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>
This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
CF \leftarrow \text{Bit(BitBase, BitOffset)}; \\
\text{Bit(BitBase, BitOffset)} \leftarrow 0;
\]

**Flags Affected**

The CF flag contains the value of the selected bit before it is cleared. The ZF flag is unaffected. The OF, SF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

- **#GP(0)** If the destination operand points to a non-writable segment.
- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#GP(0)** If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
- **#UD** If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**

- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, A-L

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
**BTS—Bit Test and Set**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AB</td>
<td>BTS r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and set.</td>
</tr>
<tr>
<td>0F AB</td>
<td>BTS r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and set.</td>
</tr>
<tr>
<td>REX.W + 0F AB</td>
<td>BTS r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag and set.</td>
</tr>
<tr>
<td>0F BA /5 ib</td>
<td>BTS r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and set.</td>
</tr>
<tr>
<td>0F BA /5 ib</td>
<td>BTS r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Store selected bit in CF flag and set.</td>
</tr>
<tr>
<td>REX.W + 0F BA /5 ib</td>
<td>BTS r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store selected bit in CF flag and set.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM:r/m (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM:r/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and sets the selected bit in the bit string to 1. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value:

- If the bit base operand specifies a register, the instruction takes the modulo 16, 32, or 64 of the bit offset operand (modulo size depends on the mode and register size; 64-bit operands are available only in 64-bit mode). This allows any bit position to be selected.
- If the bit base operand specifies a memory location, the operand represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The range of the bit position that can be referenced by the offset operand depends on the operand size.

See also: **Bit(BitBase, BitOffset)** on page 3-14.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See “BT—Bit Test” in this chapter for more information on this addressing mechanism.
This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\begin{align*}
\text{CF} & \leftarrow \text{Bit(BitBase, BitOffset)}; \\
\text{Bit(BitBase, BitOffset)} & \leftarrow 1;
\end{align*}
\]

**Flags Affected**

The CF flag contains the value of the selected bit before it is set. The ZF flag is unaffected. The OF, SF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

- #GP(0) If the destination operand points to a non-writable segment.
- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #GP(0) If the DS, ES, FS, or GS register contains a NULL segment selector.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
- #UD If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**

- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
BTS—Bit Test and Set

INSTRUCTION SET REFERENCE, A-L

#SS  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

#UD  If the LOCK prefix is used but the destination is not a memory operand.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used but the destination is not a memory operand.
## CALL—Call Procedure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E8 cw</td>
<td>CALL rel16</td>
<td>M</td>
<td>N.S.</td>
<td>Valid</td>
<td>Call near, relative, displacement relative to next instruction.</td>
</tr>
<tr>
<td>E8 cd</td>
<td>CALL rel32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Call near, relative, displacement relative to next instruction. 32-bit displacement sign extended to 64-bits in 64-bit mode.</td>
</tr>
<tr>
<td>FF /2</td>
<td>CALL r/m16</td>
<td>M</td>
<td>N.E.</td>
<td>Valid</td>
<td>Call near, absolute indirect, address given in r/m16.</td>
</tr>
<tr>
<td>FF /2</td>
<td>CALL r/m32</td>
<td>M</td>
<td>N.E.</td>
<td>Valid</td>
<td>Call near, absolute indirect, address given in r/m32.</td>
</tr>
<tr>
<td>FF /2</td>
<td>CALL r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Call near, absolute indirect, address given in r/m64.</td>
</tr>
<tr>
<td>9A cd</td>
<td>CALL ptr16:16</td>
<td>D</td>
<td>Invalid</td>
<td>Valid</td>
<td>Call far, absolute, address given in operand.</td>
</tr>
<tr>
<td>9A cp</td>
<td>CALL ptr16:32</td>
<td>D</td>
<td>Invalid</td>
<td>Valid</td>
<td>Call far, absolute, address given in operand.</td>
</tr>
<tr>
<td>FF /3</td>
<td>CALL m16:16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Call far, absolute indirect address given in m16:16.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>In 32-bit mode: if selector points to a gate, then RIP = 32-bit zero extended displacement taken from gate; else RIP = zero extended 16-bit offset from far pointer referenced in the instruction.</td>
</tr>
<tr>
<td>FF /3</td>
<td>CALL m16:32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>In 64-bit mode: If selector points to a gate, then RIP = 64-bit displacement taken from gate; else RIP = zero extended 32-bit offset from far pointer referenced in the instruction.</td>
</tr>
</tbody>
</table>
CALL—Call Procedure

### Description

Saves procedure linking information on the stack and branches to the called procedure specified using the target operand. The target operand specifies the address of the first instruction in the called procedure. The operand can be an immediate value, a general-purpose register, or a memory location.

This instruction can be used to execute four types of calls:

- **Near Call** — A call to a procedure in the current code segment (the segment currently pointed to by the CS register), sometimes referred to as an intra-segment call.
- **Far Call** — A call to a procedure located in a different segment than the current code segment, sometimes referred to as an inter-segment call.
- **Inter-privilege-level far call** — A far call to a procedure in a segment at a different privilege level than that of the currently executing program or procedure.
- **Task switch** — A call to a procedure located in a different task.

The latter two call types (inter-privilege-level call and task switch) can only be executed in protected mode. See “Calling Procedures Using Call and RET” in Chapter 6 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for additional information on near, far, and inter-privilege-level calls. See Chapter 7, “Task Management,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A, for information on performing task switches with the CALL instruction.

**Near Call.** When executing a near call, the processor pushes the value of the EIP register (which contains the offset of the instruction following the CALL instruction) on the stack (for use later as a return-instruction pointer). The processor then
branches to the address in the current code segment specified by the target operand. The target operand specifies either an absolute offset in the code segment (an offset from the base of the code segment) or a relative offset (a signed displacement relative to the current value of the instruction pointer in the EIP register; this value points to the instruction following the CALL instruction). The CS register is not changed on near calls.

For a near call absolute, an absolute offset is specified indirectly in a general-purpose register or a memory location ($r/m16$, $r/m32$, or $r/m64$). The operand-size attribute determines the size of the target operand (16, 32 or 64 bits). When in 64-bit mode, the operand size for near call (and all near branches) is forced to 64-bits. Absolute offsets are loaded directly into the EIP(RIP) register. If the operand size attribute is 16, the upper two bytes of the EIP register are cleared, resulting in a maximum instruction pointer size of 16 bits. When accessing an absolute offset indirectly using the stack pointer [ESP] as the base register, the base value used is the value of the ESP before the instruction executes.

A relative offset ($rel16$ or $rel32$) is generally specified as a label in assembly code. But at the machine code level, it is encoded as a signed, 16- or 32-bit immediate value. This value is added to the value in the EIP(RIP) register. In 64-bit mode the relative offset is always a 32-bit immediate value which is sign extended to 64-bits before it is added to the value in the RIP register for the target calculation. As with absolute offsets, the operand-size attribute determines the size of the target operand (16, 32, or 64 bits). In 64-bit mode the target operand will always be 64-bits because the operand size is forced to 64-bits for near branches.

**Far Calls in Real-Address or Virtual-8086 Mode.** When executing a far call in real-address or virtual-8086 mode, the processor pushes the current value of both the CS and EIP registers on the stack for use as a return-instruction pointer. The processor then performs a “far branch” to the code segment and offset specified with the target operand for the called procedure. The target operand specifies an absolute far address either directly with a pointer ($ptr16:16$ or $ptr16:32$) or indirectly with a memory location ($m16:16$ or $m16:32$). With the pointer method, the segment and offset of the called procedure is encoded in the instruction using a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address immediate. With the indirect method, the target operand specifies a memory location that contains a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address. The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The far address is loaded directly into the CS and EIP registers. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared.

**Far Calls in Protected Mode.** When the processor is operating in protected mode, the CALL instruction can be used to perform the following types of far calls:

- Far call to the same privilege level
- Far call to a different privilege level (inter-privilege level call)
- Task switch (far call to another task)

In protected mode, the processor always uses the segment selector part of the far address to access the corresponding descriptor in the GDT or LDT. The descriptor
type (code segment, call gate, task gate, or TSS) and access rights determine the type of call operation to be performed.

If the selected descriptor is for a code segment, a far call to a code segment at the same privilege level is performed. (If the selected code segment is at a different privilege level and the code segment is non-conforming, a general-protection exception is generated.) A far call to the same privilege level in protected mode is very similar to one carried out in real-address or virtual-8086 mode. The target operand specifies an absolute far address either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The new code segment selector and its descriptor are loaded into CS register; the offset from the instruction is loaded into the EIP register.

A call gate (described in the next paragraph) can also be used to perform a far call to a code segment at the same privilege level. Using this mechanism provides an extra level of indirection and is the preferred method of making calls between 16-bit and 32-bit code segments.

When executing an inter-privilege-level far call, the code segment for the procedure being called must be accessed through a call gate. The segment selector specified by the target operand identifies the call gate. The target operand can specify the call gate segment selector either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). The processor obtains the segment selector for the new code segment and the new instruction pointer (offset) from the call gate descriptor. (The offset from the target operand is ignored when a call gate is used.)

On inter-privilege-level calls, the processor switches to the stack for the privilege level of the called procedure. The segment selector for the new stack segment is specified in the TSS for the currently running task. The branch to the new code segment occurs after the stack switch. (Note that when using a call gate to perform a far call to a segment at the same privilege level, no stack switch occurs.) On the new stack, the processor pushes the segment selector and stack pointer for the calling procedure's stack, an optional set of parameters from the calling procedure's stack, and the segment selector and instruction pointer for the calling procedure's code segment. (A value in the call gate descriptor determines how many parameters to copy to the new stack.) Finally, the processor branches to the address of the procedure being called within the new code segment.

Executing a task switch with the CALL instruction is similar to executing a call through a call gate. The target operand specifies the segment selector of the task gate for the new task activated by the switch (the offset in the target operand is ignored). The task gate in turn points to the TSS for the new task, which contains the segment selectors for the task's code and stack segments. Note that the TSS also contains the EIP value for the next instruction that was to be executed before the calling task was suspended. This instruction pointer value is loaded into the EIP register to re-start the calling task.

The CALL instruction can also specify the segment selector of the TSS directly, which eliminates the indirection of the task gate. See Chapter 7, "Task Management," in the
When you execute a task switch with a CALL instruction, the nested task flag (NT) is set in the EFLAGS register and the new TSS's previous task link field is loaded with the old task's TSS selector. Code is expected to suspend this nested task by executing an IRET instruction which, because the NT flag is set, automatically uses the previous task link to return to the calling task. (See “Task Linking” in Chapter 7 of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A, for information on nested tasks.) Switching tasks with the CALL instruction differs in this regard from the JMP instruction. JMP does not set the NT flag and therefore does not expect an IRET instruction to suspend the task.

**Mixing 16-Bit and 32-Bit Calls.** When making far calls between 16-bit and 32-bit code segments, use a call gate. If the far call is from a 32-bit code segment to a 16-bit code segment, the call should be made from the first 64 KBytes of the 32-bit code segment. This is because the operand-size attribute of the instruction is set to 16, so only a 16-bit return address offset can be saved. Also, the call should be made using a 16-bit call gate so that 16-bit values can be pushed on the stack. See Chapter 21, “Mixing 16-Bit and 32-Bit Code,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B, for more information.

**Far Calls in Compatibility Mode.** When the processor is operating in compatibility mode, the CALL instruction can be used to perform the following types of far calls:

1. Far call to the same privilege level, remaining in compatibility mode
2. Far call to the same privilege level, transitioning to 64-bit mode
3. Far call to a different privilege level (inter-privilege level call), transitioning to 64-bit mode

Note that a CALL instruction can not be used to cause a task switch in compatibility mode since task switches are not supported in IA-32e mode.

In compatibility mode, the processor always uses the segment selector part of the far address to access the corresponding descriptor in the GDT or LDT. The descriptor type (code segment, call gate) and access rights determine the type of call operation to be performed.

If the selected descriptor is for a code segment, a far call to a code segment at the same privilege level is performed. (If the selected code segment is at a different privilege level and the code segment is non-conforming, a general-protection exception is generated.) A far call to the same privilege level in compatibility mode is very similar to one carried out in protected mode. The target operand specifies an absolute far address either directly with a pointer (\texttt{ptr16:16} or \texttt{ptr16:32}) or indirectly with a memory location (\texttt{m16:16} or \texttt{m16:32}). The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The new code segment selector and its descriptor are loaded into CS register and the offset from the instruction is loaded into the EIP register. The difference is that 64-bit mode may be entered. This specified by the L bit in the new code segment descriptor.
Note that a 64-bit call gate (described in the next paragraph) can also be used to perform a far call to a code segment at the same privilege level. However, using this mechanism requires that the target code segment descriptor have the L bit set, causing an entry to 64-bit mode.

When executing an inter-privilege-level far call, the code segment for the procedure being called must be accessed through a 64-bit call gate. The segment selector specified by the target operand identifies the call gate. The target operand can specify the call gate segment selector either directly with a pointer ($ptr16:16$ or $ptr16:32$) or indirectly with a memory location ($m16:16$ or $m16:32$). The processor obtains the segment selector for the new code segment and the new instruction pointer (offset) from the 16-byte call gate descriptor. (The offset from the target operand is ignored when a call gate is used.)

On inter-privilege-level calls, the processor switches to the stack for the privilege level of the called procedure. The segment selector for the new stack segment is set to NULL. The new stack pointer is specified in the TSS for the currently running task. The branch to the new code segment occurs after the stack switch. (Note that when using a call gate to perform a far call to a segment at the same privilege level, an implicit stack switch occurs as a result of entering 64-bit mode. The SS selector is unchanged, but stack segment accesses use a segment base of 0x0, the limit is ignored, and the default stack size is 64-bits. The full value of RSP is used for the offset, of which the upper 32-bits are undefined.) On the new stack, the processor pushes the segment selector and stack pointer for the calling procedure's stack and the segment selector and instruction pointer for the calling procedure's code segment. (Parameter copy is not supported in IA-32e mode.) Finally, the processor branches to the address of the procedure being called within the new code segment.

Near/(Far) Calls in 64-bit Mode. When the processor is operating in 64-bit mode, the CALL instruction can be used to perform the following types of far calls:

- Far call to the same privilege level, transitioning to compatibility mode
- Far call to the same privilege level, remaining in 64-bit mode
- Far call to a different privilege level (inter-privilege level call), remaining in 64-bit mode

Note that in this mode the CALL instruction can not be used to cause a task switch in 64-bit mode since task switches are not supported in IA-32e mode.

In 64-bit mode, the processor always uses the segment selector part of the far address to access the corresponding descriptor in the GDT or LDT. The descriptor type (code segment, call gate) and access rights determine the type of call operation to be performed.

If the selected descriptor is for a code segment, a far call to a code segment at the same privilege level is performed. (If the selected code segment is at a different privilege level and the code segment is non-conforming, a general-protection exception is generated.) A far call to the same privilege level in 64-bit mode is very similar to one carried out in compatibility mode. The target operand specifies an absolute far address indirectly with a memory location ($m16:16$, $m16:32$ or $m16:64$). The form of CALL with a direct specification of absolute far address is not defined in 64-bit mode.
mode. The operand-size attribute determines the size of the offset (16, 32, or 64 bits) in the far address. The new code segment selector and its descriptor are loaded into the CS register; the offset from the instruction is loaded into the EIP register. The new code segment may specify entry either into compatibility or 64-bit mode, based on the L bit value.

A 64-bit call gate (described in the next paragraph) can also be used to perform a far call to a code segment at the same privilege level. However, using this mechanism requires that the target code segment descriptor have the L bit set.

When executing an inter-privilege-level far call, the code segment for the procedure being called must be accessed through a 64-bit call gate. The segment selector specified by the target operand identifies the call gate. The target operand can only specify the call gate segment selector indirectly with a memory location (m16:16, m16:32 or m16:64). The processor obtains the segment selector for the new code segment and the new instruction pointer (offset) from the 16-byte call gate descriptor. (The offset from the target operand is ignored when a call gate is used.)

On inter-privilege-level calls, the processor switches to the stack for the privilege level of the called procedure. The segment selector for the new stack segment is set to NULL. The new stack pointer is specified in the TSS for the currently running task. The branch to the new code segment occurs after the stack switch.

Note that when using a call gate to perform a far call to a segment at the same privilege level, an implicit stack switch occurs as a result of entering 64-bit mode. The SS selector is unchanged, but stack segment accesses use a segment base of 0x0, the limit is ignored, and the default stack size is 64-bits. (The full value of RSP is used for the offset.) On the new stack, the processor pushes the segment selector and stack pointer for the calling procedure's stack and the segment selector and instruction pointer for the calling procedure's code segment. (Parameter copy is not supported in IA-32e mode.) Finally, the processor branches to the address of the procedure being called within the new code segment.

**Operation**

IF near call
THEN IF near relative call
THEN
 IF OperandSize = 64
 THEN
   tempDEST ← SignExtend(DEST); (* DEST is rel32 *)
   tempRIP ← RIP + tempDEST;
   IF stack not large enough for a 8-byte return address
   THEN #SS(0): Fi;
   Push(RIP);
   RIP ← tempRIP;
   Fi;
   IF OperandSize = 32

   tempDEST ← SignExtend(DEST); (* DEST is rel32 *)
   tempRIP ← RIP + tempDEST;
   IF stack not large enough for a 8-byte return address
   THEN #SS(0): Fi;
   Push(RIP);
   RIP ← tempRIP;
   Fi;
   IF OperandSize = 32
THEN
  tempEIP ← EIP + DEST; (* DEST is rel32 *)
  IF tempEIP is not within code segment limit THEN #GP(0); Fl;
  IF stack not large enough for a 4-byte return address
    THEN #SS(0); Fl;
    Push(EIP);
    EIP ← tempEIP;
  FI;
IF OperandSize = 16
  THEN
    tempEIP ← (EIP + DEST) AND 0000FFFFH; (* DEST is rel16 *)
    IF tempEIP is not within code segment limit THEN #GP(0); Fl;
    IF stack not large enough for a 2-byte return address
      THEN #SS(0); Fl;
      Push(IP);
      EIP ← tempEIP;
  FI;
ELSE (* Near absolute call *)
  IF OperandSize = 64
    THEN
      tempRIP ← DEST; (* DEST is r/m64 *)
      IF stack not large enough for a 8-byte return address
        THEN #SS(0); Fl;
        Push(RIP);
        RIP ← tempRIP;
      FI;
    IF OperandSize = 32
      THEN
        tempEIP ← DEST; (* DEST is r/m32 *)
        IF tempEIP is not within code segment limit THEN #GP(0); Fl;
        IF stack not large enough for a 4-byte return address
          THEN #SS(0); Fl;
          Push(EIP);
          EIP ← tempEIP;
        FI;
      IF OperandSize = 16
        THEN
          tempEIP ← DEST AND 0000FFFFH; (* DEST is r/m16 *)
          IF tempEIP is not within code segment limit THEN #GP(0); Fl;
          IF stack not large enough for a 2-byte return address
            THEN #SS(0); Fl;
            Push(IP);
            EIP ← tempEIP;
IF far call and (PE = 0 or (PE = 1 and VM = 1)) (* Real-address or virtual-8086 mode *) 
THEN
   IF OperandSize = 32
      THEN
         IF stack not large enough for a 6-byte return address
            THEN #SS(0); Fl;
         IF DEST[31:16] is not zero THEN GP(0); Fl;
         Push(CS); (* Padded with 16 high-order bits *)
         Push(EIP);
         CS ← DEST[47:32]; (* DEST is ptr16:32 or [m16:32] *)
         EIP ← DEST[31:0]; (* DEST is ptr16:32 or [m16:32] *)
      ELSE (* OperandSize = 16 *)
         IF stack not large enough for a 4-byte return address
            THEN #SS(0); Fl;
         Push(CS);
         Push(IP);
         CS ← DEST[31:16]; (* DEST is ptr16:16 or [m16:16] *)
         EIP ← DEST[15:0]; (* DEST is ptr16:16 or [m16:16]; clear upper 16 bits *)
      FI;
   FI;
IF far call and (PE = 1 and VM = 0) (* Protected mode or IA-32e Mode, not virtual-8086 mode*) 
THEN
   IF segment selector in target operand NULL
      THEN #GP(0); Fl;
   IF segment selector index not within descriptor table limits
      THEN #GP(new code segment selector); Fl;
   Read type and access rights of selected segment descriptor;
   IF IA32_EFER.LMA = 0
      THEN
         IF segment type is not a conforming or nonconforming code segment, call 
         gate, task gate, or TSS
            THEN #GP(segment selector); Fl;
         ELSE
            IF segment type is not a conforming or nonconforming code segment or 
            64-bit call gate,
               THEN #GP(segment selector); Fl;
      FI;
   Depending on type and access rights:
CALL—Call Procedure

GO TO CONFORMING-CODE-SEGMENT;
GO TO NONCONFORMING-CODE-SEGMENT;
GO TO CALL-GATE;
GO TO TASK-GATE;
GO TO TASK-STATE-SEGMENT;
FI;

CONFORMING-CODE-SEGMENT:
IF L bit = 1 and D bit = 1 and IA32_EFER.LMA = 1
THEN GP(new code segment selector); FI;
IF DPL > CPL
THEN #GP(new code segment selector); FI;
IF segment not present
THEN #NP(new code segment selector); FI;
IF stack not large enough for return address
THEN #SS(0); FI;
tempEIP ← DEST(Offset);
IF OperandSize = 16
THEN
  tempEIP ← tempEIP AND 0000FFFFH; (* Clear upper 16 bits *)
IF (EFER.LMA = 0 or target mode = Compatibility mode) and (tempEIP outside new code segment limit)
THEN #GP(0); FI;
IF tempEIP is non-canonical
THEN #GP(0); FI;
IF OperandSize = 32
THEN
  Push(CS); (* Padded with 16 high-order bits *)
  Push(EIP);
  CS ← DEST(CodeSegmentSelector);
  (* Segment descriptor information also loaded *)
  CS(RPL) ← CPL;
  EIP ← tempEIP;
ELSE
  IF OperandSize = 16
  THEN
    Push(CS);  
    Push(IP);
    CS ← DEST(CodeSegmentSelector);
    (* Segment descriptor information also loaded *)
    CS(RPL) ← CPL;
    EIP ← tempEIP;
  ELSE (* OperandSize = 64 *)
INSTRUCTION SET REFERENCE, A-L

Push(CS); (* Padded with 48 high-order bits *)
Push(RIP);
CS ← DEST(CodeSegmentSelector);
(* Segment descriptor information also loaded *)
CS(RPL) ← CPL;
RIP ← tempEIP;

FI;
FI;
END;

NONCONFORMING-CODE-SEGMENT:
IF L-Bit = 1 and D-BIT = 1 and IA32_EFER.LMA = 1
THEN GP(new code segment selector); FI;
IF (RPL > CPL) or (DPL ≠ CPL)
THEN #GP(new code segment selector); FI;
IF segment not present
THEN #NP(new code segment selector); FI;
IF stack not large enough for return address
THEN #SS(0); FI;
tempEIP ← DEST(Offset);
IF OperandSize = 16
THEN tempEIP ← tempEIP AND 0000FFFFH; FI; (* Clear upper 16 bits *)
IF (EFER.LMA = 0 or target mode = Compatibility mode) and (tempEIP outside new code segment limit)
THEN #GP(0); FI;
IF tempEIP is non-canonical
THEN #GP(0); FI;
IF OperandSize = 32
THEN
Push(CS); (* Padded with 16 high-order bits *)
Push(EIP);
CS ← DEST(CodeSegmentSelector);
(* Segment descriptor information also loaded *)
CS(RPL) ← CPL;
EIP ← tempEIP;
ELSE
IF OperandSize = 16
THEN
Push(CS);
Push(IP);
CS ← DEST(CodeSegmentSelector);
(* Segment descriptor information also loaded *)
CS(RPL) ← CPL;
EIP ← tempEIP;
ELSE (* OperandSize = 64 *)

   Push(CS); (* Padded with 48 high-order bits *)
   Push(RIP);
   CS ← DEST(CodeSegmentSelector);
   (* Segment descriptor information also loaded *)
   CS(RPL) ← CPL;
   RIP ← tempEIP;

   FI;
   FI;
END;

CALL-GATE:

   IF call gate (DPL < CPL) or (RPL > DPL)
   THEN #GP(call-gate selector); FI;
   IF call gate not present
   THEN #NP(call-gate selector); FI;
   IF call-gate code-segment selector is NULL
   THEN #GP(0); FI;
   IF call-gate code-segment selector index is outside descriptor table limits
   THEN #GP(call-gate code-segment selector); FI;
   Read call-gate code-segment descriptor;
   IF call-gate code-segment descriptor does not indicate a code segment
   or call-gate code-segment descriptor DPL > CPL
   THEN #GP(call-gate code-segment selector); FI;
   IF IA32_EFER.LMA = 1 AND (call-gate code-segment descriptor is
   not a 64-bit code segment or call-gate code-segment descriptor has both L-bit and D-bit set)
   THEN #GP(call-gate code-segment selector); FI;
   IF call-gate code segment not present
   THEN #NP(call-gate code-segment selector); FI;
   IF call-gate code segment is non-conforming and DPL < CPL
   THEN go to MORE-PRIVILEGE;
   ELSE go to SAME-PRIVILEGE;
   FI;
END;

MORE-PRIVILEGE:

   IF current TSS is 32-bit
   THEN
      TSSstackAddress ← (new code-segment DPL * 8) + 4;
      IF (TSSstackAddress + 5) > current TSS limit
         THEN #TS(current TSS selector); FI;
      NewSS ← 2 bytes loaded from (TSS base + TSSstackAddress + 4);
      NewESP ← 4 bytes loaded from (TSS base + TSSstackAddress);
      ELSE
INSTRUCTION SET REFERENCE, A-L

IF current TSS is 16-bit
THEN
    TSSstackAddress ← (new code-segment DPL + 4) + 2
    IF (TSSstackAddress + 3) > current TSS limit
        THEN #TS(current TSS selector); FI;
    NewSS ← 2 bytes loaded from (TSS base + TSSstackAddress + 2);
    NewESP ← 2 bytes loaded from (TSS base + TSSstackAddress);
ELSE (* current TSS is 64-bit *)
    TSSstackAddress ← (new code-segment DPL + 8) + 4;
    IF (TSSstackAddress + 7) > current TSS limit
        THEN #TS(current TSS selector); FI;
    NewSS ← new code-segment DPL; (* NULL selector with RPL = new CPL *)
    NewRSP ← 8 bytes loaded from (current TSS base + TSSstackAddress);
FI;

FI;
IF IA32_EFER.LMA = 0 and NewSS is NULL
THEN #TS(NewSS); FI;
Read new code-segment descriptor and new stack-segment descriptor;
IF IA32_EFER.LMA = 0 and (NewSS RPL ≠ new code-segment DPL
or new stack-segment DPL ≠ new code-segment DPL or new stack segment is not a
writable data segment)
    THEN #TS(NewSS); FI;
IF IA32_EFER.LMA = 0 and new stack segment not present
THEN #SS(NewSS); FI;
IF CallGateSize = 32
THEN
    IF new stack does not have room for parameters plus 16 bytes
        THEN #SS(NewSS); FI;
    IF CallGate(InstructionPointer) not within new code-segment limit
        THEN #GP(0); FI;
    SS ← newSS; (* Segment descriptor information also loaded *)
    ESP ← newESP;
    CS:EIP ← CallGate(CS:InstructionPointer);
    (* Segment descriptor information also loaded *)
    Push(oldSS:oldESP); (* From calling procedure *)
    temp ← parameter count from call gate, masked to 5 bits;
    Push(parameters from calling procedure's stack, temp)
    Push(oldCS:oldEIP); (* Return address to calling procedure *)
ELSE
    IF CallGateSize = 16
    THEN
        IF new stack does not have room for parameters plus 8 bytes
            THEN #SS(NewSS); FI;
        IF (CallGate(InstructionPointer) AND FFFFH) not in new code-segment limit
            THEN #SS(NewSS); FI;

CALL—Call Procedure

THEN #GP(0); Fi;
SS ← newSS; (* Segment descriptor information also loaded *)
ESP ← newESP;
CS:IP ← CallGate(CS:InstructionPointer);
(* Segment descriptor information also loaded *)
Push(oldSS:oldESP); (* From calling procedure *)
temp ← parameter count from call gate, masked to 5 bits;
Push(parameters from calling procedure’s stack, temp)
Push(oldCS:oldEIP); (* Return address to calling procedure *)
ELSE (* CallGateSize = 64 *)
IF pushing 32 bytes on the stack would use a non-canonical address
THEN #SS(NewSS); Fi;
IF (CallGate(InstructionPointer) is non-canonical)
THEN #GP(0); Fi;
SS ← NewSS; (* NewSS is NULL)
RSP ← NewESP;
CS:IP ← CallGate(CS:InstructionPointer);
(* Segment descriptor information also loaded *)
Push(oldSS:oldESP); (* From calling procedure *)
Push(oldCS:oldEIP); (* Return address to calling procedure *)
Fi;
Fi;
CPL ← CodeSegment(DPL)
CS(RPL) ← CPL
END;
SAME-PRIVILEGE:
IF CallGateSize = 32
THEN
IF stack does not have room for 8 bytes
THEN #SS(0); Fi;
IF CallGate(InstructionPointer) not within code segment limit
THEN #GP(0); Fi;
CS:EIP ← CallGate(CS:EIP) (* Segment descriptor information also loaded *)
Push(oldCS:oldEIP); (* Return address to calling procedure *)
ELSE
If CallGateSize = 16
THEN
IF stack does not have room for 4 bytes
THEN #SS(0); Fi;
IF CallGate(InstructionPointer) not within code segment limit
THEN #GP(0); Fi;
CS:IP ← CallGate(CS:Instruction pointer);
CALL—Call Procedure

(* Segment descriptor information also loaded *)
Push(oldCS:oldIP); (* Return address to calling procedure *)
ELSE (* CallGateSize = 64 *)
IF pushing 16 bytes on the stack touches non-canonical addresses
THEN #SS(0); FI;
IF RIP non-canonical
THEN #GP(0); FI;
CS:IP ← CallGate(CS:instruction pointer);
(* Segment descriptor information also loaded *)
Push(oldCS:oldIP); (* Return address to calling procedure *)
FI;
FI;
CS(RPL) ← CPL
END;

TASK-GATE:
IF task gate DPL < CPL or RPL
THEN #GP(task gate selector); FI;
IF task gate not present
THEN #NP(task gate selector); FI;
Read the TSS segment selector in the task-gate descriptor;
IF TSS segment selector local/global bit is set to local
or index not within GDT limits
THEN #GP(TSS selector); FI;
Access TSS descriptor in GDT;
IF TSS descriptor specifies that the TSS is busy (low-order 5 bits set to 00001)
THEN #GP(TSS selector); FI;
IF TSS not present
THEN #NP(TSS selector); FI;
SWITCH-TASKS (with nesting) to TSS;
IF EIP not within code segment limit
THEN #GP(0); FI;
END;

TASK-STATE-SEGMENT:
IF TSS DPL < CPL or RPL
or TSS descriptor indicates TSS not available
THEN #GP(TSS selector); FI;
IF TSS is not present
THEN #NP(TSS selector); FI;
SWITCH-TASKS (with nesting) to TSS;
IF EIP not within code segment limit
THEN #GP(0); FI;
END;

Flags Affected
All flags are affected if a task switch occurs; no flags are affected if a task switch does not occur.

Protected Mode Exceptions

#GP(0)  If the target offset in destination operand is beyond the new code segment limit.
If the segment selector in the destination operand is NULL.
If the code segment selector in the gate is NULL.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#GP(selector)  If a code segment or gate or TSS selector index is outside descriptor table limits.
If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, call gate, task gate, or task state segment.
If the DPL for a nonconforming-code segment is not equal to the CPL or the RPL for the segment’s segment selector is greater than the CPL.
If the DPL for a conforming-code segment is greater than the CPL.
If the DPL from a call-gate, task-gate, or TSS segment descriptor is less than the CPL or than the RPL of the call-gate, task-gate, or TSS’s segment selector.
If the segment descriptor for a segment selector from a call gate does not indicate it is a code segment.
If the segment selector from a call gate is beyond the descriptor table limits.
If the DPL for a code-segment obtained from a call gate is greater than the CPL.
If the segment selector for a TSS has its local/global bit set for local.
If a TSS segment descriptor specifies that the TSS is busy or not available.
INSTRUCTION SET REFERENCE, A-L

#SS(0) If pushing the return address, parameters, or stack segment pointer onto the stack exceeds the bounds of the stack segment, when no stack switch occurs.
   If a memory operand effective address is outside the SS segment limit.

#SS(selector) If pushing the return address, parameters, or stack segment pointer onto the stack exceeds the bounds of the stack segment, when a stack switch occurs.
   If the SS register is being loaded as part of a stack switch and the segment pointed to is marked not present.
   If stack segment does not have room for the return address, parameters, or stack segment pointer, when stack switch occurs.

#NP(selector) If a code segment, data segment, stack segment, call gate, task gate, or TSS is not present.

#TS(selector) If the new stack segment selector and ESP are beyond the end of the TSS.
   If the new stack segment selector is NULL.
   If the RPL of the new stack segment selector in the TSS is not equal to the DPL of the code segment being accessed.
   If DPL of the stack segment descriptor for the new stack segment is not equal to the DPL of the code segment descriptor.
   If the new stack segment is not a writable data segment.
   If segment-selector index for stack segment is outside descriptor table limits.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the target offset is beyond the code segment limit.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the target offset is beyond the code segment limit.

#PF(fault-code) If a page fault occurs.
CALL—Call Procedure

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
#GP(selector) If a memory address accessed by the selector is in non-canonical space.
#GP(0) If the target offset in the destination operand is non-canonical.

64-Bit Mode Exceptions
#GP(0) If a memory address is non-canonical.
If target offset in destination operand is non-canonical.
If the segment selector in the destination operand is NULL.
If the code segment selector in the 64-bit gate is NULL.
#GP(selector) If code segment or 64-bit call gate is outside descriptor table limits.
If code segment or 64-bit call gate overlaps non-canonical space.
If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, or 64-bit call gate.
If the segment descriptor pointed to by the segment selector in the destination operand is a code segment and has both the D-bit and the L-bit set.
If the DPL for a nonconforming-code segment is not equal to the CPL, or the RPL for the segment’s segment selector is greater than the CPL.
If the DPL for a conforming-code segment is greater than the CPL.
If the DPL from a 64-bit call-gate is less than the CPL or than the RPL of the 64-bit call-gate.
If the upper type field of a 64-bit call gate is not 0x0.
If the segment selector from a 64-bit call gate is beyond the descriptor table limits.
If the DPL for a code-segment obtained from a 64-bit call gate is greater than the CPL.
If the code segment descriptor pointed to by the selector in the 64-bit gate doesn’t have the L-bit set and the D-bit clear.
If the segment descriptor for a segment selector from the 64-bit call gate does not indicate it is a code segment.
INSTRUCTION SET REFERENCE, A-L

#SS(0)  If pushing the return offset or CS selector onto the stack exceeds the bounds of the stack segment when no stack switch occurs.
   If a memory operand effective address is outside the SS segment limit.
   If the stack address is in a non-canonical form.
#SS(selector)  If pushing the old values of SS selector, stack pointer, EFLAGS, CS selector, offset, or error code onto the stack violates the canonical boundary when a stack switch occurs.
#NP(selector)  If a code segment or 64-bit call gate is not present.
#TS(selector)  If the load of the new RSP exceeds the limit of the TSS.
#UD  (64-bit mode only) If a far call is direct to an absolute address in memory.
      If the LOCK prefix is used.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
CBW/CWDE/CDQE—Convert Byte to Word/Convert Word to Doubleword/Convert Doubleword to Quadword

**Description**
Double the size of the source operand by means of sign extension. The CBW (convert byte to word) instruction copies the sign (bit 7) in the source operand into every bit in the AH register. The CWDE (convert word to doubleword) instruction copies the sign (bit 15) of the word in the AX register into the high 16 bits of the EAX register.

CBW and CWDE reference the same opcode. The CBW instruction is intended for use when the operand-size attribute is 16; CWDE is intended for use when the operand-size attribute is 32. Some assemblers may force the operand size. Others may treat these two mnemonics as synonyms (CBW/CWDE) and use the setting of the operand-size attribute to determine the size of values to be converted.

In 64-bit mode, the default operation size is the size of the destination register. Use of the REX.W prefix promotes this instruction (CDQE when promoted) to operate on 64-bit operands. In which case, CDQE copies the sign (bit 31) of the doubleword in the EAX register into the high 32 bits of RAX.

**Operation**

IF OperandSize = 16 (* Instruction = CBW *)
THEN
   AX ← SignExtend(AL);
ELSE IF (OperandSize = 32, Instruction = CWDE)
   EAX ← SignExtend(AX); Fl;
ELSE (* 64-Bit Mode, OperandSize = 64, Instruction = CDQE*)
   RAX ← SignExtend(EAX);
Fl;

**Flags Affected**
None.
Exceptions (All Operating Modes)

#UD If the LOCK prefix is used.
**CLC—Clear Carry Flag**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F8</td>
<td>CLC</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Clear CF flag.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Clears the CF flag in the EFLAGS register. Operation is the same in all non-64-bit modes and 64-bit mode.

**Operation**

\[ CF \leftarrow 0; \]

**Flags Affected**

The CF flag is set to 0. The OF, ZF, SF, AF, and PF flags are unaffected.

**Exceptions (All Operating Modes)**

#UD If the LOCK prefix is used.
CLD—Clear Direction Flag

**Description**
Clears the DF flag in the EFLAGS register. When the DF flag is set to 0, string operations increment the index registers (ESI and/or EDI). Operation is the same in all non-64-bit modes and 64-bit mode.

**Operation**
\[ \text{DF} \leftarrow 0; \]

**Flags Affected**
The DF flag is set to 0. The CF, OF, ZF, SF, AF, and PF flags are unaffected.

**Exceptions (All Operating Modes)**
#UD If the LOCK prefix is used.

---

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
CLFLUSH—Flush Cache Line

Invalidates the cache line that contains the linear address specified with the source operand from all levels of the processor cache hierarchy (data and instruction). The invalidation is broadcast throughout the cache coherence domain. If, at any level of the cache hierarchy, the line is inconsistent with memory (dirty) it is written to memory before invalidation. The source operand is a byte memory location.

The availability of CLFLUSH is indicated by the presence of the CPUID feature flag CLFSH (bit 19 of the EDX register, see “CPUID—CPU Identification” in this chapter). The aligned cache line size affected is also indicated with the CPUID instruction (bits 8 through 15 of the EBX register when the initial value in the EAX register is 1).

The memory attribute of the page containing the affected line has no effect on the behavior of this instruction. It should be noted that processors are free to speculatively fetch and cache data from system memory regions assigned a memory-type allowing for speculative reads (such as, the WB, WC, and WT memory types). PREFETCHh instructions can be used to provide the processor with hints for this speculative behavior. Because this speculative fetching can occur at any time and is not tied to instruction execution, the CLFLUSH instruction is not ordered with respect to PREFETCHh instructions or any of the speculative fetching mechanisms (that is, data can be speculatively loaded into a cache line just before, during, or after the execution of a CLFLUSH instruction that references the cache line).

CLFLUSH is only ordered by the MFENCE instruction. It is not guaranteed to be ordered by any other fencing or serializing instructions or by another CLFLUSH instruction. For example, software can use an MFENCE instruction to ensure that previous stores are included in the write-back.

The CLFLUSH instruction can be used at all privilege levels and is subject to all permission checking and faults associated with a byte load (and in addition, a CLFLUSH instruction is allowed to flush a linear address in an execute-only segment). Like a load, the CLFLUSH instruction sets the A bit but not the D bit in the page tables.

The CLFLUSH instruction was introduced with the SSE2 extensions; however, because it has its own CPUID feature flag, it can be implemented in IA-32 processors.

### Opcode

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /7</td>
<td>CLFLUSH m8</td>
<td>M</td>
<td>Valid</td>
<td>Flushes cache line containing m8.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM/r/m (w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
that do not include the SSE2 extensions. Also, detecting the presence of the SSE2 extensions with the CPUID instruction does not guarantee that the CLFLUSH instruction is implemented in the processor.

CLFLUSH operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

Flush_Cache_Line(SRC);

**Intel C/C++ Compiler Intrinsic Equivalents**

CLFLUSH: void _mm_clflush(void const *p)

**Protected Mode Exceptions**

- #GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
- #SS(0) For an illegal address in the SS segment.
- #PF(fault-code) For a page fault.
- #UD If CPUID.01H:EDX.CLFSH[bit 19] = 0.
  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- #GP If any part of the operand lies outside the effective address space from 0 to FFFFH.
- #UD If CPUID.01H:EDX.CLFSH[bit 19] = 0.
  If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.

- #PF(fault-code) For a page fault.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- #SS(0) If a memory address referencing the SS segment is in a non-canonical form.
- #GP(0) If the memory address is in a non-canonical form.
- #PF(fault-code) For a page fault.
- #UD If CPUID.01H:EDX.CLFSH[bit 19] = 0.
  If the LOCK prefix is used.
CLI — Clear Interrupt Flag

### Opcode 

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Comp/Gen Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FA</td>
<td>CLI</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Clear interrupt flag; interrupts disabled when interrupt flag cleared.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

If protected-mode virtual interrupts are not enabled, CLI clears the IF flag in the EFLAGS register. No other flags are affected. Clearing the IF flag causes the processor to ignore maskable external interrupts. The IF flag and the CLI and STI instruction have no affect on the generation of exceptions and NMI interrupts.

When protected-mode virtual interrupts are enabled, CPL is 3, and IOPL is less than 3; CLI clears the VIF flag in the EFLAGS register, leaving IF unaffected. Table 3-6 indicates the action of the CLI instruction depending on the processor operating mode and the CPL/IOPL of the running program or procedure.

CLI operation is the same in non-64-bit modes and 64-bit mode.

### Table 3-6. Decision Table for CLI Results

<table>
<thead>
<tr>
<th>PE</th>
<th>VM</th>
<th>IOPL</th>
<th>CPL</th>
<th>PVI</th>
<th>VIP</th>
<th>VME</th>
<th>CLI Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>≥ CPL</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VIF = 0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>GP Fault</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>GP Fault</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>VIF = 0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>GP Fault</td>
</tr>
</tbody>
</table>

**NOTES:**

* X = This setting has no impact.

### Operation

IF PE = 0
THEN
  IF ← 0; (* Reset Interrupt Flag *)
ELSE
  IF VM = 0;
    THEN
      IF IOPL ≥ CPL
        THEN
          IF ← 0; (* Reset Interrupt Flag *)
        ELSE
          IF ((IOPL < CPL) and (CPL = 3) and (PVI = 1))
            THEN
              VIF ← 0; (* Reset Virtual Interrupt Flag *)
            ELSE
              #GP(0);
        FI;
      FI;
    ELSE (* VM = 1 *)
      IF IOPL = 3
        THEN
          IF ← 0; (* Reset Interrupt Flag *)
        ELSE
          IF (IOPL < 3) AND (VME = 1)
            THEN
              VIF ← 0; (* Reset Virtual Interrupt Flag *)
            ELSE
              #GP(0);
        FI;
      FI;
    FI;

Flags Affected
If protected-mode virtual interrupts are not enabled, IF is set to 0 if the CPL is equal to or less than the IOPL; otherwise, it is not affected. The other flags in the EFLAGS register are unaffected.

When protected-mode virtual interrupts are enabled, CPL is 3, and IOPL is less than 3; CLI clears the VIF flag in the EFLAGS register, leaving IF unaffected.

Protected Mode Exceptions
#GP(0)  If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.
#UD  If the LOCK prefix is used.
Real-Address Mode Exceptions

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.

#UD If the LOCK prefix is used.
CLTS—Clear Task-Switched Flag in CR0

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 06</td>
<td>CLTS</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Clears TS flag in CR0.</td>
</tr>
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</table>

InstructionOperand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Clears the task-switched (TS) flag in the CR0 register. This instruction is intended for use in operating-system procedures. It is a privileged instruction that can only be executed at a CPL of 0. It is allowed to be executed in real-address mode to allow initialization for protected mode.

The processor sets the TS flag every time a task switch occurs. The flag is used to synchronize the saving of FPU context in multitasking applications. See the description of the TS flag in the section titled “Control Registers” in Chapter 2 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A, for more information about this flag.

CLTS operation is the same in non-64-bit modes and 64-bit mode.

See Chapter 25, “VMX Non-Root Operation,” of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, for more information about the behavior of this instruction in VMX non-root operation.

Operation

CR0.TS[bit 3] ← 0;

Flags Affected

The TS flag in CR0 register is cleared.

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#UD If the LOCK prefix is used.
Virtual-8086 Mode Exceptions
#GP(0) CLTS is not recognized in virtual-8086 mode.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the CPL is greater than 0.
#UD If the LOCK prefix is used.
CMC—Complement Carry Flag

**Description**
Complements the CF flag in the EFLAGS register. CMC operation is the same in non-64-bit modes and 64-bit mode.

**Operation**
EFLAGS.CF[bit 0] ← NOT EFLAGS.CF[bit 0];

**Flags Affected**
The CF flag contains the complement of its original value. The OF, ZF, SF, AF, and PF flags are unaffected.

**Exceptions (All Operating Modes)**
#UD If the LOCK prefix is used.
# CMOVcc—Conditional Move

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 47 /r</td>
<td>CMOVA r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>0F 47 /r</td>
<td>CMOVA r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if above (CF=0 and ZF=0).</td>
</tr>
<tr>
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<td>CMOVA r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>0F 43 /r</td>
<td>CMOVAE r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if above or equal (CF=0).</td>
</tr>
<tr>
<td>0F 43 /r</td>
<td>CMOVAE r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if above or equal (CF=0).</td>
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<td>Valid</td>
<td>N.E.</td>
<td>Move if above or equal (CF=0).</td>
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<tr>
<td>0F 42 /r</td>
<td>CMOVB r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below (CF=1).</td>
</tr>
<tr>
<td>0F 42 /r</td>
<td>CMOVB r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below (CF=1).</td>
</tr>
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<td>REX.W + 0F 42 /r</td>
<td>CMOVB r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if below (CF=1).</td>
</tr>
<tr>
<td>0F 46 /r</td>
<td>CMOVBE r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below or equal (CF=1 or ZF=1).</td>
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<tr>
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<td>CMOVBE r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if below or equal (CF=1 or ZF=1).</td>
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<td>Valid</td>
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<td>Move if below or equal (CF=1 or ZF=1).</td>
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<tr>
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<td>Valid</td>
<td>N.E.</td>
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<tr>
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<td>RM</td>
<td>Valid</td>
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<td>Move if equal (ZF=1).</td>
</tr>
<tr>
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<td>Move if greater (ZF=0 and SF=OF).</td>
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<tr>
<td>0F 4F /r</td>
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<td>RM</td>
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<td>Valid</td>
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<td>Op/En</td>
<td>64-Bit Mode</td>
<td>Compat/ Leg Mode</td>
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<td>-------------</td>
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<td>------------------------------------------------</td>
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<tr>
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<td>Valid</td>
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<td>Move if less (SF≠ OF).</td>
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<td>Move if less (SF≠ OF).</td>
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<td>Valid</td>
<td>Move if not above or equal (CF=1).</td>
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<td>RM</td>
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<td>Valid</td>
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<td>RM</td>
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<tr>
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<td>CMOVNB r16, r/m16</td>
<td>RM</td>
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</tr>
<tr>
<td>0F 43</td>
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<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>Op/En</td>
<td>64-Bit Mode</td>
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<td>Move if not equal (ZF=1 or SF≠OF).</td>
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<tr>
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<td>CMOVNC r16, r/m16</td>
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<td>RM</td>
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<td>Move if not carry (CF=0).</td>
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<td>RM</td>
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<td>Move if not equal (ZF=0).</td>
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<td>0F 45 /r</td>
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<td>REX.W + 0F 45 /r</td>
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<td>RM</td>
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<td>Move if not equal (ZF=0).</td>
</tr>
<tr>
<td>0F 4E /r</td>
<td>CMOVNG r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
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<td>Move if not greater (SF=OF).</td>
</tr>
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<td>0F 4E /r</td>
<td>CMOVNG r32, r/m32</td>
<td>RM</td>
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<td>Move if not greater (SF=OF).</td>
</tr>
<tr>
<td>0F 4C /r</td>
<td>CMOVNGE r16, r/m16</td>
<td>RM</td>
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<td>Move if not greater or equal (SF≠OF).</td>
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<tr>
<td>0F 4C /r</td>
<td>CMOVNGE r32, r/m32</td>
<td>RM</td>
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<td>Valid</td>
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</tr>
<tr>
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<td>Move if not greater or equal (SF≠OF).</td>
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<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not less (SF=OF).</td>
</tr>
<tr>
<td>0F 4D /r</td>
<td>CMOVNL r32, r/m32</td>
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<td>Move if not less (SF=OF).</td>
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<td>0F 4F /r</td>
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<td>Move if not less or equal (ZF=0 and SF=OF).</td>
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<td>N.E.</td>
<td>Move if not less or equal (ZF=0 and SF=OF).</td>
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<td>CMOVNO r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not overflow (OF=0).</td>
</tr>
<tr>
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<td>CMOVNO r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not overflow (OF=0).</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>Op/En</td>
<td>64-Bit Mode</td>
<td>Compat/Leg Mode</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
<td>-------</td>
<td>-------------</td>
<td>-----------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>REX.W + 0F 41 /r</td>
<td>CMOVNO r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not overflow (OF=0).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVNP r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not parity (PF=0).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVNP r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not parity (PF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 4B /r</td>
<td>CMOVNP r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not parity (PF=0).</td>
</tr>
<tr>
<td>0F 49 /r</td>
<td>CMOVNS r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not sign (SF=0).</td>
</tr>
<tr>
<td>0F 49 /r</td>
<td>CMOVNS r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not sign (SF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 49 /r</td>
<td>CMOVNS r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not sign (SF=0).</td>
</tr>
<tr>
<td>0F 45 /r</td>
<td>CMOVNZ r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not zero (ZF=0).</td>
</tr>
<tr>
<td>0F 45 /r</td>
<td>CMOVNZ r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if not zero (ZF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 45 /r</td>
<td>CMOVNZ r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if not zero (ZF=0).</td>
</tr>
<tr>
<td>0F 40 /r</td>
<td>CMOVO r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if overflow (OF=1).</td>
</tr>
<tr>
<td>0F 40 /r</td>
<td>CMOVO r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if overflow (OF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 40 /r</td>
<td>CMOVO r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if overflow (OF=1).</td>
</tr>
<tr>
<td>0F 4A /r</td>
<td>CMOVPE r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity even (PF=1).</td>
</tr>
<tr>
<td>0F 4A /r</td>
<td>CMOVPE r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity even (PF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 4A /r</td>
<td>CMOVPE r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if parity even (PF=1).</td>
</tr>
<tr>
<td>0F 4A /r</td>
<td>CMOVPE r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>0F 4A /r</td>
<td>CMOVPE r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 4A /r</td>
<td>CMOVPE r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVPO r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVPO r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>REX.W + 0F 4B /r</td>
<td>CMOVPO r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if parity odd (PF=0).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVS r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if sign (SF=1).</td>
</tr>
<tr>
<td>0F 4B /r</td>
<td>CMOVS r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if sign (SF=1).</td>
</tr>
<tr>
<td>REX.W + 0F 4B /r</td>
<td>CMOVS r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move if sign (SF=1).</td>
</tr>
<tr>
<td>0F 44 /r</td>
<td>CMOVZ r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move if zero (ZF=1).</td>
</tr>
</tbody>
</table>
CMOVcc—Conditional Move

**Description**

The CMOVcc instructions check the state of one or more of the status flags in the EFLAGS register (CF, OF, PF, SF, and ZF) and perform a move operation if the flags are in a specified state (or condition). A condition code (cc) is associated with each instruction to indicate the condition being tested for. If the condition is not satisfied, a move is not performed and execution continues with the instruction following the CMOVcc instruction.

These instructions can move 16-bit, 32-bit or 64-bit values from memory to a general-purpose register or from one general-purpose register to another. Conditional moves of 8-bit register operands are not supported.

The condition for each CMOVcc mnemonic is given in the description column of the above table. The terms “less” and “greater” are used for comparisons of signed integers and the terms “above” and “below” are used for unsigned integers.

Because a particular state of the status flags can sometimes be interpreted in two ways, two mnemonics are defined for some opcodes. For example, the CMOVA (conditional move if above) instruction and the CMOVNBE (conditional move if not below or equal) instruction are alternate mnemonics for the opcode 0F 47H.

The CMOVcc instructions were introduced in P6 family processors; however, these instructions may not be supported by all IA-32 processors. Software can determine if the CMOVcc instructions are supported by checking the processor’s feature information with the CPUID instruction (see “CPUID—CPU Identification” in this chapter).

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

```
temp ← SRC
IF condition TRUE
```
THEN
    DEST ← temp;
FI;
ELSE
    IF (OperandSize = 32 and IA-32e mode active)
    THEN
        DEST[63:32] ← 0;
    FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.
Compatibly Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
## CMP—Compare Two Operands

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3C ib</td>
<td>CMP AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm8 with AL.</td>
</tr>
<tr>
<td>3D iw</td>
<td>CMP AX, imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm16 with AX.</td>
</tr>
<tr>
<td>3D id</td>
<td>CMP EAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm32 with EAX.</td>
</tr>
<tr>
<td>REX.w + 3D id</td>
<td>CMP RAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare imm32 sign-extended to 64-bits with RAX.</td>
</tr>
<tr>
<td>80 /7 ib</td>
<td>CMP r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm8 with r/m8.</td>
</tr>
<tr>
<td>REX + 80 /7 ib</td>
<td>CMP r/m8*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare imm8 with r/m8.</td>
</tr>
<tr>
<td>81 /7 iw</td>
<td>CMP r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm16 with r/m16.</td>
</tr>
<tr>
<td>81 /7 id</td>
<td>CMP r/m32, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm32 with r/m32.</td>
</tr>
<tr>
<td>REX.w + 81 /7 id</td>
<td>CMP r/m64, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare imm32 sign-extended to 64-bits with r/m64.</td>
</tr>
<tr>
<td>83 /7 ib</td>
<td>CMP r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm8 with r/m16.</td>
</tr>
<tr>
<td>83 /7 ib</td>
<td>CMP r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare imm8 with r/m32.</td>
</tr>
<tr>
<td>REX.w + 83 /7 ib</td>
<td>CMP r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare imm8 with r/m64.</td>
</tr>
<tr>
<td>3B ir</td>
<td>CMP r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r8 with r/m8.</td>
</tr>
<tr>
<td>REX + 3B ir</td>
<td>CMP r/m8*, r8*</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare r8 with r/m8.</td>
</tr>
<tr>
<td>39 ir</td>
<td>CMP r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r16 with r/m16.</td>
</tr>
<tr>
<td>39 ir</td>
<td>CMP r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r32 with r/m32.</td>
</tr>
<tr>
<td>REX.w + 39 ir</td>
<td>CMP r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare r64 with r/m64.</td>
</tr>
<tr>
<td>3A ir</td>
<td>CMP r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r/m8 with r8.</td>
</tr>
<tr>
<td>REX + 3A ir</td>
<td>CMP r8*, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare r/m8 with r8.</td>
</tr>
<tr>
<td>3B ir</td>
<td>CMP r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r/m16 with r16.</td>
</tr>
<tr>
<td>3B ir</td>
<td>CMP r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare r/m32 with r32.</td>
</tr>
<tr>
<td>REX.w + 3B ir</td>
<td>CMP r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare r/m64 with r64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
**Description**

Compares the first source operand with the second source operand and sets the status flags in the EFLAGS register according to the results. The comparison is performed by subtracting the second operand from the first operand and then setting the status flags in the same manner as the SUB instruction. When an immediate value is used as an operand, it is sign-extended to the length of the first operand.

The condition codes used by the Jcc, CMOVcc, and SETcc instructions are based on the results of a CMP instruction. Appendix B, “EFLAGS Condition Codes,” in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, shows the relationship of the status flags and the condition codes.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\text{temp} \leftarrow \text{SRC1} - \text{SignExtend(SRC2)}; \\
\text{ModifyStatusFlags; (* Modify status flags in the same manner as the SUB instruction*)}
\]

**Flags Affected**

The CF, OF, SF, ZF, AF, and PF flags are set according to the result.

**Protected Mode Exceptions**

- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (r, w)</td>
<td>ModRM:reg (w)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM:r/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>I</td>
<td>AL/AX/EAX/RAX</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-L

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
CMPPD—Compare Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F C2 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compare packed double-precision floating-point values in xmm2/m128 and xmm1 using imm8 as comparison predicate.</td>
</tr>
<tr>
<td>CMPPD xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG C2 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed double-precision floating-point values in xmm3/m128 and xmm2 using bits 4:0 of imm8 as a comparison predicate.</td>
</tr>
<tr>
<td>VCMPPD xmm1, xmm2, xmm3/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG C2 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed double-precision floating-point values in ymm3/m256 and ymm2 using bits 4:0 of imm8 as a comparison predicate.</td>
</tr>
<tr>
<td>VCMPPD ymm1, ymm2, ymm3/m256, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD compare of the packed double-precision floating-point values in the source operand (second operand) and the destination operand (first operand) and returns the results of the comparison to the destination operand. The comparison predicate operand (third operand) specifies the type of comparison performed on each of the pairs of packed values. The result of each comparison is a quadword mask of all 1s (comparison true) or all 0s (comparison false).

128-bit Legacy SSE version: The first source and destination operand (first operand) is an XMM register. The second source operand (second operand) can be an XMM register or 128-bit memory location. The comparison predicate operand is an 8-bit immediate, bits 2:0 of the immediate define the type of comparison to be performed (see Table 3-7). Bits 7:3 of the immediate is reserved. Bits (VLMAX-1:1) of the corresponding YMM destination register remain unchanged. Two comparisons are performed with results written to bits 127:0 of the destination operand.
The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate an exception, because a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Note that the processors with “CPUID.1H:ECX.AVX =0” do not implement the greater-than, greater-than-or-equal, not-greater-than, and not-greater-than-or-equal relations. These comparisons can be made either by using the inverse relationship (that is, use the “not-less-than-or-equal” to make a “greater-than” comparison) or by using software emulation. When using software emulation, the program must
swap the operands (copying registers when necessary to protect the data that will now be in the destination), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-7 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPPD instruction, for processors with "CPUID.1H:ECX.AVX =0". See Table 3-8. Compiler should treat reserved Imm8 values as illegal syntax.

The greater-than relations that the processor does not implement, require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.)

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Enhanced Comparison Predicate for VEX-Encoded VCMPD

VEX.128 encoded version: The first source operand (second operand) is an XMM register. The second source operand (third operand) can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the destination YMM register are zeroed. Two comparisons are performed with results written to bits 127:0 of the destination operand.

VEX.256 encoded version: The first source operand (second operand) is a YMM register. The second source operand (third operand) can be a YMM register or a 256-bit memory location. The destination operand (first operand) is a YMM register. Four comparisons are performed with results written to the destination operand.

The comparison predicate operand is an 8-bit immediate:

- For instructions encoded using the VEX prefix, bits 4:0 define the type of comparison to be performed (see Table 3-9). Bits 5 through 7 of the immediate are reserved.
### Table 3-9. Comparison Predicate for VCMPPD and VCMPPS Instructions

<table>
<thead>
<tr>
<th>Predicate</th>
<th>imm8 Value</th>
<th>Description</th>
<th>Result: A is 1st Operand, B is 2nd Operand</th>
<th>Signals #IA on QNAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>EQ_OQ (EQ)</td>
<td>0H</td>
<td>Equal (ordered, non-signaling)</td>
<td>False False True False</td>
<td>No</td>
</tr>
<tr>
<td>LT_OS (LT)</td>
<td>1H</td>
<td>Less-than (ordered, signaling)</td>
<td>False True False False</td>
<td>Yes</td>
</tr>
<tr>
<td>LE_OS (LE)</td>
<td>2H</td>
<td>Less-than-or-equal (ordered, signaling)</td>
<td>False True True False</td>
<td>Yes</td>
</tr>
<tr>
<td>UNORD_Q (UNORD)</td>
<td>3H</td>
<td>Unordered (non-signaling)</td>
<td>False False False True</td>
<td>No</td>
</tr>
<tr>
<td>NEQ_UQ (NEQ)</td>
<td>4H</td>
<td>Not-equal (unordered, non-signaling)</td>
<td>True True False True</td>
<td>No</td>
</tr>
<tr>
<td>NLT_US (NLT)</td>
<td>5H</td>
<td>Not-less-than (unordered, signaling)</td>
<td>True False True True</td>
<td>Yes</td>
</tr>
<tr>
<td>NLE_US (NLE)</td>
<td>6H</td>
<td>Not-less-than-or-equal (unordered, signaling)</td>
<td>True False False True</td>
<td>Yes</td>
</tr>
<tr>
<td>ORD_Q (ORD)</td>
<td>7H</td>
<td>Ordered (non-signaling)</td>
<td>True True True False</td>
<td>No</td>
</tr>
<tr>
<td>EQ_UQ</td>
<td>8H</td>
<td>Equal (unordered, non-signaling)</td>
<td>False False True True</td>
<td>No</td>
</tr>
<tr>
<td>NGE_US (NGE)</td>
<td>9H</td>
<td>Not-greater-than-or-equal (unordered, signaling)</td>
<td>False True False True</td>
<td>Yes</td>
</tr>
<tr>
<td>NGT_US (NGT)</td>
<td>AH</td>
<td>Not-greater-than (unordered, signaling)</td>
<td>False True True False</td>
<td>Yes</td>
</tr>
<tr>
<td>FALSE_O (FALSE)</td>
<td>BH</td>
<td>False (ordered, non-signaling)</td>
<td>False False False False</td>
<td>No</td>
</tr>
<tr>
<td>NEQ_OQ</td>
<td>CH</td>
<td>Not-equal (ordered, non-signaling)</td>
<td>True True False False</td>
<td>No</td>
</tr>
<tr>
<td>GE_OS (GE)</td>
<td>DH</td>
<td>Greater-than-or-equal (ordered, signaling)</td>
<td>True False True False</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Table 3-9. Comparison Predicate for VCMPPD and VCMPPS Instructions (Contd.)

<table>
<thead>
<tr>
<th>Predicate</th>
<th>imm8 Value</th>
<th>Description</th>
<th>Result: A Is 1st Operand, B Is 2nd Operand</th>
<th>Signals #IA on QNAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>GT_OS</td>
<td>EH</td>
<td>Greater-than (ordered, signaling)</td>
<td>A &gt; B False, A &lt; B False, A = B False, Unordered Yes</td>
<td></td>
</tr>
<tr>
<td>TRUE_UQ(TRUE)</td>
<td>FH</td>
<td>True (unordered, non-signaling)</td>
<td>A &gt; B True, A &lt; B True, A = B True, Unordered No</td>
<td></td>
</tr>
<tr>
<td>EQ_OS</td>
<td>10H</td>
<td>Equal (ordered, signaling)</td>
<td>A &gt; B False, A &lt; B False, A = B True, Unordered Yes</td>
<td></td>
</tr>
<tr>
<td>LT_OQ</td>
<td>11H</td>
<td>Less-than (ordered, nonsignaling)</td>
<td>A &gt; B False, A &lt; B True, A = B False, Unordered No</td>
<td></td>
</tr>
<tr>
<td>LE_OQ</td>
<td>12H</td>
<td>Less-than-or-equal (ordered, nonsignaling)</td>
<td>A &gt; B False, A &lt; B True, A = B True, Unordered No</td>
<td></td>
</tr>
<tr>
<td>UNORD_S</td>
<td>13H</td>
<td>Unordered (signaling)</td>
<td>A &gt; B False, A &lt; B False, A = B False, Unordered Yes</td>
<td></td>
</tr>
<tr>
<td>NEQ_US</td>
<td>14H</td>
<td>Not-equal (unordered, signaling)</td>
<td>A &gt; B True, A &lt; B True, A = B True, Unordered Yes</td>
<td></td>
</tr>
<tr>
<td>NLT_UQ</td>
<td>15H</td>
<td>Not-less-than (unordered, nonsignaling)</td>
<td>A &gt; B True, A &lt; B False, A = B True, Unordered No</td>
<td></td>
</tr>
<tr>
<td>NLE_UQ</td>
<td>16H</td>
<td>Not-less-than-or-equal (unordered, nonsignaling)</td>
<td>A &gt; B True, A &lt; B False, A = B True, Unordered No</td>
<td></td>
</tr>
<tr>
<td>ORD_S</td>
<td>17H</td>
<td>Ordered (signaling)</td>
<td>A &gt; B True, A &lt; B True, A = B True, Unordered Yes</td>
<td></td>
</tr>
<tr>
<td>EQ_US</td>
<td>18H</td>
<td>Equal (unordered, signaling)</td>
<td>A &gt; B False, A &lt; B False, A = B True, Unordered Yes</td>
<td></td>
</tr>
<tr>
<td>NGE_UQ</td>
<td>19H</td>
<td>Not-greater-than-or-equal (unordered, nonsignaling)</td>
<td>A &gt; B False, A &lt; B True, A = B True, Unordered No</td>
<td></td>
</tr>
<tr>
<td>NGT_UQ</td>
<td>1AH</td>
<td>Not-greater-than (unordered, nonsignaling)</td>
<td>A &gt; B False, A &lt; B True, A = B True, Unordered No</td>
<td></td>
</tr>
<tr>
<td>FALSE_OS</td>
<td>1BH</td>
<td>False (ordered, signaling)</td>
<td>A &gt; B False, A &lt; B False, A = B False, Unordered Yes</td>
<td></td>
</tr>
<tr>
<td>NEQ_OS</td>
<td>1CH</td>
<td>Not-equal (ordered, signaling)</td>
<td>A &gt; B True, A &lt; B True, A = B False, Unordered Yes</td>
<td></td>
</tr>
</tbody>
</table>
Processors with "CPUID.1H:ECX.AVX =1" implement the full complement of 32 predicates shown in Table 3-9, software emulation is no longer needed. Compilers and assemblers may implement the following three-operand pseudo-ops in addition to the four-operand VCMPPD instruction. See Table 3-10, where the notations of reg1, reg2, and reg3 represent either XMM registers or YMM registers. Compiler should treat reserved Imm8 values as illegal syntax. Alternately, intrinsics can map the pseudo-ops to pre-defined constants to support a simpler intrinsic interface.

### Table 3-9. Comparison Predicate for VCMPPD and VCMPPS Instructions (Contd.)

<table>
<thead>
<tr>
<th>Predicate</th>
<th>imm8 Value</th>
<th>Description</th>
<th>Result: A Is 1st Operand, B Is 2nd Operand</th>
<th>Signals</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GE_OQ</td>
<td>1DH</td>
<td>Greater-than-or-equal (ordered, non-signaling)</td>
<td>True</td>
<td>False</td>
<td>True</td>
</tr>
<tr>
<td>GT_OQ</td>
<td>1EH</td>
<td>Greater-than (ordered, non-signaling)</td>
<td>True</td>
<td>False</td>
<td>False</td>
</tr>
<tr>
<td>TRUE_US</td>
<td>1FH</td>
<td>True (unordered, signaling)</td>
<td>True</td>
<td>True</td>
<td>True</td>
</tr>
</tbody>
</table>

### Table 3-10. Pseudo-Op and VCMPPD Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPPD Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMPEQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 0</td>
</tr>
<tr>
<td>VCMPLTPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 1</td>
</tr>
<tr>
<td>VCMPLEQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 2</td>
</tr>
<tr>
<td>VCMPUNORDPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 3</td>
</tr>
<tr>
<td>VCMPNLEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 4</td>
</tr>
<tr>
<td>VCMPSLEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 5</td>
</tr>
<tr>
<td>VCMPSLEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 6</td>
</tr>
<tr>
<td>VCMPSLEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 7</td>
</tr>
<tr>
<td>VCMP_EQ_UQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 8</td>
</tr>
<tr>
<td>VCMPSLEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 9</td>
</tr>
<tr>
<td>VCMPSLEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 0AH</td>
</tr>
<tr>
<td>VCMPSLEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 0BH</td>
</tr>
<tr>
<td>VCMPSLEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 0CH</td>
</tr>
</tbody>
</table>

**NOTES:**
1. If either operand A or B is a NAN.
Table 3-10. Pseudo-Op and VCMPPD Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPPD Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMPGEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 0DH</td>
</tr>
<tr>
<td>VCMPGTPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 0EH</td>
</tr>
<tr>
<td>VCMPTUEPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 0FH</td>
</tr>
<tr>
<td>VCMEQ_OSPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 10H</td>
</tr>
<tr>
<td>VCMLT_OQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 11H</td>
</tr>
<tr>
<td>VCMLE_OQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 12H</td>
</tr>
<tr>
<td>VCMPNORDER_SPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 13H</td>
</tr>
<tr>
<td>VCMPNSEQ_USPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 14H</td>
</tr>
<tr>
<td>VCMPPNLT_UQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 15H</td>
</tr>
<tr>
<td>VCMPPNLE_UQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 16H</td>
</tr>
<tr>
<td>VCMPPORD_SPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 17H</td>
</tr>
<tr>
<td>VCMPEQ_USPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 18H</td>
</tr>
<tr>
<td>VCMNPSEQ_UQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 19H</td>
</tr>
<tr>
<td>VCMPPNGT_UQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 1AH</td>
</tr>
<tr>
<td>VCMPPFALSP_TRUE_OSPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 1BH</td>
</tr>
<tr>
<td>VCMPPSEQ_USPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 1CH</td>
</tr>
<tr>
<td>VCMPPGE_OQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 1DH</td>
</tr>
<tr>
<td>VCMPPGT_OQPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 1EH</td>
</tr>
<tr>
<td>VCMPPTRUE_USPD reg1, reg2, reg3</td>
<td>VCMPPD reg1, reg2, reg3, 1FH</td>
</tr>
</tbody>
</table>

Operation

CASE (COMPARISON PREDICATE) OF
0: OP3 ← EQ_OQ; OP5 ← EQ_OQ;
1: OP3 ← LT_OS; OP5 ← LT_OS;
2: OP3 ← LE_OS; OP5 ← LE_OS;
3: OP3 ← UNORD_Q; OP5 ← UNORD_Q;
4: OP3 ← NEQ_UQ; OP5 ← NEQ_UQ;
5: OP3 ← NLT_US; OP5 ← NLT_US;
6: OP3 ← NLE_US; OP5 ← NLE_US;
7: OP3 ← ORD_Q; OP5 ← ORD_Q;
8: OP5 ← EQ_UQ;
9: OP5 ← NGE_US;
CMPPD (128-bit Legacy SSE version)
CMPPD (VEX 128 encoded version)
CMPPD—Compare Packed Double-Precision Floating-Point Values

ELSE DEST[127:64] ← 0000000000000000H; Fl;
DEST[VLMAX-1:128] ← 0

VCMPPD (VEX.256 encoded version)
CMPO ← SRC1[63:0] OP5 SRC2[63:0];
CMP1 ← SRC1[127:64] OP5 SRC2[127:64];
CMP3 ← SRC1[255:192] OP5 SRC2[255:192];
IF CMP0 = TRUE
THEN DEST[63:0] ← FFFFFFFFFFFFFFFFH;
ELSE DEST[63:0] ← 0000000000000000H; Fl;
IF CMP1 = TRUE
THEN DEST[127:64] ← FFFFFFFFFFFFFFFFH;
ELSE DEST[127:64] ← 0000000000000000H; Fl;
IF CMP2 = TRUE
THEN DEST[191:128] ← FFFFFFFFFFFFFFFFH;
ELSE DEST[191:128] ← 0000000000000000H; Fl;
IF CMP3 = TRUE
THEN DEST[255:192] ← FFFFFFFFFFFFFFFFH;
ELSE DEST[255:192] ← 0000000000000000H; Fl;

Intel C/C++ Compiler Intrinsic Equivalents
CMPPD for equality: __m128d _mm_cmpeq_pd(__m128d a, __m128d b)
CMPPD for less-than: __m128d _mm_cmplt_pd(__m128d a, __m128d b)
CMPPD for less-than-or-equal: __m128d _mm_cmple_pd(__m128d a, __m128d b)
CMPPD for greater-than: __m128d _mm_cmpgt_pd(__m128d a, __m128d b)
CMPPD for greater-than-or-equal: __m128d _mm_cmpge_pd(__m128d a, __m128d b)
CMPPD for inequality: __m128d _mm_cmpneq_pd(__m128d a, __m128d b)
CMPPD for not-less-than: __m128d _mm_cmpnlt_pd(__m128d a, __m128d b)
CMPPD for not-greater-than: __m128d _mm_cmpngt_pd(__m128d a, __m128d b)
CMPPD for not-greater-than-or-equal: __m128d _mm_cmpnle_pd(__m128d a, __m128d b)
CMPPD for ordered: __m128d _mm_cmpord_pd(__m128d a, __m128d b)
CMPPD for unordered: __m128d _mm_cmpunord_pd(__m128d a, __m128d b)
CMPPD for not-less-than-or-equal: __m128d _mm_cmpnle_pd(__m128d a, __m128d b)
VCMPDD: __m256 _mm256_cmp_pd(__m256 a, __m256 b, const int imm)
VCMPDD: __m128 _mm_cmp_pd(__m128 a, __m128 b, const int imm)
SIMD Floating-Point Exceptions
Invalid if SNaN operand and invalid if QNaN and predicate as listed in above table, Denormal.

Other Exceptions
See Exceptions Type 2.
CMPPS—Compare Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF C2 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE</td>
<td>Compare packed single-precision floating-point values in xmm2/mem and xmm1 using imm8 as comparison predicate.</td>
</tr>
<tr>
<td>CMPPS xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG C2 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed single-precision floating-point values in xmm3/m128 and xmm2 using bits 4:0 of imm8 as a comparison predicate.</td>
</tr>
<tr>
<td>VCMPPS xmm1, xmm2, xmm3/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG C2 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed single-precision floating-point values in ymm3/m256 and ymm2 using bits 4:0 of imm8 as a comparison predicate.</td>
</tr>
<tr>
<td>VCMPPS ymm1, ymm2, ymm3/m256, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD compare of the packed single-precision floating-point values in the source operand (second operand) and the destination operand (first operand) and returns the results of the comparison to the destination operand. The comparison predicate operand (third operand) specifies the type of comparison performed on each of the pairs of packed values. The result of each comparison is a doubleword mask of all 1s (comparison true) or all 0s (comparison false).

128-bit Legacy SSE version: The first source and destination operand (first operand) is an XMM register. The second source operand (second operand) can be an XMM register or 128-bit memory location. The comparison predicate operand is an 8-bit immediate, bits 2:0 of the immediate define the type of comparison to be performed (see Table 3-7). Bits 7:3 of the immediate is reserved. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged. Four comparisons are performed with results written to bits 127:0 of the destination operand.
The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate a fault, because a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Note that processors with “CPUID.1H:ECX.AVX =0” do not implement the “greater-than”, “greater-than-or-equal”, “not-greater than”, and “not-greater-than-or-equal relations” predicates. These comparisons can be made either by using the inverse relationship (that is, use the “not-less-than-or-equal” to make a “greater-than” comparison) or by using software emulation. When using software emulation, the program must swap the operands (copying registers when necessary to protect the data that will now be in the destination), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-7 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPPS instruction, for processors with “CPUID.1H:ECX.AVX =0”. See Table 3-11. Compiler should treat reserved Imm8 values as illegal syntax.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
VEX.128 encoded version: The first source operand (second operand) is an XMM register. The second source operand (third operand) can be an XMM register or a 128-bit memory location. Bits (VLMAX-1:128) of the destination YMM register are zeroed. Four comparisons are performed with results written to bits 127:0 of the destination operand.

VEX.256 encoded version: The first source operand (second operand) is a YMM register. The second source operand (third operand) can be a YMM register or a 256-bit memory location. The destination operand (first operand) is a YMM register. Eight comparisons are performed with results written to the destination operand.

The comparison predicate operand is an 8-bit immediate:

- For instructions encoded using the VEX prefix, bits 4:0 define the type of comparison to be performed (see Table 3-9). Bits 5 through 7 of the immediate are reserved.

Processors with “CPUID.1H:ECX.AVX =1” implement the full complement of 32 predicates shown in Table 3-9, software emulation is no longer needed. Compilers and assemblers may implement the following three-operand pseudo-ops in addition to the four-operand VCMPPS instruction. See Table 3-12, where the notation of reg1 and reg2 represent either XMM registers or YMM registers. Compiler should treat reserved Imm8 values as illegal syntax. Alternately, intrinsics can map the pseudo-ops to pre-defined constants to support a simpler intrinsic interface.

**Table 3-12. Pseudo-Op and VCMPPS Implementation**

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPPS Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMPEQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 0</td>
</tr>
<tr>
<td>VCMPLTPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 1</td>
</tr>
<tr>
<td>VCMPLEPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 2</td>
</tr>
<tr>
<td>VCMMPUNORDPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 3</td>
</tr>
<tr>
<td>VCMPNEQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 4</td>
</tr>
<tr>
<td>VCMPNLTPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 5</td>
</tr>
<tr>
<td>VCMPNLEPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 6</td>
</tr>
<tr>
<td>VCMPORDPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 7</td>
</tr>
<tr>
<td>VCMPEQ_UQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 8</td>
</tr>
<tr>
<td>VCMPNGEPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 9</td>
</tr>
<tr>
<td>VCMPNGTPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 0AH</td>
</tr>
<tr>
<td>VCMMPALSEPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 0BH</td>
</tr>
<tr>
<td>VCMPEQ_OQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 0CH</td>
</tr>
<tr>
<td>VCMPGEPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 0DH</td>
</tr>
<tr>
<td>VCMPGTPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 0EH</td>
</tr>
</tbody>
</table>
Table 3-12. Pseudo-Op and VCMPPS Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPPS Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMPTRUEEPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 0FH</td>
</tr>
<tr>
<td>VCMPEQ_OSPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 10H</td>
</tr>
<tr>
<td>VCMPLT_OQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 11H</td>
</tr>
<tr>
<td>VCMPEQ_OQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 12H</td>
</tr>
<tr>
<td>VCMPPNORD_SPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 13H</td>
</tr>
<tr>
<td>VCMPPNEQ_USPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 14H</td>
</tr>
<tr>
<td>VCMPNLT_UQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 15H</td>
</tr>
<tr>
<td>VCMPNLE_UQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 16H</td>
</tr>
<tr>
<td>VCMPOORD_SPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 17H</td>
</tr>
<tr>
<td>VCMPEQ_USPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 18H</td>
</tr>
<tr>
<td>VCMPPGE_UQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 19H</td>
</tr>
<tr>
<td>VCMPPNGT_UQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 1AH</td>
</tr>
<tr>
<td>VCMPPFALSE_OSPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 1BH</td>
</tr>
<tr>
<td>VCMPPNEQ_OSPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 1CH</td>
</tr>
<tr>
<td>VCMPPGE_OQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 1DH</td>
</tr>
<tr>
<td>VCMPPGT_OQPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 1EH</td>
</tr>
<tr>
<td>VCMPTRUE_USPS reg1, reg2, reg3</td>
<td>VCMPPS reg1, reg2, reg3, 1FH</td>
</tr>
</tbody>
</table>

**Operation**

CASE (COMPARISON PREDICATE) OF

0: OP3 ← EQ_OQ; OP5 ← EQ_OQ;
1: OP3 ← LT_OS; OP5 ← LT_OS;
2: OP3 ← LE_OS; OP5 ← LE_OS;
3: OP3 ← UNORD_Q; OP5 ← UNORD_Q;
4: OP3 ← NEQ_UQ; OP5 ← NEQ_UQ;
5: OP3 ← NLT_US; OP5 ← NLT_US;
6: OP3 ← NLE_US; OP5 ← NLE_US;
7: OP3 ← ORD_Q; OP5 ← ORD_Q;
8: OP5 ← EQ_UQ;
9: OP5 ← NGE_US;
10: OP5 ← NGT_US;
11: OP5 ← FALSE_OQ;
12: OP5 ← NEQ_OQ;
13: OP5 ← GE_OS;
14: OP5 ← GT_OS;
CMPPS—Compare Packed Single-Precision Floating-Point Values

15: OP5 ← TRUE_UQ;
16: OP5 ← EQ_OS;
17: OP5 ← LT_OQ;
18: OP5 ← LE_OQ;
19: OP5 ← UNORD_S;
20: OP5 ← NEQ_US;
21: OP5 ← NLT_UQ;
22: OP5 ← NLE_UQ;
23: OP5 ← ORD_S;
24: OP5 ← EQ_US;
25: OP5 ← NGE_UQ;
26: OP5 ← NGT_UQ;
27: OP5 ← FALSE_OS;
28: OP5 ← NEQ_OS;
29: OP5 ← GE_OQ;
30: OP5 ← GT_OQ;
31: OP5 ← TRUE_US;
DEFAULT: Reserved

EASC;

CMPPS (128-bit Legacy SSE version)
CMPO ← SRC1[31:0] OP3 SRC2[31:0];
CMP1 ← SRC1[63:32] OP3 SRC2[63:32];
CMP2 ← SRC1[95:64] OP3 SRC2[95:64];
CMP3 ← SRC1[127:96] OP3 SRC2[127:96];
IF CMP0 = TRUE
  THEN DEST[31:0] ← FFFFFFFFH;
  ELSE DEST[31:0] ← 000000000H; Fl;
IF CMP1 = TRUE
  THEN DEST[63:32] ← FFFFFFFFH;
  ELSE DEST[63:32] ← 000000000H; Fl;
IF CMP2 = TRUE
  THEN DEST[95:64] ← FFFFFFFFH;
  ELSE DEST[95:64] ← 000000000H; Fl;
IF CMP3 = TRUE
  THEN DEST[127:96] ← FFFFFFFFH;
  ELSE DEST[127:96] ← 000000000H; Fl;
DEST[VLMAX-1:128] (Unmodified)

VCMPSS (VEX.128 encoded version)
CMPO ← SRC1[31:0] OP5 SRC2[31:0];
CMP1 ← SRC1[63:32] OP5 SRC2[63:32];
CMP2 ← SRC1[95:64] OP5 SRC2[95:64];
INSTRUCTION SET REFERENCE, A-L

CMP3 ← SRC1[127:96] OP5 SRC2[127:96];
IF CMP0 = TRUE
    THEN DEST[31:0] ← FFFFFFFFH;
    ELSE DEST[31:0] ← 000000000H; Fl;
IF CMP1 = TRUE
    THEN DEST[63:32] ← FFFFFFFFH;
    ELSE DEST[63:32] ← 000000000H; Fl;
IF CMP2 = TRUE
    THEN DEST[95:64] ← FFFFFFFFH;
    ELSE DEST[95:64] ← 000000000H; Fl;
IF CMP3 = TRUE
    THEN DEST[127:96] ← FFFFFFFFH;
    ELSE DEST[127:96] ← 000000000H; Fl;
DEST[VLMAX-1:128] ← 0

VCMPPS (VEX.256 encoded version)
CMP0 ← SRC1[31:0] OP5 SRC2[31:0];
CMP1 ← SRC1[63:32] OP5 SRC2[63:32];
CMP2 ← SRC1[95:64] OP5 SRC2[95:64];
CMP3 ← SRC1[127:96] OP5 SRC2[127:96];
CMP4 ← SRC1[159:128] OP5 SRC2[159:128];
CMP5 ← SRC1[191:160] OP5 SRC2[191:160];
CMP6 ← SRC1[223:192] OP5 SRC2[223:192];
CMP7 ← SRC1[255:224] OP5 SRC2[255:224];
IF CMP0 = TRUE
    THEN DEST[31:0] ← FFFFFFFFH;
    ELSE DEST[31:0] ← 000000000H; Fl;
IF CMP1 = TRUE
    THEN DEST[63:32] ← FFFFFFFFH;
    ELSE DEST[63:32] ← 000000000H; Fl;
IF CMP2 = TRUE
    THEN DEST[95:64] ← FFFFFFFFH;
    ELSE DEST[95:64] ← 000000000H; Fl;
IF CMP3 = TRUE
    THEN DEST[127:96] ← FFFFFFFFH;
    ELSE DEST[127:96] ← 000000000H; Fl;
IF CMP4 = TRUE
    THEN DEST[159:128] ← FFFFFFFFH;
    ELSE DEST[159:128] ← 000000000H; Fl;
IF CMP5 = TRUE
    THEN DEST[191:160] ← FFFFFFFFH;
    ELSE DEST[191:160] ← 000000000H; Fl;
IF CMP6 = TRUE
    THEN DEST[223:192] ← FFFFFFFFH;
    ELSE DEST[223:192] ← 000000000H; Fl;
IF CMP7 = TRUE
    THEN DEST[255:224] ← FFFFFFFFH;
    ELSE DEST[255:224] ← 000000000H; Fl;
THEN DEST[223:192] ← FFFFFFFFH;
ELSE DEST[223:192] ← 000000000H; Fl;
IF CMP7 = TRUE
THEN DEST[255:224] ← FFFFFFFFH;
ELSE DEST[255:224] ← 000000000H; Fl;

**Intel C/C++ Compiler Intrinsic Equivalents**

CMPPS for equality:  __m128 _mm_cmpeq_ps(__m128 a, __m128 b)
CMPPS for less-than:  __m128 _mm_cmplt_ps(__m128 a, __m128 b)
CMPPS for less-than-or-equal:  __m128 _mm_cmpale_ps(__m128 a, __m128 b)
CMPPS for greater-than:  __m128 _mm_cmpgt_ps(__m128 a, __m128 b)
CMPPS for greater-than-or-equal:  __m128 _mm_cmpge_ps(__m128 a, __m128 b)
CMPPS for inequality:  __m128 _mm_cmpneq_ps(__m128 a, __m128 b)
CMPPS for not-less-than:  __m128 _mm_cmpnlt_ps(__m128 a, __m128 b)
CMPPS for not-greater-than:  __m128 _mm_cmpngt_ps(__m128 a, __m128 b)
CMPPS for not-greater-than-or-equal:  __m128 _mm_cmpnge_ps(__m128 a, __m128 b)
CMPPS for ordered:  __m128 _mm_cmpord_ps(__m128 a, __m128 b)
CMPPS for unordered:  __m128 _mm_cmpunord_ps(__m128 a, __m128 b)
VCMPPS:  __m256 _mm256_cmp_ps(__m256 a, __m256 b, const int imm)
VCMPPS:  __m128 _mm_cmp_ps(__m128 a, __m128 b, const int imm)

**SIMD Floating-Point Exceptions**

Invalid if SNaN operand and invalid if QNaN and predicate as listed in above table,
Denormal.

**Other Exceptions**

See Exceptions Type 2.
## CMPS/CMPSB/CMPSW/CMPSD/CMPSQ—Compare String Operands

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A6</td>
<td>CMPS m8, m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare byte at address DS:(E)SI with byte at address ES:(E)DI; For 64-bit mode compare byte at address (R</td>
</tr>
<tr>
<td>A7</td>
<td>CMPS m16, m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare word at address DS:(E)SI with word at address ES:(E)DI; For 64-bit mode compare word at address (R</td>
</tr>
<tr>
<td>A7</td>
<td>CMPS m32, m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare dword at address DS:(E)SI at dword at address ES:(E)DI; For 64-bit mode compare dword at address (R</td>
</tr>
<tr>
<td>REX.w + A7</td>
<td>CMPS m64, m64</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compares quadword at address (R</td>
</tr>
<tr>
<td>A6</td>
<td>CMPSB</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, compare byte at address DS:(E)SI with byte at address ES:(E)DI; For 64-bit mode compare byte at address (R</td>
</tr>
</tbody>
</table>
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CMPS/CMPSB/CMPSW/CMPSD/CMPSQ—Compare String Operands

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INSTRUCTION SET REFERENCE, A-L

Op/En Instruction Op/ 64-Bit Comp/ Description
En Mode Leg Mode

A7 CMPSW NP Valid Valid For legacy mode, compare
word at address DS:(E)SI
with word at address
ES:(E)DI; For 64-bit mode
compare word at address
(RE)SI with word at address
(RE)DI. The status flags are
set accordingly.

A7 CMPSD NP Valid Valid For legacy mode, compare
dword at address DS:(E)SI
with dword at address
ES:(E)DI; For 64-bit mode
compare dword at address
(RE)SI with dword at
address (RE)DI. The status
flags are set accordingly.

REX.W + A7 CMPSQ NP Valid N.E. Compares quadword at
address (RE)SI with
quadword at address (RE)DI
and sets the status flags
accordingly.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Compares the byte, word, doubleword, or quadword specified with the first source operand with the byte, word, doubleword, or quadword specified with the second source operand and sets the status flags in the EFLAGS register according to the results.

Both source operands are located in memory. The address of the first source operand is read from DS:SI, DS:ESI or RSI (depending on the address-size attribute of the instruction is 16, 32, or 64, respectively). The address of the second source operand is read from ES:DI, ES:EDI or RDI (again depending on the address-size attribute of the instruction is 16, 32, or 64). The DS segment may be overridden with a segment override prefix, but the ES segment cannot be overridden.

At the assembly-code level, two forms of this instruction are allowed: the "explicit-operands" form and the "no-operands" form. The explicit-operands form (specified with the CMPS mnemonic) allows the two source operands to be specified explicitly.
Here, the source operands should be symbols that indicate the size and location of the source values. This explicit-operand form is provided to allow documentation. However, note that the documentation provided by this form can be misleading. That is, the source operand symbols must specify the correct type (size) of the operands (bytes, words, or doublewords, quadwords), but they do not have to specify the correct location. Locations of the source operands are always specified by the DS:(E)SI (or RSI) and ES:(E)DI (or RDI) registers, which must be loaded correctly before the compare string instruction is executed.

The no-operands form provides “short forms” of the byte, word, and doubleword versions of the CMPS instructions. Here also the DS:(E)SI (or RSI) and ES:(E)DI (or RDI) registers are assumed by the processor to specify the location of the source operands. The size of the source operands is selected with the mnemonic: CMPSB (byte comparison), CMPSW (word comparison), CMPSD (doubleword comparison), or CMPSQ (quadword comparison using REX.W).

After the comparison, the (E/R)SI and (E/R)DI registers increment or decrement automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E/R)SI and (E/R)DI register increment; if the DF flag is 1, the registers decrement.) The registers increment or decrement by 1 for byte operations, by 2 for word operations, 4 for doubleword operations. If operand size is 64, RSI and RDI registers increment by 8 for quadword operations.

The CMPS, CMPSB, CMPSW, CMPSD, and CMPSQ instructions can be preceded by the REP prefix for block comparisons. More often, however, these instructions will be used in a LOOP construct that takes some action based on the setting of the status flags before the next comparison is made. See “REP/REPE/REPZ /REPNE/REPNZ—Repeat String Operation Prefix” in Chapter 4 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B, for a description of the REP prefix.

In 64-bit mode, the instruction’s default address size is 64 bits, 32 bit address size is supported using the prefix 67H. Use of the REX.W prefix promotes doubleword operation to 64 bits (see CMPSQ). See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

temp ← SRC1 - SRC2;
SetStatusFlags(temp);

IF (64-Bit Mode)
    THEN
        IF (Byte comparison)
            THEN IF DF = 0
                THEN
                    (R|E)SI ← (R|E)SI + 1;
                    (R|E)DI ← (R|E)DI + 1;
                ELSE
INSTRUCTION SET REFERENCE, A-L

CMPS/CMPSB/CMPSW/CMPSD/CMPSQ—Compare String Operands

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(R|E)SI ← (R|E)SI – 1;
(R|E)DI ← (R|E)DI – 1;
FI;
ELSE IF (Word comparison)
THEN IF DF = 0
THEN
(R|E)SI ← (R|E)SI + 2;
(R|E)DI ← (R|E)DI + 2;
ELSE
(R|E)SI ← (R|E)SI – 2;
(R|E)DI ← (R|E)DI – 2;
FI;
ELSE IF (Doubleword comparison)
THEN IF DF = 0
THEN
(R|E)SI ← (R|E)SI + 4;
(R|E)DI ← (R|E)DI + 4;
ELSE
(R|E)SI ← (R|E)SI – 4;
(R|E)DI ← (R|E)DI – 4;
FI;
ELSE (* Quadword comparison *)
THEN IF DF = 0
(R|E)SI ← (R|E)SI + 8;
(R|E)DI ← (R|E)DI + 8;
ELSE
(R|E)SI ← (R|E)SI – 8;
(R|E)DI ← (R|E)DI – 8;
FI;
FI;
ELSE (* Non-64-bit Mode *)
IF (byte comparison)
THEN IF DF = 0
THEN
(E)SI ← (E)SI + 1;
(E)DI ← (E)DI + 1;
ELSE
(E)SI ← (E)SI – 1;
(E)DI ← (E)DI – 1;
FI;
ELSE IF (Word comparison)
THEN IF DF = 0
(E)SI ← (E)SI + 2;
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\[(E)DI \leftarrow (E)DI + 2;\]
ELSE
\[(E)SI \leftarrow (E)SI - 2;\]
\[(E)DI \leftarrow (E)DI - 2;\]
FI;
ELSE (* Doubleword comparison *)
THEN IF DF = 0
\[(E)SI \leftarrow (E)SI + 4;\]
\[(E)DI \leftarrow (E)DI + 4;\]
ELSE
\[(E)SI \leftarrow (E)SI - 4;\]
\[(E)DI \leftarrow (E)DI - 4;\]
FI;
FI;
FI;

Flags Affected
The CF, OF, SF, ZF, AF, and PF flags are set according to the temporary result of the comparison.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
CMPSD—Compare Scalar Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 OF C2 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compare low double-precision floating-point value in xmm2/m64 and xmm1 using imm8 as comparison predicate.</td>
</tr>
<tr>
<td>CMPSD xmm1, xmm2/m64, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F.WIG C2 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare low double precision floating-point value in xmm3/m64 and xmm2 using bits 4:0 of imm8 as comparison predicate.</td>
</tr>
<tr>
<td>VCMPSD xmm1, xmm2, xmm3/m64, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Compares the low double-precision floating-point values in the source operand (second operand) and the destination operand (first operand) and returns the results of the comparison to the destination operand. The comparison predicate operand (third operand) specifies the type of comparison performed. The comparison result is a quadword mask of all 1s (comparison true) or all 0s (comparison false).

128-bit Legacy SSE version: The first source and destination operand (first operand) is an XMM register. The second source operand (second operand) can be an XMM register or 64-bit memory location. The comparison predicate operand is an 8-bit immediate, bits 2:0 of the immediate define the type of comparison to be performed (see Table 3-7). Bits 7:3 of the immediate is reserved. Bits (VMAX-1:64) of the corresponding YMM destination register remain unchanged.

The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate a fault, because a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Note that processors with "CPUID.1H:ECX.AVX =0" do not implement the "greater-than", "greater-than-or-equal", "not-greater than", and "not-greater-than-or-equal"
relations” predicates. These comparisons can be made either by using the inverse relationship (that is, use the “not-less-than-or-equal” to make a “greater-than” comparison) or by using software emulation. When using software emulation, the program must swap the operands (copying registers when necessary to protect the data that will now be in the destination operand), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-7 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPSD instruction, for processors with "CPUID.1H:ECX.AVX =0". See Table 3-13. Compiler should treat reserved Imm8 values as illegal syntax.

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 0</td>
</tr>
<tr>
<td>CMPLTSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 1</td>
</tr>
<tr>
<td>CMPSLESD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 2</td>
</tr>
<tr>
<td>CMPUNORDSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 3</td>
</tr>
<tr>
<td>CMPNEQSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 4</td>
</tr>
<tr>
<td>CMPNLTSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 5</td>
</tr>
<tr>
<td>CMPNLESDD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 6</td>
</tr>
<tr>
<td>CMPORDSD xmm1, xmm2</td>
<td>CMPSD xmm1,xmm2, 7</td>
</tr>
</tbody>
</table>

The greater-than relations not implemented in the processor require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.)

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Enhanced Comparison Predicate for VEX-Encoded VCMPSD**

VEX.128 encoded version: The first source operand (second operand) is an XMM register. The second source operand (third operand) can be an XMM register or a 64-bit memory location. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

The comparison predicate operand is an 8-bit immediate:

- For instructions encoded using the VEX prefix, bits 4:0 define the type of comparison to be performed (see Table 3-9). Bits 5 through 7 of the immediate are reserved.

Processors with "CPUID.1H:ECX.AVX =1" implement the full complement of 32 predicates shown in Table 3-9, software emulation is no longer needed. Compilers and
assemblers may implement the following three-operand pseudo-ops in addition to
the four-operand VCMPSD instruction. See Table 3-14, where the notations of reg1
reg2, and reg3 represent either XMM registers or YMM registers. Compiler should
treat reserved Imm8 values as illegal syntax. Alternately, intrinsics can map the
pseudo-ops to pre-defined constants to support a simpler intrinsic interface.

### Table 3-14. Pseudo-Op and VCMPSD Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPSD Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMPEQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 0</td>
</tr>
<tr>
<td>VCMLTSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 1</td>
</tr>
<tr>
<td>VCMPLESD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 2</td>
</tr>
<tr>
<td>VCMUNORDSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 3</td>
</tr>
<tr>
<td>VCMPEQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 4</td>
</tr>
<tr>
<td>VCMPLTSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 5</td>
</tr>
<tr>
<td>VCMPLESD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 6</td>
</tr>
<tr>
<td>VCMORDSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 7</td>
</tr>
<tr>
<td>VCMPEQ_UQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 8</td>
</tr>
<tr>
<td>VCMPNGESD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 9</td>
</tr>
<tr>
<td>VCMPNGTSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 0AH</td>
</tr>
<tr>
<td>VCMFALSED reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 0BH</td>
</tr>
<tr>
<td>VCMPEQ_OQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 0CH</td>
</tr>
<tr>
<td>VCMGESD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 0DH</td>
</tr>
<tr>
<td>VCMGTSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 0EH</td>
</tr>
<tr>
<td>VCMTRUESD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 0FH</td>
</tr>
<tr>
<td>VCMPEQ_OSSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 10H</td>
</tr>
<tr>
<td>VCMPLT_OQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 11H</td>
</tr>
<tr>
<td>VCMPLE_OQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 12H</td>
</tr>
<tr>
<td>VCMUNORD_OQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 13H</td>
</tr>
<tr>
<td>VCMPEQ_USSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 14H</td>
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<tr>
<td>VCMPLT_UQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 15H</td>
</tr>
<tr>
<td>VCMPLE_UQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 16H</td>
</tr>
<tr>
<td>VCMORD_UQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 17H</td>
</tr>
<tr>
<td>VCMPEQ_USSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 18H</td>
</tr>
<tr>
<td>VCMPNEQ_UQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 19H</td>
</tr>
<tr>
<td>VCMPNLT_UQSD reg1, reg2, reg3</td>
<td>VCMPSD regl, reg2, reg3, 1AH</td>
</tr>
</tbody>
</table>
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Table 3-14. Pseudo-Op and VCMPSD Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPSD Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMPFALSE_OSSD reg1, reg2, reg3</td>
<td>VCMPSD reg1, reg2, reg3, 1BH</td>
</tr>
<tr>
<td>VCMPNEQ_OSSD reg1, reg2, reg3</td>
<td>VCMPSD reg1, reg2, reg3, 1CH</td>
</tr>
<tr>
<td>VCMMPGE_OQSD reg1, reg2, reg3</td>
<td>VCMPSD reg1, reg2, reg3, 1DH</td>
</tr>
<tr>
<td>VCMPGT_OQSD reg1, reg2, reg3</td>
<td>VCMPSD reg1, reg2, reg3, 1EH</td>
</tr>
<tr>
<td>VCMPTURE_USSD reg1, reg2, reg3</td>
<td>VCMPSD reg1, reg2, reg3, IFH</td>
</tr>
</tbody>
</table>

**Operation**

**CASE (COMPARISON PREDICATE) OF**

0: OP3 ← EQ_OQ; OP5 ← EQ_OQ;
1: OP3 ← LT_OS; OP5 ← LT_OS;
2: OP3 ← LE_OS; OP5 ← LE_OS;
3: OP3 ← UNORD_Q; OP5 ← UNORD_Q;
4: OP3 ← NEQ_UQ; OP5 ← NEQ_UQ;
5: OP3 ← NLT_US; OP5 ← NLT_US;
6: OP3 ← NLE_US; OP5 ← NLE_US;
7: OP3 ← ORD_Q; OP5 ← ORD_Q;
8: OP5 ← EQ_UQ;
9: OP5 ← NGE_US;
10: OP5 ← NGT_US;
11: OP5 ← FALSE_OQ;
12: OP5 ← NEQ_OQ;
13: OP5 ← GE_OS;
14: OP5 ← GT_OS;
15: OP5 ← TRUE_UQ;
16: OP5 ← EQ_OS;
17: OP5 ← LT_OQ;
18: OP5 ← LE_OQ;
19: OP5 ← UNORD_S;
20: OP5 ← NEQ_US;
21: OP5 ← NLT_UQ;
22: OP5 ← NLE_UQ;
23: OP5 ← ORD_S;
24: OP5 ← EQ_US;
25: OP5 ← NGE_UQ;
26: OP5 ← NGT_UQ;
27: OP5 ← FALSE_OS;
28: OP5 ← NEQ_OS;
INSTRUCTION SET REFERENCE, A-L

29: OP5 ← GE_OQ;
30: OP5 ← GT_OQ;
31: OP5 ← TRUE_US;
DEFAULT: Reserved
ESAC;

CMPSD (128-bit Legacy SSE version)
CMP0 ← DEST[63:0] OP3 SRC[63:0];
IF CMP0 = TRUE
THEN DEST[63:0] ← FFFFFFFFFFFFFFFFFFHF;
ELSE DEST[63:0] ← 0000000000000000H; FI;
DEST[VLMAX-1:64] (Unmodified)

VCMPSD (VEX.128 encoded version)
CMP0 ← SRC1[63:0] OP5 SRC2[63:0];
IF CMP0 = TRUE
THEN DEST[63:0] ← FFFFFFFFFFFFFFFFFFHF;
ELSE DEST[63:0] ← 0000000000000000H; FI;
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
CMPSD for equality: __m128d _mm_cmpeq_sd(__m128d a, __m128d b)
CMPSD for less-than: __m128d _mm_cmplt_sd(__m128d a, __m128d b)
CMPSD for less-than-or-equal: __m128d _mm_cmple_sd(__m128d a, __m128d b)
CMPSD for greater-than: __m128d _mm_cmpgt_sd(__m128d a, __m128d b)
CMPSD for greater-than-or-equal: __m128d _mm_cmpge_sd(__m128d a, __m128d b)
CMPSD for inequality: __m128d _mm_cmpneq_sd(__m128d a, __m128d b)
CMPSD for not-less-than: __m128d _mm_cmpnlt_sd(__m128d a, __m128d b)
CMPSD for not-less-than-or-equal: __m128d _mm_cmpnle_sd(__m128d a, __m128d b)
CMPSD for ordered: __m128d _mm_cmpord_sd(__m128d a, __m128d b)
CMPSD for unordered: __m128d _mm_cmpunord_sd(__m128d a, __m128d b)
CMPSD for not-greater-than: __m128d _mm_cmpngt_sd(__m128d a, __m128d b)
CMPSD for not-greater-than-or-equal: __m128d _mm_cmpnge_sd(__m128d a, __m128d b)
VCMPSD: __m128 _mm_cmpeq_sd(__m128 a, __m128 b, const int imm)

SIMD Floating-Point Exceptions
Invalid if SNaN operand, Invalid if QNaN and predicate as listed in above table,
Denormal.
**Other Exceptions**

See Exceptions Type 3.
CMPSS—Compare Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F C2 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE</td>
<td>Compare low single-precision floating-point value in xmm2/m32 and xmm1 using imm8 as comparison predicate.</td>
</tr>
<tr>
<td>CMPSS xmm1, xmm2/m32, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.WIG C2 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare low single precision floating-point value in xmm3/m32 and xmm2 using bits 4:0 of imm8 as comparison predicate.</td>
</tr>
<tr>
<td>VCMPS S xmm1, xmm2, xmm3/m32, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:reg/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:reg/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

**Description**

Compares the low single-precision floating-point values in the source operand (second operand) and the destination operand (first operand) and returns the results of the comparison to the destination operand. The comparison predicate operand (third operand) specifies the type of comparison performed. The comparison result is a doubleword mask of all 1s (comparison true) or all 0s (comparison false).

128-bit Legacy SSE version: The first source and destination operand (first operand) is an XMM register. The second source operand (second operand) can be an XMM register or 64-bit memory location. The comparison predicate operand is an 8-bit immediate, bits 2:0 of the immediate define the type of comparison to be performed (see Table 3-7). Bits 7:3 of the immediate is reserved. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

The unordered relationship is true when at least one of the two source operands being compared is a NaN; the ordered relationship is true when neither source operand is a NaN.

A subsequent computational instruction that uses the mask result in the destination operand as an input operand will not generate a fault, since a mask of all 0s corresponds to a floating-point value of +0.0 and a mask of all 1s corresponds to a QNaN.

Note that processors with "CPUID.1H:ECX.AVX =0” do not implement the “greater-than”, “greater-than-or-equal”, “not-greater-than”, and “not-greater-than-or-equal
relations” predicates. These comparisons can be made either by using the inverse relationship (that is, use the “not-less-than-or-equal” to make a “greater-than” comparison) or by using software emulation. When using software emulation, the program must swap the operands (copying registers when necessary to protect the data that will now be in the destination operand), and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in Table 3-7 under the heading Emulation.

Compilers and assemblers may implement the following two-operand pseudo-ops in addition to the three-operand CMPSS instruction, for processors with "CPUID.1H:ECX.AVX =0". See Table 3-15. Compiler should treat reserved Imm8 values as illegal syntax.

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPSS Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 0</td>
</tr>
<tr>
<td>CMPLTSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 1</td>
</tr>
<tr>
<td>CMPLESS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 2</td>
</tr>
<tr>
<td>CMPUNORDSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 3</td>
</tr>
<tr>
<td>CMPNEQSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 4</td>
</tr>
<tr>
<td>CMPNLTSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 5</td>
</tr>
<tr>
<td>CMPNLESS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 6</td>
</tr>
<tr>
<td>CMPORDSS xmm1, xmm2</td>
<td>CMPSS xmm1, xmm2, 7</td>
</tr>
</tbody>
</table>

The greater-than relations not implemented in the processor require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.)

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Enhanced Comparison Predicate for VEX-Encoded VCMPSD**

VEX.128 encoded version: The first source operand (second operand) is an XMM register. The second source operand (third operand) can be an XMM register or a 32-bit memory location. Bits (VLMAX-1:128) of the destination YMM register are zeroed. The comparison predicate operand is an 8-bit immediate:

- For instructions encoded using the VEX prefix, bits 4:0 define the type of comparison to be performed (see Table 3-9). Bits 5 through 7 of the immediate are reserved.

Processors with "CPUID.1H:ECX.AVX =1" implement the full complement of 32 predicates shown in Table 3-9, software emulation is no longer needed. Compilers and
assemblers may implement the following three-operand pseudo-ops in addition to the four-operand VCMPSS instruction. See Table 3-16, where the notations of reg1 reg2, and reg3 represent either XMM registers or YMM registers. Compiler should treat reserved Imm8 values as illegal syntax. Alternately, intrinsics can map the pseudo-ops to pre-defined constants to support a simpler intrinsic interface.

**Table 3-16. Pseudo-Op and VCMPSS Implementation**

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPSS Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMPEQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 0</td>
</tr>
<tr>
<td>VCMPLTSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 1</td>
</tr>
<tr>
<td>VCMPELESS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 2</td>
</tr>
<tr>
<td>VCMPPUNORDSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 3</td>
</tr>
<tr>
<td>VCMPPNEQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 4</td>
</tr>
<tr>
<td>VCMPPNLTSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 5</td>
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<tr>
<td>VCMPPNLESS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 6</td>
</tr>
<tr>
<td>VCMPPORDSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 7</td>
</tr>
<tr>
<td>VCMPEQ_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 8</td>
</tr>
<tr>
<td>VCMPPNGE_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 9</td>
</tr>
<tr>
<td>VCMPPNLT_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 10H</td>
</tr>
<tr>
<td>VCMPPNGE_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 0AH</td>
</tr>
<tr>
<td>VCMPPNEQ_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 0BH</td>
</tr>
<tr>
<td>VCMPPNGT_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 0CH</td>
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<tr>
<td>VCMPPGTSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 0DH</td>
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<tr>
<td>VCMPPGTSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 0EH</td>
</tr>
<tr>
<td>VCMPPORD_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 0FH</td>
</tr>
<tr>
<td>VCMPPNGN_UQSS reg1, reg2, reg3</td>
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</tr>
<tr>
<td>VCMPPNL_G_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 11H</td>
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<tr>
<td>VCMPPNEQ_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 12H</td>
</tr>
<tr>
<td>VCMPPORD_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 13H</td>
</tr>
<tr>
<td>VCMPPNGT_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 14H</td>
</tr>
<tr>
<td>VCMPPGTSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 15H</td>
</tr>
<tr>
<td>VCMPPORD_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 16H</td>
</tr>
<tr>
<td>VCMPPORD_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 17H</td>
</tr>
<tr>
<td>VCMPPNGT_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 18H</td>
</tr>
<tr>
<td>VCMPPNGT_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 19H</td>
</tr>
<tr>
<td>VCMPPORD_UQSS reg1, reg2, reg3</td>
<td>VCMPSS reg1, reg2, reg3, 1AH</td>
</tr>
</tbody>
</table>
Table 3-16. Pseudo-Op and VCMPPSS Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>CMPSS Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMPFALSE_OSSS reg1, reg2, reg3</td>
<td>VCMPPSS reg1, reg2, reg3, 1BH</td>
</tr>
<tr>
<td>VCMPNEQ_OSSS reg1, reg2, reg3</td>
<td>VCMPPSS reg1, reg2, reg3, 1CH</td>
</tr>
<tr>
<td>VCMPGE_OQSS reg1, reg2, reg3</td>
<td>VCMPPSS reg1, reg2, reg3, 1DH</td>
</tr>
<tr>
<td>VCMPGT_OQSS reg1, reg2, reg3</td>
<td>VCMPPSS reg1, reg2, reg3, 1EH</td>
</tr>
<tr>
<td>VCMPTURE_USSS reg1, reg2, reg3</td>
<td>VCMPPSS reg1, reg2, reg3, 1FH</td>
</tr>
</tbody>
</table>

Operation

CASE (COMPARISON PREDICATE) OF
0: OP3 ← EQ_OQ; OP5 ← EQ_OQ;
1: OP3 ← LT_OS; OP5 ← LT_OS;
2: OP3 ← LE_OQ; OP5 ← LE_OQ;
3: OP3 ← UNORD_Q; OP5 ← UNORD_Q;
4: OP3 ← NEQ_UQ; OP5 ← NEQ_UQ;
5: OP3 ← NLT_US; OP5 ← NLT_US;
6: OP3 ← NLE_US; OP5 ← NLE_US;
7: OP3 ← ORD_Q; OP5 ← ORD_Q;
8: OP5 ← EQ_UQ;
9: OP5 ← NGE_US;
10: OP5 ← NGT_US;
11: OP5 ← FALSE_OQ;
12: OP5 ← NEQ_OQ;
13: OP5 ← GE_OQ;
14: OP5 ← GT_OQ;
15: OP5 ← TRUE_UQ;
16: OP5 ← EQ_OS;
17: OP5 ← LT_OQ;
18: OP5 ← LE_OQ;
19: OP5 ← UNORD_S;
20: OP5 ← NEQ_US;
21: OP5 ← NLT_UQ;
22: OP5 ← NLE_UQ;
23: OP5 ← ORD_S;
24: OP5 ← EQ_US;
25: OP5 ← NGE_UQ;
26: OP5 ← NGT_UQ;
27: OP5 ← FALSE_OS;
28: OP5 ← NEQ_OS;
29: OP5 ← GE_OQ;
30: OP5 ← GT_OQ;
3: OP5 ← TRUE_US;
    DEFAULT: Reserved
ESAC;

**CMPSS (128-bit Legacy SSE version)**

CMP0 ← DEST[31:0] OP3 SRC[31:0];
IF CMP0 = TRUE
    THEN DEST[31:0] ← FFFFFFFFH;
ELSE DEST[31:0] ← 00000000H; Fl;
DEST[VLMAX-1:32] (Unmodified)

**VCMPSS (VEX.128 encoded version)**

CMP0 ← SRC1[31:0] OP5 SRC2[31:0];
IF CMP0 = TRUE
    THEN DEST[31:0] ← FFFFFFFFH;
ELSE DEST[31:0] ← 00000000H; Fl;
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalents**

CMPSS for equality: __m128 _mm_cmpeq_ss(__m128 a, __m128 b)
CMPSS for less-than: __m128 _mm_cmlt_ss(__m128 a, __m128 b)
CMPSS for less-than-or-equal: __m128 _mm_cmlple_ss(__m128 a, __m128 b)
CMPSS for greater-than: __m128 _mm_cmpgt_ss(__m128 a, __m128 b)
CMPSS for greater-than-or-equal: __m128 _mm_cmpge_ss(__m128 a, __m128 b)
CMPSS for inequality: __m128 _mm_cmpneq_ss(__m128 a, __m128 b)
CMPSS for not-less-than: __m128 _mm_cmpnlt_ss(__m128 a, __m128 b)
CMPSS for not-greater-than: __m128 _mm_cmpngt_ss(__m128 a, __m128 b)
CMPSS for not-greater-than-or-equal: __m128 _mm_cmpngle_ss(__m128 a, __m128 b)
CMPSS for ordered: __m128 _mm_cmpord_ss(__m128 a, __m128 b)
CMPSS for unordered: __m128 _mm_cmpunord_ss(__m128 a, __m128 b)
CMPSS for not-less-than-or-equal: __m128 _mm_cmpnle_ss(__m128 a, __m128 b)
VCMPSS: __m128 _mm_cmp_ss(__m128 a, __m128 b, const int imm)

**SIMD Floating-Point Exceptions**

Invalid if SNaN operand, Invalid if QNaN and predicate as listed in above table,
Denormal.
Other Exceptions
See Exceptions Type 3.
CMPXCHG—Compare and Exchange

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F B0/r</td>
<td>CMPXCHG r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid*</td>
<td>Compare AL with r/m8. If equal, ZF is set and r8 is loaded into r/m8. Else, clear ZF and load r/m8 into AL.</td>
</tr>
<tr>
<td>REX + 0F B0/r</td>
<td>CMPXCHG r/m8**, r8</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare AL with r/m8. If equal, ZF is set and r8 is loaded into r/m8. Else, clear ZF and load r/m8 into AL.</td>
</tr>
<tr>
<td>0F B1/r</td>
<td>CMPXCHG r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid*</td>
<td>Compare AX with r/m16. If equal, ZF is set and r16 is loaded into r/m16. Else, clear ZF and load r/m16 into AX.</td>
</tr>
<tr>
<td>0F B1/r</td>
<td>CMPXCHG r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid*</td>
<td>Compare EAX with r/m32. If equal, ZF is set and r32 is loaded into r/m32. Else, clear ZF and load r/m32 into EAX.</td>
</tr>
<tr>
<td>REX.w + 0F B1/r</td>
<td>CMPXCHG r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare RAX with r/m64. If equal, ZF is set and r64 is loaded into r/m64. Else, clear ZF and load r/m64 into RAX.</td>
</tr>
</tbody>
</table>

NOTES:
* See the IA-32 Architecture Compatibility section below.
** In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRMreg (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Compares the value in the AL, AX, EAX, or RAX register with the first operand (destination operand). If the two values are equal, the second operand (source operand) is loaded into the destination operand. Otherwise, the destination operand is loaded into the AL, AX, EAX or RAX register. RAX register is available only in 64-bit mode.
This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically. To simplify the interface to the processor’s bus, the destination operand receives a write cycle without regard to the result of the comparison. The destination operand is written back if the comparison fails; otherwise, the source operand is written into the destination. (The processor never produces a locked read without also producing a locked write.)

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**IA-32 Architecture Compatibility**

This instruction is not supported on Intel processors earlier than the Intel486 processors.

**Operation**

(* Accumulator = AL, AX, EAX, or RAX depending on whether a byte, word, doubleword, or quadword comparison is being performed *)

IF accumulator = DEST
    THEN
        ZF ← 1;
        DEST ← SRC;
    ELSE
        ZF ← 0;
        accumulator ← DEST;
FI;

**Flags Affected**

The ZF flag is set if the values in the destination operand and register AL, AX, or EAX are equal; otherwise it is cleared. The CF, PF, AF, SF, and OF flags are set according to the results of the comparison operation.

**Protected Mode Exceptions**

#GP(0) If the destination is located in a non-writable segment.
    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.
INSTRUCTION SET REFERENCE, A-L

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
CMPXCHG8B/CMPXCHG16B—Compare and Exchange Bytes

Description

Compares the 64-bit value in EDX:EAX (or 128-bit value in RDX:RAX if operand size is 128 bits) with the operand (destination operand). If the values are equal, the 64-bit value in ECX:EBX (or 128-bit value in RCX:RBX) is stored in the destination operand. Otherwise, the value in the destination operand is loaded into EDX:EAX (or RDX:RAX). The destination operand is an 8-byte memory location (or 16-byte memory location if operand size is 128 bits). For the EDX:EAX and ECX:EBX register pairs, EDX and ECX contain the high-order 32 bits and EAX and EBX contain the low-order 32 bits of a 64-bit value. For the RDX:RAX and RCX:RBX register pairs, RDX and RCX contain the high-order 64 bits and RAX and RBX contain the low-order 64 bits of a 128-bit value.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically. To simplify the interface to the processor’s bus, the destination operand receives a write cycle without regard to the result of the comparison. The destination operand is written back if the comparison fails; otherwise, the source operand is written into the destination. (The processor never produces a locked read without also producing a locked write.)

In 64-bit mode, default operation size is 64 bits. Use of the REX.W prefix promotes operation to 128 bits. Note that CMPXCHG16B requires that the destination (memory) operand be 16-byte aligned. See the summary chart at the beginning of this section for encoding data and limits. For information on the CPUID flag that indicates CMPXCHG16B, see page 3-214.

NOTES:

*See IA-32 Architecture Compatibility section below.
IA-32 Architecture Compatibility
This instruction encoding is not supported on Intel processors earlier than the Pentium processors.

Operation

IF (64-Bit Mode and OperandSize = 64)
  THEN
    IF (RDX:RAX = DEST)
      ZF ← 1;
      DEST ← RCX:RBX;
    ELSE
      ZF ← 0;
      RDX:RAX ← DEST;
    FI
  ELSE
    IF (EDX:EAX = DEST)
      ZF ← 1;
      DEST ← ECX:EBX;
    ELSE
      ZF ← 0;
      EDX:EAX ← DEST;
    FI;
  FI;

Flags Affected
The ZF flag is set if the destination operand and EDX:EAX are equal; otherwise it is cleared. The CF, PF, AF, SF, and OF flags are unaffected.

Protected Mode Exceptions

#UD If the destination is not a memory operand.
#GP(0) If the destination is located in a non-writable segment.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
Real-Address Mode Exceptions

#UD If the destination operand is not a memory location.
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual-8086 Mode Exceptions

#UD If the destination operand is not a memory location.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
If memory operand for CMPXCHG16B is not aligned on a 16-byte boundary.
If CPUID.01H:ECX.CMPXCHG16B[bit 13] = 0.
#UD If the destination operand is not a memory location.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
COMISD—Compare Scalar Ordered Double-Precision Floating-Point Values and Set EFLAGS

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 2F /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compare low double-precision floating-point values in xmm1 and xmm2/mem64 and set the EFLAGS flags accordingly.</td>
</tr>
<tr>
<td>COMISD xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.66.0F.WIG 2F /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare low double precision floating-point values in xmm1 and xmm2/mem64 and set the EFLAGS flags accordingly.</td>
</tr>
<tr>
<td>VCOMISD xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Compares the double-precision floating-point values in the low quadwords of operand 1 (first operand) and operand 2 (second operand), and sets the ZF, PF, and CF flags in the EFLAGS register according to the result (unordered, greater than, less than, or equal). The OF, SF and AF flags in the EFLAGS register are set to 0. The unordered result is returned if either source operand is a NaN (QNaN or SNaN).

Operand 1 is an XMM register; operand 2 can be an XMM register or a 64 bit memory location.

The COMISD instruction differs from the UCOMISD instruction in that it signals a SIMD floating-point invalid operation exception (#I) when a source operand is either a QNaN or SNaN. The UCOMISD instruction signals an invalid numeric exception only if a source operand is an SNaN.

The EFLAGS register is not updated if an unmasked SIMD floating-point exception is generated.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.
INSTRUCTION SET REFERENCE, A-L

Operation

RESULT ← OrderedCompare(DEST[63:0] <> SRC[63:0])
(* Set EFLAGS *) CASE (RESULT) OF
  UNORDERED: ZF,PF,CF ← 111;
  GREATER_THAN: ZF,PF,CF ← 000;
  LESS_THAN: ZF,PF,CF ← 001;
  EQUAL: ZF,PF,CF ← 100;
ESAC;
OF, AF, SF ← 0;

Intel C/C++ Compiler Intrinsic Equivalents

int _mm_comieq_sd (__m128d a, __m128d b)
int _mm_comilt_sd (__m128d a, __m128d b)
int _mm_comile SD (__m128d a, __m128d b)
int _mm_comigt_sd (__m128d a, __m128d b)
int _mm_comige_sd (__m128d a, __m128d b)
int _mm_comineq_sd (__m128d a, __m128d b)

SIMD Floating-Point Exceptions

Invalid (if SNaN or QNaN operands), Denormal.

Other Exceptions

See Exceptions Type 3; additionally

#UD If VEX.vvvv != 1111B.
COMISS—Compare Scalar Ordered Single-Precision Floating-Point Values and Set EFLAGS

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 2F /r COMISS xmm1, xmm2/m32</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Compare low single-precision floating-point values in xmm1 and xmm2/mem32 and set the EFLAGS flags accordingly.</td>
</tr>
<tr>
<td>VEX.LIG.0F 2F.WIG /r VCOMISS xmm1, xmm2/m32</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare low single precision floating-point values in xmm1 and xmm2/mem32 and set the EFLAGS flags accordingly.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

COMISS compares the single-precision floating-point values in the low doublewords of operand 1 (first operand) and operand 2 (second operand), and sets the ZF, PF, and CF flags in the EFLAGS register according to the result (unordered, greater than, less than, or equal). The OF, SF, and AF flags in the EFLAGS register are set to 0. The unordered result is returned if either source operand is a NaN (QNaN or SNaN).

Operand 1 is an XMM register; Operand 2 can be an XMM register or a 32 bit memory location.

The COMISS instruction differs from the UCOMISS instruction in that it signals a SIMD floating-point invalid operation exception (#I) when a source operand is either a QNaN or SNaN. The UCOMISS instruction signals an invalid numeric exception only if a source operand is an SNaN.

The EFLAGS register is not updated if an unmasked SIMD floating-point exception is generated.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvv is reserved and must be 1111b, otherwise instructions will #UD.
INSTRUCTION SET REFERENCE, A-L

Operation
RESULT ← OrderedCompare(SRC1[31:0] <> SRC2[31:0]) {
(* Set EFLAGS *) CASE (RESULT) OF
  UNORDERED: ZF,PF,CF ← 111;
  GREATER_THAN: ZF,PF,CF ← 000;
  LESS_THAN: ZF,PF,CF ← 001;
  EQUAL: ZF,PF,CF ← 100;
ESAC;
OF,AF,SF ← 0; }

Intel C/C++ Compiler Intrinsic Equivalents
int _mm_comieq_ss (__m128 a, __m128 b)
int _mm_comilt_ss (__m128 a, __m128 b)
int _mm_comile_ss (__m128 a, __m128 b)
int _mm_comigt_ss (__m128 a, __m128 b)
int _mm_comige_ss (__m128 a, __m128 b)
int _mm_comineq_ss (__m128 a, __m128 b)

SIMD Floating-Point Exceptions
Invalid (if SNaN or QNaN operands), Denormal.

Other Exceptions
See Exceptions Type 3; additionally
#UD If VEX.vvvv != 1111B.
CPUID—CPU Identification

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F A2</td>
<td>CPUID</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Returns processor identification and feature information to the EAX, EBX, ECX, and EDX registers, as determined by input entered in EAX (in some cases, ECX as well).</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

The ID flag (bit 21) in the EFLAGS register indicates support for the CPUID instruction. If a software procedure can set and clear this flag, the processor executing the procedure supports the CPUID instruction. This instruction operates the same in non-64-bit modes and 64-bit mode.

CPUID returns processor identification and feature information in the EAX, EBX, ECX, and EDX registers. The instruction’s output is dependent on the contents of the EAX register upon execution (in some cases, ECX as well). For example, the following pseudocode loads EAX with 00H and causes CPUID to return a Maximum Return Value and the Vendor Identification String in the appropriate registers:

```assembly
MOV EAX, 00H
CPUID
```

Table 3-17 shows information returned, depending on the initial value loaded into the EAX register. Table 3-18 shows the maximum CPUID input value recognized for each family of IA-32 processors on which CPUID is implemented.

Two types of information are returned: basic and extended function information. If a value entered for CPUID.EAX is higher than the maximum input value for basic or extended function for that processor then the data for the highest basic information leaf is returned. For example, using the Intel Core i7 processor, the following is true:

- CPUID.EAX = 05H (* Returns MONITOR/MWAIT leaf. *)
- CPUID.EAX = 0AH (* Returns Architectural Performance Monitoring leaf. *)
- CPUID.EAX = 0BH (* Returns Extended Topology Enumeration leaf. *)

1. On Intel 64 processors, CPUID clears the high 32 bits of the RAX/RBX/RCX/RDX registers in all modes.
CPUID.EAX = 0CH (* INVALID: Returns the same information as CPUID.EAX = 0BH. *)
CPUID.EAX = 80000008H (* Returns linear/physical address size data. *)
CPUID.EAX = 8000000AH (* INVALID: Returns same information as CPUID.EAX = 0BH. *)

If a value entered for CPUID.EAX is less than or equal to the maximum input value and the leaf is not supported on that processor then 0 is returned in all the registers. For example, using the Intel Core i7 processor, the following is true:

CPUID.EAX = 07H (*Returns EAX=EBX=ECX=EDX=0. *)

When CPUID returns the highest basic leaf information as a result of an invalid input EAX value, any dependence on input ECX value in the basic leaf is honored.

CPUID can be executed at any privilege level to serialize instruction execution. Serializing instruction execution guarantees that any modifications to flags, registers, and memory for previous instructions are completed before the next instruction is fetched and executed.

See also:

“Serializing Instructions” in Chapter 8, “Multiple-Processor Management,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

“Caching Translation Information” in Chapter 4, “Paging,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>0H</strong></td>
<td><strong>Basic CPUID Information</strong></td>
</tr>
<tr>
<td>EAX</td>
<td>Maximum Input Value for Basic CPUID Information (see Table 3-18)</td>
</tr>
<tr>
<td>EBX</td>
<td>“Genu”</td>
</tr>
<tr>
<td>ECX</td>
<td>“intel”</td>
</tr>
<tr>
<td>EDX</td>
<td>“inel”</td>
</tr>
<tr>
<td><strong>01H</strong></td>
<td><strong>Version Information: Type, Family, Model, and Stepping ID (see Figure 3-5)</strong></td>
</tr>
<tr>
<td>EAX</td>
<td>Bits 07-00: Brand Index</td>
</tr>
<tr>
<td>EBX</td>
<td>Bits 15-08: CLFLUSH line size (Value × 8 = cache line size in bytes)</td>
</tr>
<tr>
<td></td>
<td>Bits 23-16: Maximum number of addressable IDs for logical processors in this physical package*.</td>
</tr>
<tr>
<td></td>
<td>Bits 31-24: Initial APIC ID</td>
</tr>
<tr>
<td>ECX</td>
<td>Feature Information (see Figure 3-6 and Table 3-20)</td>
</tr>
<tr>
<td>EDX</td>
<td>Feature Information (see Figure 3-7 and Table 3-21)</td>
</tr>
</tbody>
</table>
### Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NOTES:</strong></td>
<td>* The nearest power-of-2 integer that is not smaller than EBX[23:16] is the number of unique initial APIC IDs reserved for addressing different logical processors in a physical package. This field is only valid if CPUID.1.EDX.HTT[bit 28]= 1.</td>
</tr>
<tr>
<td>02H</td>
<td>EAX Cache and TLB Information (see Table 3-22)</td>
</tr>
<tr>
<td></td>
<td>EBX Cache and TLB Information</td>
</tr>
<tr>
<td></td>
<td>ECX Cache and TLB Information</td>
</tr>
<tr>
<td></td>
<td>EDX Cache and TLB Information</td>
</tr>
<tr>
<td>03H</td>
<td>EAX Reserved.</td>
</tr>
<tr>
<td></td>
<td>EBX Reserved.</td>
</tr>
<tr>
<td></td>
<td>ECX Bits 00-31 of 96 bit processor serial number. (Available in Pentium III processor only; otherwise, the value in this register is reserved.)</td>
</tr>
<tr>
<td></td>
<td>EDX Bits 32-63 of 96 bit processor serial number. (Available in Pentium III processor only; otherwise, the value in this register is reserved.)</td>
</tr>
<tr>
<td></td>
<td><strong>NOTES:</strong> Processor serial number (PSN) is not supported in the Pentium 4 processor or later. On all models, use the PSN flag (returned using CPUID) to check for PSN support before accessing the feature.</td>
</tr>
<tr>
<td></td>
<td>See AP-485, Intel Processor Identification and the CPUID Instruction (Order Number 241618) for more information on PSN.</td>
</tr>
<tr>
<td></td>
<td>CPUID leaves &gt; 3 &lt; 80000000 are visible only when IA32_MISC_ENABLE.BOOT_NT4[bit 22] = 0 (default).</td>
</tr>
<tr>
<td><strong>Deterministic Cache Parameters Leaf</strong></td>
<td></td>
</tr>
<tr>
<td>04H</td>
<td><strong>NOTES:</strong> Leaf 04H output depends on the initial value in ECX. See also: *INPUT EAX = 4: Returns Deterministic Cache Parameters for each level on page 3-224.</td>
</tr>
<tr>
<td></td>
<td>EAX Bits 04-00: Cache Type Field</td>
</tr>
<tr>
<td></td>
<td>0 = Null - No more caches</td>
</tr>
<tr>
<td></td>
<td>1 = Data Cache</td>
</tr>
<tr>
<td></td>
<td>2 = Instruction Cache</td>
</tr>
<tr>
<td></td>
<td>3 = Unified Cache</td>
</tr>
<tr>
<td></td>
<td>4-31 = Reserved</td>
</tr>
</tbody>
</table>
### Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Bits 07-05: Cache Level (starts at 1)</td>
</tr>
<tr>
<td></td>
<td>Bit 08: Self Initializing cache level (does not need SW initialization)</td>
</tr>
<tr>
<td></td>
<td>Bit 09: Fully Associative cache</td>
</tr>
<tr>
<td></td>
<td>Bits 13-10: Reserved</td>
</tr>
<tr>
<td>EBX</td>
<td>Bits 21-12: P = Physical Line partitions*</td>
</tr>
<tr>
<td></td>
<td>Bits 31-22: W = Ways of associativity*</td>
</tr>
<tr>
<td>ECX</td>
<td>Bits 31-00: S = Number of Sets*</td>
</tr>
<tr>
<td>EDX</td>
<td>Bit 0: Write-Back Invalidate/Invalidate</td>
</tr>
<tr>
<td></td>
<td>0 = WBINVD/INVD from threads sharing this cache acts upon lower level caches for threads sharing this cache.</td>
</tr>
<tr>
<td></td>
<td>1 = WBINVD/INVD is not guaranteed to act upon lower level caches of non-originating threads sharing this cache.</td>
</tr>
<tr>
<td></td>
<td>Bit 1: Cache Inclusiveness</td>
</tr>
<tr>
<td></td>
<td>0 = Cache is not inclusive of lower cache levels.</td>
</tr>
<tr>
<td></td>
<td>1 = Cache is inclusive of lower cache levels.</td>
</tr>
<tr>
<td></td>
<td>Bit 2: Complex Cache Indexing</td>
</tr>
<tr>
<td></td>
<td>0 = Direct mapped cache.</td>
</tr>
<tr>
<td></td>
<td>1 = A complex function is used to index the cache, potentially using all address bits.</td>
</tr>
<tr>
<td></td>
<td>Bits 31-03: Reserved = 0</td>
</tr>
</tbody>
</table>

**NOTES:**

* Add one to the return value to get the result.

** The nearest power-of-2 integer that is not smaller than \((1 + \text{EAX}[25:14])\) is the number of unique initial APIC IDs reserved for addressing different logical processors sharing this cache.

*** The nearest power-of-2 integer that is not smaller than \((1 + \text{EAX}[31:26])\) is the number of unique Core IDs reserved for addressing different processor cores in a physical package. Core ID is a subset of bits of the initial APIC ID.

**** The returned value is constant for valid initial values in ECX. Valid ECX values start from 0.
### Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
</table>
| 05H               | EAX Bits 15-00: Smallest monitor-line size in bytes (default is processor’s monitor granularity)  
|                   | Bits 31-16: Reserved = 0  
|                   | EBX Bits 15-00: Largest monitor-line size in bytes (default is processor’s monitor granularity)  
|                   | Bits 31-16: Reserved = 0  
|                   | ECX Bit 00: Enumeration of Monitor-Mwait extensions (beyond EAX and EBX registers) supported  
|                   | Bit 01: Supports treating interrupts as break-event for MWAIT, even when interrupts disabled  
|                   | Bits 31 - 02: Reserved  
|                   | EDX Bits 03 - 00: Number of C0* sub C-states supported using MWAIT  
|                   | Bits 07 - 04: Number of C1* sub C-states supported using MWAIT  
|                   | Bits 11 - 08: Number of C2* sub C-states supported using MWAIT  
|                   | Bits 15 - 12: Number of C3* sub C-states supported using MWAIT  
|                   | Bits 19 - 16: Number of C4* sub C-states supported using MWAIT  
|                   | Bits 31 - 20: Reserved = 0  
|                   | **NOTE:**  
|                   | * The definition of C0 through C4 states for MWAIT extension are processor-specific C-states, not ACPI C-states. |

**Thermal and Power Management Leaf**

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
</table>
| 06H               | EAX Bit 00: Digital temperature sensor is supported if set  
|                   | Bit 01: Intel Turbo Boost Technology Available (see description of IA32_MISC_ENABLE[38]).  
|                   | Bit 02: ARAT. APIC-Timer-always-running feature is supported if set.  
|                   | Bit 03: Reserved  
|                   | Bit 04: PLN. Power limit notification controls are supported if set.  
|                   | Bit 05: ECMD. Clock modulation duty cycle extension is supported if set.  
|                   | Bit 06: PTM. Package thermal management is supported if set.  
|                   | Bits 31 - 07: Reserved  
|                   | EBX Bits 03 - 00: Number of Interrupt Thresholds in Digital Thermal Sensor  
|                   | Bits 31 - 04: Reserved |
### Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECX</td>
<td>Bit 00: Hardware Coordination Feedback Capability (Presence of IA32_MPERF and IA32_APERF). The capability to provide a measure of delivered processor performance (since last reset of the counters), as a percentage of expected processor performance at frequency specified in CPUID Brand String. Bits 02 - 01: Reserved = 0. Bit 03: The processor supports performance-energy bias preference if CPUID.06H:ECX.SETBH[bit 3] is set and it also implies the presence of a new architectural MSR called IA32__ENERGY_PERF_BIAS (1B0H). Bits 31 - 04: Reserved = 0.</td>
</tr>
<tr>
<td>EDX</td>
<td>Reserved = 0</td>
</tr>
</tbody>
</table>

**Structured Extended Feature Flags Enumeration Leaf** *(Output depends on ECX input value)*

<table>
<thead>
<tr>
<th>07H</th>
<th>EAX</th>
<th>Bits 31-00: Reports the maximum number of supported leaf 7 sub-leaves.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EBX</td>
<td>Bit 00: FSGSBASE. Supports RDQSBASE/RDGQSBASE/WQSBASE/WQGSBASE if 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 06: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 07: SMEP. Supports Supervisor Mode Execution Protection if 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 08: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 09: Supports Enhanced REP MOVSB/STOSB if 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 10: INVPCID. If 1, supports INVPCID instruction for system software that manages process-context identifiers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 31:11: Reserved</td>
</tr>
<tr>
<td></td>
<td>ECX</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>EDX</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Direct Cache Access Information Leaf**

<table>
<thead>
<tr>
<th>09H</th>
<th>EAX</th>
<th>Value of bits [31:0] of IA32_PLATFORM_DCA_CAP MSR (address 1F8H)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EBX</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>ECX</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>EDX</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Architectural Performance Monitoring Leaf**
### Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0AH EAX</td>
<td>Bits 07 - 00: Version ID of architectural performance monitoring</td>
</tr>
<tr>
<td></td>
<td>Bits 15- 08: Number of general-purpose performance monitoring counter per logical processor</td>
</tr>
<tr>
<td></td>
<td>Bits 23 - 16: Bit width of general-purpose, performance monitoring counter</td>
</tr>
<tr>
<td></td>
<td>Bits 31 - 24: Length of EBX bit vector to enumerate architectural performance monitoring events</td>
</tr>
<tr>
<td>EBX</td>
<td>Bit 00: Core cycle event not available if 1</td>
</tr>
<tr>
<td></td>
<td>Bit 01: Instruction retired event not available if 1</td>
</tr>
<tr>
<td></td>
<td>Bit 02: Reference cycles event not available if 1</td>
</tr>
<tr>
<td></td>
<td>Bit 03: Last-level cache reference event not available if 1</td>
</tr>
<tr>
<td></td>
<td>Bit 04: Last-level cache misses event not available if 1</td>
</tr>
<tr>
<td></td>
<td>Bit 05: Branch instruction retired event not available if 1</td>
</tr>
<tr>
<td></td>
<td>Bit 06: Branch mispredict retired event not available if 1</td>
</tr>
<tr>
<td></td>
<td>Bits 31 - 07: Reserved = 0</td>
</tr>
<tr>
<td>ECX</td>
<td>Reserved = 0</td>
</tr>
<tr>
<td>EDX</td>
<td>Bits 04 - 00: Number of fixed-function performance counters (if Version ID &gt; 1)</td>
</tr>
<tr>
<td></td>
<td>Bits 12- 05: Bit width of fixed-function performance counters (if Version ID &gt; 1)</td>
</tr>
<tr>
<td></td>
<td>Reserved = 0</td>
</tr>
</tbody>
</table>

**Extended Topology Enumeration Leaf**

<table>
<thead>
<tr>
<th>0BH EAX</th>
<th>NOTES:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Most of Leaf 0BH output depends on the initial value in ECX.</td>
</tr>
<tr>
<td></td>
<td>EDX output do not vary with initial value in ECX.</td>
</tr>
<tr>
<td></td>
<td>ECX[7:0] output always reflect initial value in ECX.</td>
</tr>
<tr>
<td></td>
<td>All other output value for an invalid initial value in ECX are 0.</td>
</tr>
<tr>
<td></td>
<td>Leaf 0BH exists if EBX[15:0] is not zero.</td>
</tr>
<tr>
<td>EBX</td>
<td>Bits 04-00: Number of bits to shift right on x2APIC ID to get a unique topology ID of the next level type*. All logical processors with the same next level ID share current level.</td>
</tr>
<tr>
<td></td>
<td>Bits 31-05: Reserved.</td>
</tr>
<tr>
<td>ECX</td>
<td>Bits 07 - 00: Level number. Same value in ECX input</td>
</tr>
<tr>
<td></td>
<td>Bits 15 - 08: Level type***.</td>
</tr>
<tr>
<td></td>
<td>Bits 31 - 16: Reserved.</td>
</tr>
</tbody>
</table>
### Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDX</td>
<td>Bits 31-00: x2APIC ID the current logical processor.</td>
</tr>
<tr>
<td><strong>NOTES:</strong></td>
<td>* Software should use this field (EAX[4:0]) to enumerate processor topology of the system.</td>
</tr>
<tr>
<td></td>
<td>** Software must not use EBX[15:0] to enumerate processor topology of the system. This value in this field (EBX[15:0]) is only intended for display/diagnostic purposes. The actual number of logical processors available to BIOS/OS/Applications may be different from the value of EBX[15:0], depending on software and platform hardware configurations.</td>
</tr>
<tr>
<td></td>
<td>*** The value of the “level type” field is not related to level numbers in any way, higher “level type” values do not mean higher levels. Level type field has the following encoding:</td>
</tr>
<tr>
<td></td>
<td>0 : invalid</td>
</tr>
<tr>
<td></td>
<td>1 : SMT</td>
</tr>
<tr>
<td></td>
<td>2 : Core</td>
</tr>
<tr>
<td></td>
<td>3-255 : Reserved</td>
</tr>
</tbody>
</table>

**Processor Extended State Enumeration Main Leaf (EAX = ODH, ECX = 0)**

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAX</td>
<td>Bits 31-00: Reports the valid bit fields of the lower 32 bits of XCR0. If a bit is 0, the corresponding bit field in XCR0 is reserved.</td>
</tr>
<tr>
<td></td>
<td>Bit 00: legacy x87</td>
</tr>
<tr>
<td></td>
<td>Bit 01: 128-bit SSE</td>
</tr>
<tr>
<td></td>
<td>Bit 02: 256-bit AVX</td>
</tr>
<tr>
<td></td>
<td>Bits 31-03: Reserved</td>
</tr>
<tr>
<td>EBX</td>
<td>Bits 31-00: Maximum size (bytes, from the beginning of the XSAVE/XRSTOR save area) required by enabled features in XCR0. May be different than ECX if some features at the end of the XSAVE save area are not enabled.</td>
</tr>
<tr>
<td>ECX</td>
<td>Bit 31-00: Maximum size (bytes, from the beginning of the XSAVE/XRSTOR save area) of the XSAVE/XRSTOR save area required by all supported features in the processor, i.e all the valid bit fields in XCR0.</td>
</tr>
<tr>
<td>EDX</td>
<td>Bit 31-00: Reports the valid bit fields of the upper 32 bits of XCR0. If a bit is 0, the corresponding bit field in XCR0 is reserved.</td>
</tr>
</tbody>
</table>

**Processor Extended State Enumeration Sub-leaf (EAX = ODH, ECX = 1)**
Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAX</td>
<td>Bits 31-01: Reserved</td>
</tr>
<tr>
<td></td>
<td>Bit 00: XSAVEOPT is available;</td>
</tr>
<tr>
<td>EBX</td>
<td>Reserved</td>
</tr>
<tr>
<td>ECX</td>
<td>Reserved</td>
</tr>
<tr>
<td>EDX</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Processor Extended State Enumeration Sub-leaves (EAX = 0DH, ECX = n, n > 1)**

<table>
<thead>
<tr>
<th>0DH</th>
<th>NOTES:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Leaf 0DH output depends on the initial value in ECX.</td>
</tr>
<tr>
<td></td>
<td>If ECX contains an invalid sub leaf index, EAX/EBX/ECX/EDX return 0.</td>
</tr>
<tr>
<td></td>
<td>Each valid sub-leaf index maps to a valid bit in the XCR0 register starting at bit position 2</td>
</tr>
<tr>
<td>EAX</td>
<td>Bits 31-0: The size in bytes (from the offset specified in EBX) of the save area for an extended state feature associated with a valid sub-leaf index, n. This field reports 0 if the sub-leaf index, n, is invalid*.</td>
</tr>
<tr>
<td>EBX</td>
<td>Bits 31-0: The offset in bytes of this extended state component's save area from the beginning of the XSAVE/XRSTOR area. This field reports 0 if the sub-leaf index, n, is invalid*.</td>
</tr>
<tr>
<td>ECX</td>
<td>This field reports 0 if the sub-leaf index, n, is invalid*; otherwise it is reserved.</td>
</tr>
<tr>
<td>EDX</td>
<td>This field reports 0 if the sub-leaf index, n, is invalid*; otherwise it is reserved.</td>
</tr>
</tbody>
</table>

**Unimplemented CPUID Leaf Functions**

| 40000000H - 4FFFFFFFH | Invalid. No existing or future CPU will return processor identification or feature information if the initial EAX value is in the range 40000000H to 4FFFFFFFH. |

**Extended Function CPUID Information**

<table>
<thead>
<tr>
<th>80000000H</th>
<th>EAX</th>
<th>Maximum Input Value for Extended Function CPUID Information (see Table 3-18).</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EBX</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>ECX</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>EDX</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
</table>
| 80000001H         | EAX: Extended Processor Signature and Feature Bits.  
                     EBX: Reserved  
                     ECX: Bit 00: LAHF/SAHF available in 64-bit mode  
                     Bits 31-01 Reserved  
                     EDX: Bits 10-00: Reserved  
                     Bit 11: SYSCALL/SYSRET available (when in 64-bit mode)  
                     Bits 19-12: Reserved = 0  
                     Bit 20: Execute Disable Bit available  
                     Bits 25-21: Reserved = 0  
                     Bit 26: 1-GByte pages are available if 1  
                     Bit 27: RDTSCP and IA32_TSC_AUX are available if 1  
                     Bits 28: Reserved = 0  
                     Bit 29: Intel® 64 Architecture available if 1  
                     Bits 31-30: Reserved = 0 |
| 80000002H         | EAX: Processor Brand String  
                     EBX: Processor Brand String Continued  
                     ECX: Processor Brand String Continued  
                     EDX: Processor Brand String Continued |
| 80000003H         | EAX: Processor Brand String Continued  
                     EBX: Processor Brand String Continued  
                     ECX: Processor Brand String Continued  
                     EDX: Processor Brand String Continued |
| 80000004H         | EAX: Processor Brand String Continued  
                     EBX: Processor Brand String Continued  
                     ECX: Processor Brand String Continued  
                     EDX: Processor Brand String Continued |
| 80000005H         | EAX: Reserved = 0  
                     EBX: Reserved = 0  
                     ECX: Reserved = 0  
                     EDX: Reserved = 0 |
| 80000006H         | EAX: Reserved = 0  
                     EBX: Reserved = 0  
                     ECX: Bits 07-00: Cache Line size in bytes  
                     Bits 11-08: Reserved  
                     Bits 15-12: L2 Associativity field *  
                     Bits 31-16: Cache size in 1K units  
                     EDX: Reserved = 0 |
INPUT EAX = 0: Returns CPUID’s Highest Value for Basic Processor Information and the Vendor Identification String

When CPUID executes with EAX set to 0, the processor returns the highest value the CPUID recognizes for returning basic processor information. The value is returned in the EAX register (see Table 3-18) and is processor specific.

A vendor identification string is also returned in EBX, EDX, and ECX. For Intel processors, the string is “GenuineIntel” and is expressed:

EBX ← 756e6547h (* “Genu”, with G in the low eight bits of BL *)
EDX ← 49656e69h (* “inel”, with i in the low eight bits of DL *)
ECX ← 6c65746eh (* “ntel”, with n in the low eight bits of CL *)

NOTES:
* L2 associativity field encodings:
  00H - Disabled
  01H - Direct mapped
  02H - 2-way
  04H - 4-way
  06H - 8-way
  08H - 16-way
  0FH - Fully associative

Table 3-17. Information Returned by CPUID Instruction (Contd.)

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>80000007H EAX</td>
<td>Reserved = 0</td>
</tr>
<tr>
<td>EBX</td>
<td>Reserved = 0</td>
</tr>
<tr>
<td>ECX</td>
<td>Reserved = 0</td>
</tr>
<tr>
<td>EDX</td>
<td>Bits 07-00: Reserved = 0</td>
</tr>
<tr>
<td></td>
<td>Bit 08: Invariant TSC available if 1</td>
</tr>
<tr>
<td></td>
<td>Bits 31-09: Reserved = 0</td>
</tr>
<tr>
<td>80000008H EAX</td>
<td>Linear/Physical Address size</td>
</tr>
<tr>
<td>EBX</td>
<td>Reserved = 0</td>
</tr>
<tr>
<td>ECX</td>
<td>Reserved = 0</td>
</tr>
<tr>
<td>EDX</td>
<td>Reserved = 0</td>
</tr>
</tbody>
</table>

NOTES:
* If CPUID.80000008H:EAX[7:0] is supported, the maximum physical address number supported should come from this field.
**INPUT EAX = 80000000H: Returns CPUID’s Highest Value for Extended Processor Information**

When CPUID executes with EAX set to 80000000H, the processor returns the highest value the processor recognizes for returning extended processor information. The value is returned in the EAX register (see Table 3-18) and is processor specific.

**Table 3-18. Highest CPUID Source Operand for Intel 64 and IA-32 Processors**

<table>
<thead>
<tr>
<th>Intel 64 or IA-32 Processors</th>
<th>Highest Value in EAX</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Basic Information</td>
</tr>
<tr>
<td>Earlier Intel486 Processors</td>
<td>CPUID Not Implemented</td>
</tr>
<tr>
<td>Later Intel486 Processors</td>
<td>01H</td>
</tr>
<tr>
<td>Pentium Pro and Pentium II Processors</td>
<td>02H</td>
</tr>
<tr>
<td>Pentium III Processors</td>
<td>03H</td>
</tr>
<tr>
<td>Pentium 4 Processors</td>
<td>02H</td>
</tr>
<tr>
<td>Intel Xeon Processors</td>
<td>02H</td>
</tr>
<tr>
<td>Pentium M Processor</td>
<td>02H</td>
</tr>
<tr>
<td>Pentium 4 Processor</td>
<td>05H</td>
</tr>
<tr>
<td>Pentium D Processor (8xx)</td>
<td>05H</td>
</tr>
<tr>
<td>Pentium D Processor (9xx)</td>
<td>06H</td>
</tr>
<tr>
<td>Intel Core Duo Processor</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Core 2 Duo Processor</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Xeon Processor 3000, 5100, 5200, 5300, 5400 Series</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Core 2 Duo Processor 8000 Series</td>
<td>0DH</td>
</tr>
<tr>
<td>Intel Xeon Processor 5200, 5400 Series</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Atom Processor</td>
<td>0AH</td>
</tr>
<tr>
<td>Intel Core i7 Processor</td>
<td>0BH</td>
</tr>
</tbody>
</table>
IA32_BIOS_SIGN_ID Returns Microcode Update Signature

For processors that support the microcode update facility, the IA32_BIOS_SIGN_ID MSR is loaded with the update signature whenever CPUID executes. The signature is returned in the upper DWORD. For details, see Chapter 9 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

INPUT EAX = 1: Returns Model, Family, Stepping Information

When CPUID executes with EAX set to 1, version information is returned in EAX (see Figure 3-5). For example: model, family, and processor type for the Intel Xeon processor 5100 series is as follows:

- Model — 1111B
- Family — 0101B
- Processor Type — 00B

See Table 3-19 for available processor type values. Stepping IDs are provided as needed.

Figure 3-5. Version Information Returned by CPUID in EAX
NOTE
See Chapter 14 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for information on identifying earlier IA-32 processors.

The Extended Family ID needs to be examined only when the Family ID is 0FH. Integrate the fields into a display using the following rule:

\[
\text{IF } \text{Family}_{\text{ID}} \neq 0FH \\
\text{THEN } \text{DisplayFamily} = \text{Family}_{\text{ID}}; \\
\text{ELSE } \text{DisplayFamily} = \text{Extended Family}_{\text{ID}} + \text{Family}_{\text{ID}}; \\
(* \text{ Right justify and zero-extend 4-bit field. } *)
\]

FI;
(* Show DisplayFamily as HEX field. *)

The Extended Model ID needs to be examined only when the Family ID is 06H or 0FH. Integrate the field into a display using the following rule:

\[
\text{IF } (\text{Family}_{\text{ID}} = 06H \text{ or } \text{Family}_{\text{ID}} = 0FH) \\
\text{THEN } \text{DisplayModel} = (\text{Extended Model}_{\text{ID}} \ll 4) + \text{Model}_{\text{ID}}; \\
(* \text{ Right justify and zero-extend 4-bit field; display Model}_{\text{ID}} \text{ as HEX field. } *)
\]

ELSE \text{DisplayModel} = \text{Model}_{\text{ID}};
(* Show DisplayModel as HEX field. *)

INPUT EAX = 1: Returns Additional Information in EBX

When CPUID executes with EAX set to 1, additional information is returned to the EBX register:
- Brand index (low byte of EBX) — this number provides an entry into a brand string table that contains brand strings for IA-32 processors. More information about this field is provided later in this section.
- CLFLUSH instruction cache line size (second byte of EBX) — this number indicates the size of the cache line flushed with CLFLUSH instruction in 8-byte increments. This field was introduced in the Pentium 4 processor.

<table>
<thead>
<tr>
<th>Type</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original OEM Processor</td>
<td>00B</td>
</tr>
<tr>
<td>Intel OverDrive® Processor</td>
<td>01B</td>
</tr>
<tr>
<td>Dual processor (not applicable to Intel486 processors)</td>
<td>10B</td>
</tr>
<tr>
<td>Intel reserved</td>
<td>11B</td>
</tr>
</tbody>
</table>
• Local APIC ID (high byte of EBX) — this number is the 8-bit ID that is assigned to the local APIC on the processor during power up. This field was introduced in the Pentium 4 processor.

**INPUT EAX = 1: Returns Feature Information in ECX and EDX**

When CPUID executes with EAX set to 1, feature information is returned in ECX and EDX.
• Figure 3-6 and Table 3-20 show encodings for ECX.
• Figure 3-7 and Table 3-21 show encodings for EDX.
For all feature flags, a 1 indicates that the feature is supported. Use Intel to properly interpret feature flags.

**NOTE**
Software must confirm that a processor feature is present using feature flags returned by CPUID prior to using the feature. Software should not depend on future offerings retaining all features.
Figure 3-6. Feature Information Returned in the ECX Register

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDRAND</td>
<td></td>
</tr>
<tr>
<td>F16C</td>
<td></td>
</tr>
<tr>
<td>AVX</td>
<td></td>
</tr>
<tr>
<td>OSXSAVE</td>
<td></td>
</tr>
<tr>
<td>XSAVE</td>
<td></td>
</tr>
<tr>
<td>AES</td>
<td></td>
</tr>
<tr>
<td>TSC-Deadline</td>
<td></td>
</tr>
<tr>
<td>POPCNT</td>
<td></td>
</tr>
<tr>
<td>MOVBE</td>
<td></td>
</tr>
<tr>
<td>x2APIC</td>
<td></td>
</tr>
<tr>
<td>SSE4_2</td>
<td>SSE4.2</td>
</tr>
<tr>
<td>SSE4_1</td>
<td>SSE4.1</td>
</tr>
<tr>
<td>TM2</td>
<td>Thermal Monitor 2</td>
</tr>
<tr>
<td>DCA</td>
<td>Direct Cache Access</td>
</tr>
<tr>
<td>PCID</td>
<td>Process-context Identifiers</td>
</tr>
<tr>
<td>PDCM</td>
<td>Perf/Debug Capability MSR</td>
</tr>
<tr>
<td>xTPR Update Control</td>
<td></td>
</tr>
<tr>
<td>CMPXCHG16B</td>
<td></td>
</tr>
<tr>
<td>FMA</td>
<td>Fused Multiply Add</td>
</tr>
<tr>
<td>CNXT-ID</td>
<td>L1 Context ID</td>
</tr>
<tr>
<td>SSSE3</td>
<td>SSSE3 Extensions</td>
</tr>
<tr>
<td>TM2</td>
<td>Thermal Monitor 2</td>
</tr>
<tr>
<td>EST</td>
<td>Enhanced Intel SpeedStep® Technology</td>
</tr>
<tr>
<td>SMX</td>
<td>Safer Mode Extensions</td>
</tr>
<tr>
<td>VMX</td>
<td>Virtual Machine Extensions</td>
</tr>
<tr>
<td>DS-CPL</td>
<td>CPL Qualified Debug Store</td>
</tr>
<tr>
<td>MONITOR</td>
<td>MONITOR/MWAIT</td>
</tr>
<tr>
<td>DTE64</td>
<td>64-bit DS Area</td>
</tr>
<tr>
<td>PCLMULQDQ</td>
<td>Carryless Multiplication</td>
</tr>
<tr>
<td>SSE3</td>
<td>SSE3 Extensions</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>
Table 3-20. Feature Information Returned in the ECX Register

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SSE3</td>
<td>Streaming SIMD Extensions 3 (SSE3). A value of 1 indicates the processor supports this technology.</td>
</tr>
<tr>
<td>1</td>
<td>PCLMULQDQ</td>
<td>PCLMULQDQ. A value of 1 indicates the processor supports the PCLMULQDQ instruction</td>
</tr>
<tr>
<td>2</td>
<td>DTES64</td>
<td>64-bit DS Area. A value of 1 indicates the processor supports DS area using 64-bit layout</td>
</tr>
<tr>
<td>3</td>
<td>MONITOR</td>
<td>MONITOR/MWAIT. A value of 1 indicates the processor supports this feature.</td>
</tr>
<tr>
<td>4</td>
<td>DS-CPL</td>
<td>CPL Qualified Debug Store. A value of 1 indicates the processor supports the extensions to the Debug Store feature to allow for branch message storage qualified by CPL.</td>
</tr>
<tr>
<td>5</td>
<td>VMX</td>
<td>Virtual Machine Extensions. A value of 1 indicates that the processor supports this technology</td>
</tr>
<tr>
<td>6</td>
<td>SMX</td>
<td>Safer Mode Extensions. A value of 1 indicates that the processor supports this technology. See Chapter 5, &quot;Safer Mode Extensions Reference&quot;.</td>
</tr>
<tr>
<td>7</td>
<td>EIST</td>
<td>Enhanced Intel SpeedStep® technology. A value of 1 indicates that the processor supports this technology.</td>
</tr>
<tr>
<td>8</td>
<td>TM2</td>
<td>Thermal Monitor 2. A value of 1 indicates whether the processor supports this technology.</td>
</tr>
<tr>
<td>9</td>
<td>SSSE3</td>
<td>A value of 1 indicates the presence of the Supplemental Streaming SIMD Extensions 3 (SSSE3). A value of 0 indicates the instruction extensions are not present in the processor</td>
</tr>
<tr>
<td>10</td>
<td>CNXT-ID</td>
<td>L1 Context ID. A value of 1 indicates the L1 data cache mode can be set to either adaptive mode or shared mode. A value of 0 indicates this feature is not supported. See definition of the IA32_MISC_ENABLE MSR Bit 24 (L1 Data Cache Context Mode) for details.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>FMA</td>
<td>A value of 1 indicates the processor supports FMA extensions using YMM state.</td>
</tr>
<tr>
<td>13</td>
<td>CMPXCHG16B</td>
<td>CMPXCHG16B Available. A value of 1 indicates that the feature is available. See the “CMPXCHG8B/CMPXCHG16B—Compare and Exchange Bytes” section in this chapter for a description.</td>
</tr>
<tr>
<td>14</td>
<td>xTPR Update Control</td>
<td>xTPR Update Control. A value of 1 indicates that the processor supports changing IA32_MISC_ENABLE[bit 23].</td>
</tr>
<tr>
<td>15</td>
<td>PDCM</td>
<td>Perfmon and Debug Capability: A value of 1 indicates the processor supports the performance and debug feature indication MSR IA32_PERF_CAPABILITIES.</td>
</tr>
</tbody>
</table>
Table 3-20. Feature Information Returned in the ECX Register  (Contd.)

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>17</td>
<td>PCID</td>
<td><strong>Process-context identifiers.</strong> A value of 1 indicates that the processor supports PCIDs and that software may set CR4.PCIDE to 1.</td>
</tr>
<tr>
<td>18</td>
<td>DCA</td>
<td>A value of 1 indicates the processor supports the ability to prefetch data from a memory mapped device.</td>
</tr>
<tr>
<td>19</td>
<td>SSE4.1</td>
<td>A value of 1 indicates that the processor supports SSE4.1.</td>
</tr>
<tr>
<td>20</td>
<td>SSE4.2</td>
<td>A value of 1 indicates that the processor supports SSE4.2.</td>
</tr>
<tr>
<td>21</td>
<td>x2APIC</td>
<td>A value of 1 indicates that the processor supports x2APIC feature.</td>
</tr>
<tr>
<td>22</td>
<td>MOVBE</td>
<td>A value of 1 indicates that the processor supports MOVBE instruction.</td>
</tr>
<tr>
<td>23</td>
<td>POPCNT</td>
<td>A value of 1 indicates that the processor supports the POPCNT instruction.</td>
</tr>
<tr>
<td>24</td>
<td>TSC-Deadline</td>
<td>A value of 1 indicates that the processor’s local APIC timer supports one-shot operation using a TSC deadline value.</td>
</tr>
<tr>
<td>25</td>
<td>AESNI</td>
<td>A value of 1 indicates that the processor supports the AESNI instruction extensions.</td>
</tr>
<tr>
<td>26</td>
<td>XSAVE</td>
<td>A value of 1 indicates that the processor supports the XSAVE/XRSTOR processor extended states feature, the XSETBV/XGETBV instructions, and XCR0.</td>
</tr>
<tr>
<td>27</td>
<td>OSXSAVE</td>
<td>A value of 1 indicates that the OS has enabled XSETBV/XGETBV instructions to access XCR0, and support for processor extended state management using XSAVE/XRSTOR.</td>
</tr>
<tr>
<td>28</td>
<td>AVX</td>
<td>A value of 1 indicates the processor supports the AVX instruction extensions.</td>
</tr>
<tr>
<td>29</td>
<td>F16C</td>
<td>A value of 1 indicates that processor supports 16-bit floating-point conversion instructions.</td>
</tr>
<tr>
<td>30</td>
<td>RDRAND</td>
<td>A value of 1 indicates that processor supports RDRAND instruction.</td>
</tr>
<tr>
<td>31</td>
<td>Not Used</td>
<td>Always returns 0.</td>
</tr>
</tbody>
</table>
Figure 3-7. Feature Information Returned in the EDX Register
Table 3-21. More on Feature Information Returned in the EDX Register

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>FPU</td>
<td>Floating Point Unit On-Chip. The processor contains an x87 FPU.</td>
</tr>
<tr>
<td>1</td>
<td>VME</td>
<td>Virtual 8086 Mode Enhancements. Virtual 8086 mode enhancements, including CR4.VME for controlling the feature, CR4.PVI for protected mode virtual interrupts, software interrupt indirection, expansion of the TSS with the software indirection bitmap, and EFLAGS.VIF and EFLAGS.VIP flags.</td>
</tr>
<tr>
<td>2</td>
<td>DE</td>
<td>Debugging Extensions. Support for I/O breakpoints, including CR4.DE for controlling the feature, and optional trapping of accesses to DR4 and DR5.</td>
</tr>
<tr>
<td>3</td>
<td>PSE</td>
<td>Page Size Extension. Large pages of size 4 MByte are supported, including CR4.PSE for controlling the feature, the defined dirty bit in PDE (Page Directory Entries), optional reserved bit trapping in CR3, PDEs, and PTEs.</td>
</tr>
<tr>
<td>4</td>
<td>TSC</td>
<td>Time Stamp Counter. The RDTSC instruction is supported, including CR4.TSD for controlling privilege.</td>
</tr>
<tr>
<td>5</td>
<td>MSR</td>
<td>Model Specific Registers RDMSR and WRMSR Instructions. The RDMSR and WRMSR instructions are supported. Some of the MSRs are implementation dependent.</td>
</tr>
<tr>
<td>6</td>
<td>PAE</td>
<td>Physical Address Extension. Physical addresses greater than 32 bits are supported: extended page table entry formats, an extra level in the page translation tables is defined, 2-MByte pages are supported instead of 4 Mbyte pages if PAE bit is 1.</td>
</tr>
<tr>
<td>7</td>
<td>MCE</td>
<td>Machine Check Exception. Exception 18 is defined for Machine Checks, including CR4.MCE for controlling the feature. This feature does not define the model-specific implementations of machine-check error logging, reporting, and processor shutdowns. Machine Check exception handlers may have to depend on processor version to do model specific processing of the exception, or test for the presence of the Machine Check feature.</td>
</tr>
<tr>
<td>8</td>
<td>CX8</td>
<td>CMPXCHG8B Instruction. The compare-and-exchange 8 bytes (64 bits) instruction is supported (implicitly locked and atomic).</td>
</tr>
<tr>
<td>9</td>
<td>APIC</td>
<td>APIC On-Chip. The processor contains an Advanced Programmable Interrupt Controller (APIC), responding to memory mapped commands in the physical address range FFFE0000H to FFFE0FFFH (by default - some processors permit the APIC to be relocated).</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>11</td>
<td>SEP</td>
<td>SYSENTER and SYSEXIT Instructions. The SYSENTER and SYSEXIT and associated MSRs are supported.</td>
</tr>
<tr>
<td>12</td>
<td>MTRR</td>
<td>Memory Type Range Registers. MTRRs are supported. The MTRRcap MSR contains feature bits that describe what memory types are supported, how many variable MTRRs are supported, and whether fixed MTRRs are supported.</td>
</tr>
</tbody>
</table>
### Table 3-21. More on Feature Information Returned in the EDX Register (Contd.)

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>PGE</td>
<td><strong>Page Global Bit.</strong> The global bit is supported in paging-structure entries that map a page, indicating TLB entries that are common to different processes and need not be flushed. The CR4.PGE bit controls this feature.</td>
</tr>
<tr>
<td>14</td>
<td>MCA</td>
<td><strong>Machine Check Architecture.</strong> The Machine Check Architecture, which provides a compatible mechanism for error reporting in P6 family, Pentium 4, Intel Xeon processors, and future processors, is supported. The MCG_CAP MSR contains feature bits describing how many banks of error reporting MSRs are supported.</td>
</tr>
<tr>
<td>15</td>
<td>CMOV</td>
<td><strong>Conditional Move Instructions.</strong> The conditional move instruction CMOV is supported. In addition, if x87 FPU is present as indicated by the CPUID.FPU feature bit, then the FCOMI and FCMOV instructions are supported.</td>
</tr>
<tr>
<td>16</td>
<td>PAT</td>
<td><strong>Page Attribute Table.</strong> Page Attribute Table is supported. This feature augments the Memory Type Range Registers (MTRRs), allowing an operating system to specify attributes of memory accessed through a linear address on a 4KB granularity.</td>
</tr>
<tr>
<td>17</td>
<td>PSE-36</td>
<td><strong>32-Bit Page Size Extension.</strong> 4-MByte pages addressing physical memory beyond 4 GBytes are supported with 32-bit paging. This feature indicates that upper bits of the physical address of a 4-MByte page are encoded in bits 20:13 of the page-directory entry. Such physical addresses are limited by MAXPHYADDR and may be up to 40 bits in size.</td>
</tr>
<tr>
<td>18</td>
<td>PSN</td>
<td><strong>Processor Serial Number.</strong> The processor supports the 96-bit processor identification number feature and the feature is enabled.</td>
</tr>
<tr>
<td>19</td>
<td>CFSH</td>
<td><strong>CLFLUSH Instruction.</strong> CLFLUSH Instruction is supported.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>21</td>
<td>DS</td>
<td><strong>Debug Store.</strong> The processor supports the ability to write debug information into a memory resident buffer. This feature is used by the branch trace store (BTS) and precise event-based sampling (PEBS) facilities (see Chapter 23, “Introduction to Virtual-Machine Extensions,” in the <em>Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C</em>).</td>
</tr>
<tr>
<td>22</td>
<td>ACPI</td>
<td><strong>Thermal Monitor and Software Controlled Clock Facilities.</strong> The processor implements internal MSRs that allow processor temperature to be monitored and processor performance to be modulated in predefined duty cycles under software control.</td>
</tr>
<tr>
<td>23</td>
<td>MMX</td>
<td><strong>Intel MMX Technology.</strong> The processor supports the Intel MMX technology.</td>
</tr>
<tr>
<td>24</td>
<td>FXSR</td>
<td><strong>FXSAVE and FXRSTOR Instructions.</strong> The FXSAVE and FXRSTOR instructions are supported for fast save and restore of the floating point context. Presence of this bit also indicates that CR4.OSFXSR is available for an operating system to indicate that it supports the FXSAVE and FXRSTOR instructions.</td>
</tr>
</tbody>
</table>
CPUID—CPU Identification

**INPUT EAX = 2: TLB/Cache/Prefetch Information Returned in EAX, EBX, ECX, EDX**

When CPUID executes with EAX set to 2, the processor returns information about the processor’s internal TLBs, cache and prefetch hardware in the EAX, EBX, ECX, and EDX registers. The information is reported in encoded form and fall into the following categories:

- The least-significant byte in register EAX (register AL) indicates the number of times the CPUID instruction must be executed with an input value of 2 to get a complete description of the processor’s TLB/Cache/Prefetch hardware. The Intel Xeon processor 7400 series will return a 1.
- The most significant bit (bit 31) of each register indicates whether the register contains valid information (set to 0) or is reserved (set to 1).
- If a register contains valid information, the information is contained in 1 byte descriptors. There are four types of encoding values for the byte descriptor, the encoding type is noted in the second column of Table 3-22. Table 3-22 lists the encoding of these descriptors. Note that the order of descriptors in the EAX, EBX, ECX, and EDX registers is not defined; that is, specific bytes are not designated to contain descriptors for specific cache, prefetch, or TLB types. The descriptors may appear in any order. Note also a processor may report a general descriptor type (FFH) and not report any byte descriptor of "cache type" via CPUID leaf 2.

---

**Table 3-21. More on Feature Information Returned in the EDX Register (Contd.)**

<table>
<thead>
<tr>
<th>Bit #</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>SSE</td>
<td>SSE. The processor supports the SSE extensions.</td>
</tr>
<tr>
<td>26</td>
<td>SSE2</td>
<td>SSE2. The processor supports the SSE2 extensions.</td>
</tr>
<tr>
<td>27</td>
<td>SS</td>
<td><strong>Self Snoop.</strong> The processor supports the management of conflicting memory types by performing a snoop of its own cache structure for transactions issued to the bus.</td>
</tr>
<tr>
<td>28</td>
<td>HTT</td>
<td><strong>Max APIC IDs reserved field is Valid.</strong> A value of 0 for HTT indicates there is only a single logical processor in the package and software should assume only a single APIC ID is reserved. A value of 1 for HTT indicates the value in CPUID.1.EBX[23:16] (the Maximum number of addressable IDs for logical processors in this package) is valid for the package.</td>
</tr>
<tr>
<td>29</td>
<td>TM</td>
<td>Thermal Monitor. The processor implements the thermal monitor automatic thermal control circuitry (TCC).</td>
</tr>
<tr>
<td>30</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>31</td>
<td>PBE</td>
<td>Pending Break Enable. The processor supports the use of the FERR#/PBE# pin when the processor is in the stop-clock state (STPCLK# is asserted) to signal the processor that an interrupt is pending and that the processor should return to normal operation to handle the interrupt. Bit 10 (PBE enable) in the IA32_MISC_ENABLE MSR enables this capability.</td>
</tr>
</tbody>
</table>
### Table 3-22. Encoding of CPUID Leaf 2 Descriptors

<table>
<thead>
<tr>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>General</td>
<td>Null descriptor, this byte contains no information</td>
</tr>
<tr>
<td>01H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte pages, 4-way set associative, 32 entries</td>
</tr>
<tr>
<td>02H</td>
<td>TLB</td>
<td>Instruction TLB: 4 MByte pages, fully associative, 2 entries</td>
</tr>
<tr>
<td>03H</td>
<td>TLB</td>
<td>Data TLB: 4 KByte pages, 4-way set associative, 64 entries</td>
</tr>
<tr>
<td>04H</td>
<td>TLB</td>
<td>Data TLB: 4 MByte pages, 4-way set associative, 8 entries</td>
</tr>
<tr>
<td>05H</td>
<td>TLB</td>
<td>Data TLB1: 4 MByte pages, 4-way set associative, 32 entries</td>
</tr>
<tr>
<td>06H</td>
<td>Cache</td>
<td>1st-level instruction cache: 8 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>08H</td>
<td>Cache</td>
<td>1st-level instruction cache: 16 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>09H</td>
<td>Cache</td>
<td>1st-level instruction cache: 32 KBytes, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>0AH</td>
<td>Cache</td>
<td>1st-level data cache: 8 KBytes, 2-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>0BH</td>
<td>TLB</td>
<td>Instruction TLB: 4 MByte pages, 4-way set associative, 4 entries</td>
</tr>
<tr>
<td>0CH</td>
<td>Cache</td>
<td>1st-level data cache: 16 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>0DH</td>
<td>Cache</td>
<td>1st-level data cache: 16 KBytes, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>0EH</td>
<td>Cache</td>
<td>1st-level data cache: 24 KBytes, 6-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>21H</td>
<td>Cache</td>
<td>2nd-level cache: 256 KBytes, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>22H</td>
<td>Cache</td>
<td>3rd-level cache: 512 KBytes, 4-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>23H</td>
<td>Cache</td>
<td>3rd-level cache: 1 MBytes, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>25H</td>
<td>Cache</td>
<td>3rd-level cache: 2 MBytes, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>29H</td>
<td>Cache</td>
<td>3rd-level cache: 4 MBytes, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>2CH</td>
<td>Cache</td>
<td>1st-level data cache: 32 KBytes, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>30H</td>
<td>Cache</td>
<td>1st-level instruction cache: 32 KBytes, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>40H</td>
<td>Cache</td>
<td>No 2nd-level cache or, if processor contains a valid 2nd-level cache, no 3rd-level cache</td>
</tr>
<tr>
<td>41H</td>
<td>Cache</td>
<td>2nd-level cache: 128 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>42H</td>
<td>Cache</td>
<td>2nd-level cache: 256 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>43H</td>
<td>Cache</td>
<td>2nd-level cache: 512 KBytes, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>44H</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 4-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>45H</td>
<td>Cache</td>
<td>2nd-level cache: 2 MByte, 4-way set associative, 32 byte line size</td>
</tr>
</tbody>
</table>
### Table 3-22. Encoding of CPUID Leaf 2 Descriptors (Contd.)

<table>
<thead>
<tr>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>46H</td>
<td>Cache</td>
<td>3rd-level cache: 4 MByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>47H</td>
<td>Cache</td>
<td>3rd-level cache: 8 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>48H</td>
<td>Cache</td>
<td>2nd-level cache: 3MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>49H</td>
<td>Cache</td>
<td>3rd-level cache: 4MB, 16-way set associative, 64-byte line size (Intel Xeon processor MP, Family 0FH, Model 06H); 2nd-level cache: 4 MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4AH</td>
<td>Cache</td>
<td>3rd-level cache: 6MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4BH</td>
<td>Cache</td>
<td>3rd-level cache: 6MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>48H</td>
<td>Cache</td>
<td>3rd-level cache: 16MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4AH</td>
<td>Cache</td>
<td>3rd-level cache: 6MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4BH</td>
<td>Cache</td>
<td>3rd-level cache: 16MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4CH</td>
<td>Cache</td>
<td>3rd-level cache: 12MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4DH</td>
<td>Cache</td>
<td>3rd-level cache: 16MByte, 16-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4EH</td>
<td>Cache</td>
<td>2nd-level cache: 6MByte, 24-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>4FH</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte pages, 32 entries</td>
</tr>
<tr>
<td>50H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte and 2-MByte or 4-MByte pages, 64 entries</td>
</tr>
<tr>
<td>51H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte and 2-MByte or 4-MByte pages, 128 entries</td>
</tr>
<tr>
<td>52H</td>
<td>TLB</td>
<td>Instruction TLB: 2-MByte or 4-MByte pages, fully associative, 7 entries</td>
</tr>
<tr>
<td>53H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte and 4 MByte pages, 64 entries</td>
</tr>
<tr>
<td>54H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte and 4 MByte pages, 128 entries</td>
</tr>
<tr>
<td>55H</td>
<td>TLB</td>
<td>Instruction TLB: 2-MByte or 4-MByte pages, fully associative, 7 entries</td>
</tr>
<tr>
<td>56H</td>
<td>TLB</td>
<td>Data TLB0: 4 MByte pages, 4-way set associative, 16 entries</td>
</tr>
<tr>
<td>57H</td>
<td>TLB</td>
<td>Data TLB0: 4 KByte pages, 4-way associative, 16 entries</td>
</tr>
<tr>
<td>59H</td>
<td>TLB</td>
<td>Data TLB0: 4 KByte pages, fully associative, 16 entries</td>
</tr>
<tr>
<td>5AH</td>
<td>TLB</td>
<td>Data TLB0: 2-MByte or 4 MByte pages, 4-way set associative, 32 entries</td>
</tr>
<tr>
<td>5BH</td>
<td>TLB</td>
<td>Data TLB0: 2-MByte or 4 MByte pages, 64 entries</td>
</tr>
<tr>
<td>5CH</td>
<td>TLB</td>
<td>Data TLB0: 2-MByte or 4 MByte pages, 128 entries</td>
</tr>
<tr>
<td>5DH</td>
<td>TLB</td>
<td>Data TLB0: 2-MByte or 4 MByte pages, 256 entries</td>
</tr>
<tr>
<td>60H</td>
<td>Cache</td>
<td>1st-level data cache: 16 KByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>66H</td>
<td>Cache</td>
<td>1st-level data cache: 8 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>67H</td>
<td>Cache</td>
<td>1st-level data cache: 16 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>68H</td>
<td>Cache</td>
<td>1st-level data cache: 32 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>70H</td>
<td>Cache</td>
<td>Trace cache: 12 K-byte, 8-way set associative</td>
</tr>
<tr>
<td>71H</td>
<td>Cache</td>
<td>Trace cache: 16 K-byte, 8-way set associative</td>
</tr>
<tr>
<td>72H</td>
<td>Cache</td>
<td>Trace cache: 32 K-byte, 8-way set associative</td>
</tr>
<tr>
<td>76H</td>
<td>TLB</td>
<td>Instruction TLB: 2M/4M pages, fully associative, 8 entries</td>
</tr>
<tr>
<td>78H</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 4-way set associative, 64byte line size</td>
</tr>
</tbody>
</table>
### Table 3-22. Encoding of CPUID Leaf 2 Descriptors (Contd.)

<table>
<thead>
<tr>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>79H</td>
<td>Cache</td>
<td>2nd-level cache: 128 KByte, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>7AH</td>
<td>Cache</td>
<td>2nd-level cache: 256 KByte, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>7BH</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>7CH</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 8-way set associative, 64 byte line size, 2 lines per sector</td>
</tr>
<tr>
<td>7DH</td>
<td>Cache</td>
<td>2nd-level cache: 2 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>7FH</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 2-way set associative, 64-byte line size</td>
</tr>
<tr>
<td>80H</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 8-way set associative, 64-byte line size</td>
</tr>
<tr>
<td>82H</td>
<td>Cache</td>
<td>2nd-level cache: 256 KByte, 8-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>83H</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 8-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>84H</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 8-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>85H</td>
<td>Cache</td>
<td>2nd-level cache: 2 MByte, 8-way set associative, 32 byte line size</td>
</tr>
<tr>
<td>86H</td>
<td>Cache</td>
<td>2nd-level cache: 512 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>87H</td>
<td>Cache</td>
<td>2nd-level cache: 1 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>B0H</td>
<td>TLB</td>
<td>Instruction TLB: 4 KByte pages, 4-way set associative, 128 entries</td>
</tr>
<tr>
<td>B1H</td>
<td>TLB</td>
<td>Instruction TLB: 2M pages, 4-way, 8 entries or 4M pages, 4-way, 4 entries</td>
</tr>
<tr>
<td>B2H</td>
<td>TLB</td>
<td>Instruction TLB: 4KByte pages, 4-way set associative, 64 entries</td>
</tr>
<tr>
<td>B3H</td>
<td>TLB</td>
<td>Data TLB: 4 KByte pages, 4-way set associative, 128 entries</td>
</tr>
<tr>
<td>B4H</td>
<td>TLB</td>
<td>Data TLB: 4 KByte pages, 4-way associative, 256 entries</td>
</tr>
<tr>
<td>BAH</td>
<td>TLB</td>
<td>Data TLB: 4 KByte pages, 4-way associative, 64 entries</td>
</tr>
<tr>
<td>C0H</td>
<td>TLB</td>
<td>Data TLB: 4 KByte and 4 MByte pages, 4-way associative, 8 entries</td>
</tr>
<tr>
<td>CAH</td>
<td>TLB</td>
<td>Shared 2nd-Level TLB: 4 KByte pages, 4-way associative, 512 entries</td>
</tr>
<tr>
<td>D0H</td>
<td>Cache</td>
<td>3rd-level cache: 512 KByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>D1H</td>
<td>Cache</td>
<td>3rd-level cache: 1 MByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>D2H</td>
<td>Cache</td>
<td>3rd-level cache: 2 MByte, 4-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>D6H</td>
<td>Cache</td>
<td>3rd-level cache: 1 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>D7H</td>
<td>Cache</td>
<td>3rd-level cache: 2 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>D8H</td>
<td>Cache</td>
<td>3rd-level cache: 4 MByte, 8-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>DCH</td>
<td>Cache</td>
<td>3rd-level cache: 1.5 MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>DDH</td>
<td>Cache</td>
<td>3rd-level cache: 3 MByte, 12-way set associative, 64 byte line size</td>
</tr>
<tr>
<td>DEH</td>
<td>Cache</td>
<td>3rd-level cache: 6 MByte, 12-way set associative, 64 byte line size</td>
</tr>
</tbody>
</table>
Example 3-1. Example of Cache and TLB Interpretation

The first member of the family of Pentium 4 processors returns the following information about caches and TLBs when the CPUID executes with an input value of 2:

EAX 66 5B 50 01H
EBX 0H
ECX 0H
EDX 00 7A 70 00H

Which means:

- The least-significant byte (byte 0) of register EAX is set to 01H. This indicates that CPUID needs to be executed once with an input value of 2 to retrieve complete information about caches and TLBs.
- The most-significant bit of all four registers (EAX, EBX, ECX, and EDX) is set to 0, indicating that each register contains valid 1-byte descriptors.
- Bytes 1, 2, and 3 of register EAX indicate that the processor has:
  - 50H - a 64-entry instruction TLB, for mapping 4-KByte and 2-MByte or 4-MByte pages.
  - 5BH - a 64-entry data TLB, for mapping 4-KByte and 4-MByte pages.
  - 66H - an 8-KByte 1st level data cache, 4-way set associative, with a 64-Byte cache line size.
- The descriptors in registers EBX and ECX are valid, but contain NULL descriptors.
- Bytes 0, 1, 2, and 3 of register EDX indicate that the processor has:
  - 00H - NULL descriptor.
  - 70H - Trace cache: 12 K-µop, 8-way set associative.
INSTRUCTION SET REFERENCE, A-L

— 7AH - a 256-KByte 2nd level cache, 8-way set associative, with a sectored, 64-byte cache line size.
— 00H - NULL descriptor.

INPUT EAX = 04H: Returns Deterministic Cache Parameters for Each Level

When CPUID executes with EAX set to 04H and ECX contains an index value, the processor returns encoded data that describe a set of deterministic cache parameters (for the cache level associated with the input in ECX). Valid index values start from 0.

Software can enumerate the deterministic cache parameters for each level of the cache hierarchy starting with an index value of 0, until the parameters report the value associated with the cache type field is 0. The architecturally defined fields reported by deterministic cache parameters are documented in Table 3-17.

This Cache Size in Bytes
\[
= (\text{Ways} + 1) \times (\text{Partitions} + 1) \times (\text{Line Size} + 1) \times (\text{Sets} + 1)
\]
\[
= (\text{EBX}[31:22] + 1) \times (\text{EBX}[21:12] + 1) \times (\text{EBX}[11:0] + 1) \times (\text{ECX} + 1)
\]

The CPUID leaf 04H also reports data that can be used to derive the topology of processor cores in a physical package. This information is constant for all valid index values. Software can query the raw data reported by executing CPUID with EAX=04H and ECX=0 and use it as part of the topology enumeration algorithm described in Chapter 8, "Multiple-Processor Management," in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

INPUT EAX = 05H: Returns MONITOR and MWAIT Features

When CPUID executes with EAX set to 05H, the processor returns information about features available to MONITOR/MWAIT instructions. The MONITOR instruction is used for address-range monitoring in conjunction with MWAIT instruction. The MWAIT instruction optionally provides additional extensions for advanced power management. See Table 3-17.

INPUT EAX = 06H: Returns Thermal and Power Management Features

When CPUID executes with EAX set to 06H, the processor returns information about thermal and power management features. See Table 3-17.

INPUT EAX = 07H: Returns Structured Extended Feature Enumeration Information

When CPUID executes with EAX set to 7 and ECX = 0, the processor returns information about the maximum number of sub-leaves that contain extended feature flags. See Table 3-17.

When CPUID executes with EAX set to 7 and ECX = n (n > 1 and less than the num-
CPU identifier—CPU Identification

The CPUID function returns information about extended feature flags. In subleaf 0, only EAX has the number of sub-leaves. In subleaf 0, EBX, ECX & EDX all contain extended feature flags.

**INPUT EAX = 09H: Returns Direct Cache Access Information**

When CPUID executes with EAX set to 09H, the processor returns information about Direct Cache Access capabilities. See Table 3-17.

**INPUT EAX = 0AH: Returns Architectural Performance Monitoring Features**

When CPUID executes with EAX set to 0AH, the processor returns information about support for architectural performance monitoring capabilities. Architectural performance monitoring is supported if the version ID (see Table 3-17) is greater than Pn 0. See Table 3-17.

For each version of architectural performance monitoring capability, software must enumerate this leaf to discover the programming facilities and the architectural performance events available in the processor. The details are described in Chapter 23, “Introduction to Virtual-Machine Extensions,” in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C*.

**INPUT EAX = 0BH: Returns Extended Topology Information**

When CPUID executes with EAX set to 0BH, the processor returns information about extended topology enumeration data. Software must detect the presence of CPUID leaf 0BH by verifying (a) the highest leaf index supported by CPUID is >= 0BH, and (b) CPUID.0BH:EBX[15:0] reports a non-zero value. See Table 3-17.

**INPUT EAX = 0DH: Returns Processor Extended States Enumeration Information**

When CPUID executes with EAX set to 0DH and ECX = 0, the processor returns information about the bit-vector representation of all processor state extensions that are supported in the processor and storage size requirements of the XSAVE/XRSTOR area. See Table 3-17.

When CPUID executes with EAX set to 0DH and ECX = n (n > 1, and is a valid sub-leaf index), the processor returns information about the size and offset of each processor extended state save area within the XSAVE/XRSTOR area. See Table 3-17. Software can use the forward-extendable technique depicted below to query the valid sub-leaves and obtain size and offset information for each processor extended state save area:

For i = 2 to 62 // sub-leaf 1 is reserved
IF (CPUID.(EAX=0DH, ECX=0):VECTOR[i] = 1 ) // VECTOR is the 64-bit value of EDX:EAX
  Execute CPUID.(EAX=0DH, ECX = i) to examine size and offset for sub-leaf i;
FI;
METHODS FOR RETURNING BRANDING INFORMATION

Use the following techniques to access branding information:

1. Processor brand string method; this method also returns the processor’s maximum operating frequency
2. Processor brand index; this method uses a software supplied brand string table.

These two methods are discussed in the following sections. For methods that are available in early processors, see Section: “Identification of Earlier IA-32 Processors” in Chapter 14 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*.

The Processor Brand String Method

Figure 3-8 describes the algorithm used for detection of the brand string. Processor brand identification software should execute this algorithm on all Intel 64 and IA-32 processors.

This method (introduced with Pentium 4 processors) returns an ASCII brand identification string and the maximum operating frequency of the processor to the EAX, EBX, ECX, and EDX registers.
How Brand Strings Work

To use the brand string method, execute CPUID with EAX input of 80000002H through 80000004H. For each input value, CPUID returns 16 ASCII characters using EAX, EBX, ECX, and EDX. The returned string will be NULL-terminated.

Table 3-23 shows the brand string that is returned by the first processor in the Pentium 4 processor family.
Table 3-23. Processor Brand String Returned with Pentium 4 Processor

<table>
<thead>
<tr>
<th>EAX Input Value</th>
<th>Return Values</th>
<th>ASCII Equivalent</th>
</tr>
</thead>
<tbody>
<tr>
<td>80000002H</td>
<td>EAX = 20202020H</td>
<td>&quot; &quot;</td>
</tr>
<tr>
<td></td>
<td>EBX = 20202020H</td>
<td>&quot; &quot;</td>
</tr>
<tr>
<td></td>
<td>ECX = 20202020H</td>
<td>&quot; &quot;</td>
</tr>
<tr>
<td></td>
<td>EDX = 6E492020H</td>
<td>&quot;nl&quot;</td>
</tr>
<tr>
<td>80000003H</td>
<td>EAX = 286C6574H</td>
<td>&quot;(let&quot;</td>
</tr>
<tr>
<td></td>
<td>EBX = 50202952H</td>
<td>&quot;P )R&quot;</td>
</tr>
<tr>
<td></td>
<td>ECX = 69746E65H</td>
<td>&quot;itne&quot;</td>
</tr>
<tr>
<td></td>
<td>EDX = 52286D75H</td>
<td>&quot;R(mu&quot;</td>
</tr>
<tr>
<td>80000004H</td>
<td>EAX = 20342029H</td>
<td>&quot; 4 )&quot;</td>
</tr>
<tr>
<td></td>
<td>EBX = 20555043H</td>
<td>&quot; UPC&quot;</td>
</tr>
<tr>
<td></td>
<td>ECX = 30303531H</td>
<td>&quot;0051&quot;</td>
</tr>
<tr>
<td></td>
<td>EDX = 007A484DH</td>
<td>&quot;\0zHM&quot;</td>
</tr>
</tbody>
</table>

Extracting the Maximum Processor Frequency from Brand Strings

Figure 3-9 provides an algorithm which software can use to extract the maximum processor operating frequency from the processor brand string.

**NOTE**

When a frequency is given in a brand string, it is the maximum qualified frequency of the processor, not the frequency at which the processor is currently running.
The Processor Brand Index Method

The brand index method (introduced with Pentium® III Xeon® processors) provides an entry point into a brand identification table that is maintained in memory by system software and is accessible from system- and user-level code. In this table, each brand index is associate with an ASCII brand identification string that identifies the official Intel family and model number of a processor.

When CPUID executes with EAX set to 1, the processor returns a brand index to the low byte in EBX. Software can then use this index to locate the brand identification string for the processor in the brand identification table. The first entry (brand index 0) in this table is reserved, allowing for backward compatibility with processors that
do not support the brand identification feature. Starting with processor signature family ID = 0FH, model = 03H, brand index method is no longer supported. Use brand string method instead.

Table 3-24 shows brand indices that have identification strings associated with them.

**Table 3-24. Mapping of Brand Indices; and Intel 64 and IA-32 Processor Brand Strings**

<table>
<thead>
<tr>
<th>Brand Index</th>
<th>Brand String</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>This processor does not support the brand identification feature</td>
</tr>
<tr>
<td>01H</td>
<td>Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>02H</td>
<td>Intel(R) Pentium(R) III processor¹</td>
</tr>
<tr>
<td>03H</td>
<td>Intel(R) Pentium(R) III Xeon(R) processor; If processor signature = 000006B1h, then Intel(R) Celeron(R) processor</td>
</tr>
<tr>
<td>04H</td>
<td>Intel(R) Pentium(R) III processor</td>
</tr>
<tr>
<td>06H</td>
<td>Mobile Intel(R) Pentium(R) III processor-M</td>
</tr>
<tr>
<td>07H</td>
<td>Mobile Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>08H</td>
<td>Intel(R) Pentium(R) 4 processor</td>
</tr>
<tr>
<td>09H</td>
<td>Intel(R) Pentium(R) 4 processor</td>
</tr>
<tr>
<td>0AH</td>
<td>Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>0BH</td>
<td>Intel(R) Xeon(R) processor; If processor signature = 00000F13h, then Intel(R) Xeon(R) processor MP</td>
</tr>
<tr>
<td>0CH</td>
<td>Intel(R) Xeon(R) processor MP</td>
</tr>
<tr>
<td>0EH</td>
<td>Mobile Intel(R) Pentium(R) 4 processor-M; If processor signature = 00000F13h, then Intel(R) Xeon(R) processor</td>
</tr>
<tr>
<td>0FH</td>
<td>Mobile Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>11H</td>
<td>Mobile Genuine Intel(R) processor</td>
</tr>
<tr>
<td>12H</td>
<td>Intel(R) Celeron(R) M processor</td>
</tr>
<tr>
<td>13H</td>
<td>Mobile Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>14H</td>
<td>Intel(R) Celeron(R) processor</td>
</tr>
<tr>
<td>15H</td>
<td>Mobile Genuine Intel(R) processor</td>
</tr>
<tr>
<td>16H</td>
<td>Intel(R) Pentium(R) M processor</td>
</tr>
<tr>
<td>17H</td>
<td>Mobile Intel(R) Celeron(R) processor¹</td>
</tr>
<tr>
<td>18H - 0FFH</td>
<td>RESERVED</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Indicates versions of these processors that were introduced after the Pentium III
IA-32 Architecture Compatibility

CPUID is not supported in early models of the Intel486 processor or in any IA-32 processor earlier than the Intel486 processor.

Operation

IA32_BIOS_SIGN_ID MSR ← Update with installed microcode revision number;

CASE (EAX) OF
  EAX = 0:
    EAX ← Highest basic function input value understood by CPUID;
    EBX ← Vendor identification string;
    EDX ← Vendor identification string;
    ECX ← Vendor identification string;
  BREAK;
  EAX = 1H:
    EAX[3:0] ← Stepping ID;
    EAX[7:4] ← Model;
    EAX[11:8] ← Family;
    EAX[13:12] ← Processor type;
    EAX[15:14] ← Reserved;
    EAX[19:16] ← Extended Model;
    EAX[27:20] ← Extended Family;
    EAX[31:28] ← Reserved;
    EBX[7:0] ← Brand Index; (* Reserved if the value is zero. *)
    EBX[15:8] ← CLFLUSH Line Size;
    EBX[16:23] ← Reserved; (* Number of threads enabled = 2 if MT enable fuse set. *)
    EBX[24:31] ← Initial APIC ID;
    ECX ← Feature flags; (* See Figure 3-6. *)
    EDX ← Feature flags; (* See Figure 3-7. *)
  BREAK;
  EAX = 2H:
    EAX ← Cache and TLB information;
    EBX ← Cache and TLB information;
    ECX ← Cache and TLB information;
    EDX ← Cache and TLB information;
  BREAK;
  EAX = 3H:
    EAX ← Reserved;
    EBX ← Reserved;
    ECX ← ProcessorSerialNumber[31:0];
    (* Pentium III processors only, otherwise reserved. *)
    EDX ← ProcessorSerialNumber[63:32];
    (* Pentium III processors only, otherwise reserved. *)
BREAK

EAX = 4H:
EAX ← Deterministic Cache Parameters Leaf; (* See Table 3-17. *)
EBX ← Deterministic Cache Parameters Leaf;
ECX ← Deterministic Cache Parameters Leaf;
EDX ← Deterministic Cache Parameters Leaf;
BREAK;

EAX = 5H:
EAX ← MONITOR/MWAIT Leaf; (* See Table 3-17. *)
EBX ← MONITOR/MWAIT Leaf;
ECX ← MONITOR/MWAIT Leaf;
EDX ← MONITOR/MWAIT Leaf;
BREAK;

EAX = 6H:
EAX ← Thermal and Power Management Leaf; (* See Table 3-17. *)
EBX ← Thermal and Power Management Leaf;
ECX ← Thermal and Power Management Leaf;
EDX ← Thermal and Power Management Leaf;
BREAK;

EAX = 7H:
EAX ← Structured Extended Feature Flags Enumeration Leaf; (* See Table 3-17. *)
EBX ← Structured Extended Feature Flags Enumeration Leaf;
ECX ← Structured Extended Feature Flags Enumeration Leaf;
EDX ← Structured Extended Feature Flags Enumeration Leaf;
BREAK;

EAX = 8H:
EAX ← Reserved = 0;
EBX ← Reserved = 0;
ECX ← Reserved = 0;
EDX ← Reserved = 0;
BREAK;

EAX = 9H:
EAX ← Direct Cache Access Information Leaf; (* See Table 3-17. *)
EBX ← Direct Cache Access Information Leaf;
ECX ← Direct Cache Access Information Leaf;
EDX ← Direct Cache Access Information Leaf;
BREAK;

EAX = AH:
EAX ← Architectural Performance Monitoring Leaf; (* See Table 3-17. *)
EBX ← Architectural Performance Monitoring Leaf;
ECX ← Architectural Performance Monitoring Leaf;
EDX ← Architectural Performance Monitoring Leaf;
BREAK
EAX = BH:
   EAX ← Extended Topology Enumeration Leaf; (* See Table 3-17. *)
   EBX ← Extended Topology Enumeration Leaf;
   ECX ← Extended Topology Enumeration Leaf;
   EDX ← Extended Topology Enumeration Leaf;
BREAK;
EAX = CH:
   EAX ← Reserved = 0;
   EBX ← Reserved = 0;
   ECX ← Reserved = 0;
   EDX ← Reserved = 0;
BREAK;
EAX = DH:
   EAX ← Processor Extended State Enumeration Leaf; (* See Table 3-17. *)
   EBX ← Processor Extended State Enumeration Leaf;
   ECX ← Processor Extended State Enumeration Leaf;
   EDX ← Processor Extended State Enumeration Leaf;
BREAK;
BREAK;
EAX = 80000000H:
   EAX ← Highest extended function input value understood by CPUID;
   EBX ← Reserved;
   ECX ← Reserved;
   EDX ← Reserved;
BREAK;
EAX = 80000001H:
   EAX ← Reserved;
   EBX ← Reserved;
   ECX ← Extended Feature Bits (* See Table 3-17.);
   EDX ← Extended Feature Bits (* See Table 3-17. );
BREAK;
EAX = 80000002H:
   EAX ← Processor Brand String;
   EBX ← Processor Brand String, continued;
   ECX ← Processor Brand String, continued;
   EDX ← Processor Brand String, continued;
BREAK;
EAX = 80000003H:
   EAX ← Processor Brand String, continued;
   EBX ← Processor Brand String, continued;
   ECX ← Processor Brand String, continued;
   EDX ← Processor Brand String, continued;
BREAK;
EAX = 80000004H:
    EAX ← Processor Brand String, continued;
    EBX ← Processor Brand String, continued;
    ECX ← Processor Brand String, continued;
    EDX ← Processor Brand String, continued;
BREAK;

EAX = 80000005H:
    EAX ← Reserved = 0;
    EBX ← Reserved = 0;
    ECX ← Reserved = 0;
    EDX ← Reserved = 0;
BREAK;

EAX = 80000006H:
    EAX ← Reserved = 0;
    EBX ← Reserved = 0;
    ECX ← Cache information;
    EDX ← Reserved = 0;
BREAK;

EAX = 80000007H:
    EAX ← Reserved = 0;
    EBX ← Reserved = 0;
    ECX ← Reserved = 0;
    EDX ← Reserved = Misc Feature Flags;
BREAK;

EAX = 80000008H:
    EAX ← Reserved = Physical Address Size Information;
    EBX ← Reserved = Virtual Address Size Information;
    ECX ← Reserved = 0;
    EDX ← Reserved = 0;
BREAK;

EAX >= 40000000H and EAX <= 4FFFFFFFH:
    DEFAULT: (* EAX = Value outside of recognized range for CPUID. *)
    (* If the highest basic information leaf data depend on ECX input value, ECX is honored.*)
    EAX ← Reserved; (* Information returned for highest basic information leaf.*)
    EBX ← Reserved; (* Information returned for highest basic information leaf.*)
    ECX ← Reserved; (* Information returned for highest basic information leaf.*)
    EDX ← Reserved; (* Information returned for highest basic information leaf.*)
BREAK;
ESAC;

Flags Affected
None.
Exceptions (All Operating Modes)

#UD If the LOCK prefix is used.

In earlier IA-32 processors that do not support the CPUID instruction, execution of the instruction results in an invalid opcode (#UD) exception being generated.
CRC32 — Accumulate CRC32 Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 3B F0 /r</td>
<td>CRC32 r32, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Accumulate CRC32 on r/m8.</td>
</tr>
<tr>
<td>F2 REX OF 3B F0 /r</td>
<td>CRC32 r32, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Accumulate CRC32 on r/m8.</td>
</tr>
<tr>
<td>F2 0F 3B F1 /r</td>
<td>CRC32 r32, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Accumulate CRC32 on r/m16.</td>
</tr>
<tr>
<td>F2 0F 3B F1 /r</td>
<td>CRC32 r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Accumulate CRC32 on r/m32.</td>
</tr>
<tr>
<td>F2 REX.W 0F 3B F0 /r</td>
<td>CRC32 r64, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Accumulate CRC32 on r/m8.</td>
</tr>
<tr>
<td>F2 REX.W 0F 3B F1 /r</td>
<td>CRC32 r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Accumulate CRC32 on r/m64.</td>
</tr>
</tbody>
</table>

NOTES:
*In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Starting with an initial value in the first operand (destination operand), accumulates a CRC32 (polynomial 0x11EDC6F41) value for the second operand (source operand) and stores the result in the destination operand. The source operand can be a register or a memory location. The destination operand must be an r32 or r64 register. If the destination is an r64 register, then the 32-bit result is stored in the least significant double word and 00000000H is stored in the most significant double word of the r64 register.

The initial value supplied in the destination operand is a double word integer stored in the r32 register or the least significant double word of the r64 register. To incrementally accumulate a CRC32 value, software retains the result of the previous CRC32 operation in the destination operand, then executes the CRC32 instruction again with new input data in the source operand. Data contained in the source operand is processed in reflected bit order. This means that the most significant bit of the source operand is treated as the least significant bit of the quotient, and so on, for all the bits of the source operand. Likewise, the result of the CRC operation is stored in the destination operand in reflected bit order. This means that the most significant bit of the resulting CRC (bit 31) is stored in the least significant bit of the destination operand (bit 0), and so on, for all the bits of the CRC.
CRC32 instruction for 64-bit source operand and 64-bit destination operand:

\[
\begin{align*}
\text{TEMP1}[63:0] & \leftarrow \text{BIT REFLECT64 (SRC}[63:0]) \\
\text{TEMP2}[31:0] & \leftarrow \text{BIT REFLECT32 (DEST}[31:0]) \\
\text{TEMP3}[95:0] & \leftarrow \text{TEMP1}[63:0] \ll 32 \\
\text{TEMP4}[95:0] & \leftarrow \text{TEMP2}[31:0] \ll 64 \\
\text{TEMP5}[95:0] & \leftarrow \text{TEMP3}[95:0] \text{ XOR TEMP4}[95:0] \\
\text{TEMP6}[31:0] & \leftarrow \text{TEMP5}[95:0] \text{ MOD2 } 11EDC6F41H \\
\text{DEST}[31:0] & \leftarrow \text{BIT REFLECT (TEMP6}[31:0]) \\
\text{DEST}[63:32] & \leftarrow 00000000H
\end{align*}
\]

CRC32 instruction for 32-bit source operand and 32-bit destination operand:

\[
\begin{align*}
\text{TEMP1}[31:0] & \leftarrow \text{BIT REFLECT32 (SRC}[31:0]) \\
\text{TEMP2}[31:0] & \leftarrow \text{BIT REFLECT32 (DEST}[31:0]) \\
\text{TEMP3}[63:0] & \leftarrow \text{TEMP1}[31:0] \ll 32 \\
\text{TEMP4}[63:0] & \leftarrow \text{TEMP2}[31:0] \ll 32 \\
\text{TEMP5}[63:0] & \leftarrow \text{TEMP3}[63:0] \text{ XOR TEMP4}[63:0] \\
\text{TEMP6}[31:0] & \leftarrow \text{TEMP5}[63:0] \text{ MOD2 } 11EDC6F41H \\
\text{DEST}[31:0] & \leftarrow \text{BIT REFLECT (TEMP6}[31:0])
\end{align*}
\]

CRC32 instruction for 16-bit source operand and 32-bit destination operand:

\[
\begin{align*}
\text{TEMP1}[15:0] & \leftarrow \text{BIT REFLECT16 (SRC}[15:0]) \\
\text{TEMP2}[31:0] & \leftarrow \text{BIT REFLECT32 (DEST}[31:0]) \\
\text{TEMP3}[47:0] & \leftarrow \text{TEMP1}[15:0] \ll 32 \\
\text{TEMP4}[47:0] & \leftarrow \text{TEMP2}[31:0] \ll 16 \\
\text{TEMP5}[47:0] & \leftarrow \text{TEMP3}[47:0] \text{ XOR TEMP4}[47:0] \\
\text{TEMP6}[31:0] & \leftarrow \text{TEMP5}[47:0] \text{ MOD2 } 11EDC6F41H \\
\text{DEST}[31:0] & \leftarrow \text{BIT REFLECT (TEMP6}[31:0])
\end{align*}
\]

CRC32 instruction for 8-bit source operand and 64-bit destination operand:

\[
\begin{align*}
\text{TEMP1}[7:0] & \leftarrow \text{BIT REFLECT8 (SRC}[7:0]) \\
\text{TEMP2}[31:0] & \leftarrow \text{BIT REFLECT32 (DEST}[31:0]) \\
\text{TEMP3}[39:0] & \leftarrow \text{TEMP1}[7:0] \ll 32 \\
\text{TEMP4}[39:0] & \leftarrow \text{TEMP2}[31:0] \ll 8 \\
\text{TEMP5}[39:0] & \leftarrow \text{TEMP3}[39:0] \text{ XOR TEMP4}[39:0]
\end{align*}
\]
Temp6[31-0] ← Temp5[39-0] MOD2 11EDC6F41H
Dest[31-0] ← Bit_Reflect (Temp6[31-0])
Dest[63-32] ← 00000000H

CRC32 instruction for 8-bit source operand and 32-bit destination operand:

Temp1[7-0] ← Bit_Reflect8(Src[7-0])
Temp2[31-0] ← Bit_Reflect32 (Dest[31-0])
Temp3[39-0] ← Temp1[7-0] « 32
Temp4[39-0] ← Temp2[31-0] « 8
Temp6[31-0] ← Temp5[39-0] MOD2 11EDC6F41H
Dest[31-0] ← Bit_Reflect (Temp6[31-0])

Flags Affected
None

Intel C/C++ Compiler Intrinsic Equivalent

unsigned int _mm_crc32_u8( unsigned int crc, unsigned char data )
unsigned int _mm_crc32_u16( unsigned int crc, unsigned short data )
unsigned int _mm_crc32_u32( unsigned int crc, unsigned int data )
unsigned __int64 _mm_crc32_u64( unsigned __int64 crc, unsigned __int64 data )

SIMD Floating Point Exceptions
None

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segments.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF (fault-code) For a page fault.
#UD If CPUID.01H:ECX.SSE4_2 [Bit 20] = 0.
If LOCK prefix is used.

Real Mode Exceptions

#GP(0) If any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If CPUID.01H:ECX.SSE4_2 [Bit 20] = 0.
If LOCK prefix is used.
Virtual 8086 Mode Exceptions

#GP(0) If any part of the operand lies outside of the effective address space from 0 to 0FFFFH.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF (fault-code) For a page fault.
#UD If CPUID.01H:ECX.SSE4_2 [Bit 20] = 0.
If LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in Protected Mode.

64-Bit Mode Exceptions

#GP(0) If the memory address is in a non-canonical form.
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#PF (fault-code) For a page fault.
#UD If CPUID.01H:ECX.SSE4_2 [Bit 20] = 0.
If LOCK prefix is used.
**CVTDQ2PD—Convert Packed Dword Integers to Packed Double-Precision FP Values**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F E6 CVTDQ2PD xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Convert two packed signed doubleword integers from xmm2/m128 to two packed double-precision floating-point values in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.F3.0F:WIG E6 /r VCVTDQ2PD xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Convert two packed signed doubleword integers from xmm2/mem to two packed double-precision floating-point values in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.F3.0F:WIG E6 /r VCVTDQ2PD ymm1, ymm2/m128</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Convert four packed signed doubleword integers from ymm2/mem to four packed double-precision floating-point values in ymm1.</td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Converts two packed signed doubleword integers in the source operand (second operand) to two packed double-precision floating-point values in the destination operand (first operand).

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source operand is an XMM register or 64-bit memory location. The destination operation is an XMM register. The upper bits (VMAX-1:128) of the corresponding XMM register destination are unmodified.

VEX.128 encoded version: The source operand is an XMM register or 64-bit memory location. The destination operation is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or 128-bit memory location. The destination operation is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.
Figure 3-10. CVTDQ2PD (VEX.256 encoded version)

**Operation**

**CVTDQ2PD (128-bit Legacy SSE version)**
- DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[31:0])
- DEST[127:64] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[63:32])
- DEST[VLMAX-1:128] (unmodified)

**VCVTDQ2PD (VEX.128 encoded version)**
- DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[31:0])
- DEST[127:64] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[63:32])
- DEST[VLMAX-1:128] ← 0

**VCVTDQ2PD (VEX.256 encoded version)**
- DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[31:0])
- DEST[127:64] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[63:32])
- DEST[191:128] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[95:64])
- DEST[255:192] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[127:96])

**Intel C/C++ Compiler Intrinsic Equivalent**
- CVTDQ2PD: __m128d _mm_cvtepi32_pd(__m128i a)
- VCVTDQ2PD: __m256d _mm256_cvtepi32_pd(__m128i src)

**SIMD Floating-Point Exceptions**
- None.

**Other Exceptions**
- See Exceptions Type 5; additionally

---

CVTDQ2PD—Convert Packed Dword Integers to Packed Double-Precision FP Values
#UD If VEX.vvvv != 1111B.
CVTDQ2PS—Convert Packed Dword Integers to Packed Single-Precision FP Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVTDQ2PS xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Convert four packed signed doubleword integers from xmm2/m128 to four packed single-precision floating-point values in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F.WIG 5B /r</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Convert four packed signed doubleword integers from xmm2/mem to four packed single-precision floating-point values in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.0F.WIG 5B /r</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Convert eight packed signed doubleword integers from ymm2/mem to eight packed single-precision floating-point values in ymm1.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Converts four packed signed doubleword integers in the source operand (second operand) to four packed single-precision floating-point values in the destination operand (first operand).

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source operand is an XMM register or 128-bit memory location. The destination operation is an XMM register. The upper bits (VMAX-1:128) of the corresponding XMM register destination are unmodified.

VEX.128 encoded version: The source operand is an XMM register or 128-bit memory location. The destination operation is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or 256-bit memory location. The destination operation is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.
INSTRUCTION SET REFERENCE, A-L

Operation

CVTDQ2PS (128-bit Legacy SSE version)
DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[31:0])
DEST[63:32] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[63:32])
DEST[95:64] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[95:64])
DEST[127:96] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[127:96])
DEST[VLMAX-1:128] (unmodified)

VCVTDQ2PS (VEX.128 encoded version)
DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[31:0])
DEST[63:32] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[63:32])
DEST[95:64] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[95:64])
DEST[127:96] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[127:96])
DEST[VLMAX-1:128] ← 0

VCVTDQ2PS (VEX.256 encoded version)
DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[31:0])
DEST[63:32] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[63:32])
DEST[95:64] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[95:64])
DEST[127:96] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[127:96])
DEST[159:128] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[159:128])
DEST[191:160] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[191:160])
DEST[223:192] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[223:192])
DEST[255:224] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[255:224])

Intel C/C++ Compiler Intrinsic Equivalent
CVTDQ2PS: __m128 _mm_cvtepi32_ps(__m128i a)
VCVTDQ2PS: __m256 _mm256_cvtepi32_ps (__m256i src)

SIMD Floating-Point Exceptions

Precision.

Other Exceptions
See Exceptions Type 2; additionally
#UD If VEX.vvvv != 1111B.
**CVTPD2DQ—Convert Packed Double-Precision FP Values to Packed Dword Integers**

**Opcode/Instruction** | Op/En | 64/32-bit Mode | CPUID Feature Flag | Description
--- | --- | --- | --- | ---
F2 0F E6 CVTPD2DQ xmm1, xmm2/m128 | RM | V/V | SSE2 | Convert two packed double-precision floating-point values from xmm2/m128 to two packed signed doubleword integers in xmm1.

VEX.128.F2.0F:W1G E6 /r VCVTPD2DQ xmm1, xmm2/m128 | RM | V/V | AVX | Convert two packed double-precision floating-point values in xmm2/mem to two signed doubleword integers in xmm1.

VEX.256.F2.0F:W1G E6 /r VCVTPD2DQ xmm1, ymm2/m256 | RM | V/V | AVX | Convert four packed double-precision floating-point values in ymm2/mem to four signed doubleword integers in xmm1.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:rm (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Converts two packed double-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The result is stored in the low quadword of the destination operand and the high quadword is cleared to all 0s.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source operand is an XMM register or 128-bit memory location. The destination operation is an XMM register. Bits[127:64] of the
destination XMM register are zeroed. However, the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: The source operand is an XMM register or 128-bit memory location. The destination operation is a YMM register. The upper bits (VLMAX-1:64) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or 256-bit memory location. The destination operation is an XMM register. The upper bits (255:128) of the corresponding YMM register destination are zeroed.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

![Figure 3-11. VCVTPD2DQ (VEX.256 encoded version)](image)

**Operation**

**CVTPD2DQ (128-bit Legacy SSE version)**
- DEST[31:0] \(\leftarrow\) Convert_Double_Precision_Floating_Point_To_Integer(SRC[63:0])
- DEST[63:32] \(\leftarrow\) Convert_Double_Precision_Floating_Point_To_Integer(SRC[127:64])
- DEST[127:64] \(\leftarrow\) 0
- DEST[VLMAX-1:128] (unmodified)

**VCVTPD2DQ (VEX.128 encoded version)**
- DEST[31:0] \(\leftarrow\) Convert_Double_Precision_Floating_Point_To_Integer(SRC[63:0])
- DEST[63:32] \(\leftarrow\) Convert_Double_Precision_Floating_Point_To_Integer(SRC[127:64])
- DEST[VLMAX-1:64] \(\leftarrow\) 0

**VCVTPD2DQ (VEX.256 encoded version)**
- DEST[31:0] \(\leftarrow\) Convert_Double_Precision_Floating_Point_To_Integer(SRC[63:0])
- DEST[63:32] \(\leftarrow\) Convert_Double_Precision_Floating_Point_To_Integer(SRC[127:64])
DEST[95:64] ← Convert_Double_Precision_Floating_Point_To_Integer(SRC[191:128])
DEST[127:96] ← Convert_Double_Precision_Floating_Point_To_Integer(SRC[255:192])
DEST[255:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
CVTPD2DQ: __m128i _mm_cvtpd_epi32 (__m128d src)
CVTPD2DQ: __m128i _mm256_cvtpd_epi32 (__m256d src)

SIMD Floating-Point Exceptions
Invalid, Precision.

Other Exceptions
See Exceptions Type 2; additionally
#UD If VEX.vvvv != 1111B.
INSTRUCTION SET REFERENCE, A-L

CVTPD2PI—Convert Packed Double-Precision FP Values to Packed Dword Integers

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 2D /r</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two packed double-precision floating-point values from xmm/m128 to two packed signed doubleword integers in mm.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>InstructionOperand Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Op/En</td>
</tr>
<tr>
<td>RM</td>
</tr>
</tbody>
</table>

**Description**

Converts two packed double-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an MMX technology register.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTPD2PI instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer32(SRC[63:0]);
DEST[63:32] ← Convert_Double_Precision_Floating_Point_To_Integer32(SRC[127:64]);

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTPD1PI: __m64 _mm_cvtpd_pi32(__m128d a)
**SIMD Floating-Point Exceptions**
Invalid, Precision.

**Other Exceptions**
See Table 22-4, "Exception Conditions for Legacy SIMD/MMX Instructions with FP Exception and 16-Byte Alignment," in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B.
**CVTPD2PS—Convert Packed Double-Precision FP Values to Packed Single-Precision FP Values**

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Converts two packed double-precision floating-point values in the source operand (second operand) to two packed single-precision floating-point values in the destination operand (first operand).

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source operand is an XMM register or 128-bit memory location. The destination operation is an XMM register. Bits[127:64] of the destination XMM register are zeroed. However, the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.
VEX.128 encoded version: The source operand is an XMM register or 128-bit memory location. The destination operation is a YMM register. The upper bits (VLMAX-1:64) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or 256-bit memory location. The destination operation is an XMM register. The upper bits (255:128) of the corresponding YMM register destination are zeroed.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Figure 3-12. VCVTPD2PS (VEX.256 encoded version)**

**Operation**

**CVTPD2PS (128-bit Legacy SSE version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{Convert\_Double\_Precision\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[63:0]) \\
\text{DEST}[63:32] & \leftarrow \text{Convert\_Double\_Precision\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[127:64]) \\
\text{DEST}[127:64] & \leftarrow 0 \\
\text{DEST}[\text{VLMAX}-1:128] & \text{ (unmodified)}
\end{align*}
\]

**VCVTPD2PS (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{Convert\_Double\_Precision\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[63:0]) \\
\text{DEST}[63:32] & \leftarrow \text{Convert\_Double\_Precision\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[127:64]) \\
\text{DEST}[95:64] & \leftarrow \text{Convert\_Double\_Precision\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[191:128]) \\
\text{DEST}[127:96] & \leftarrow \text{Convert\_Double\_Precision\_To\_Single\_Precision\_Floating\_Point}(\text{SRC}[255:192])
\end{align*}
\]

CVTPD2PS—Convert Packed Double-Precision FP Values to Packed Single-Precision FP Values
INSTRUCTION SET REFERENCE, A-L

DEST[255:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTPD2PS: __m128 _mm_cvtpd_ps(__m128d a)
CVTPD2PS: __m256 _mm256_cvtpd_ps (__m256d a)

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**

See Exceptions Type 2; additionally

#UD If VEX.vvvv ≠ 1111B.
CVTPI2PD—Convert Packed Dword Integers to Packed Double-Precision FP Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 2A /r</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two packed signed doubleword integers from mm/mem64 to two packed double-precision floating-point values in xmm.</td>
</tr>
</tbody>
</table>

CVTPI2PD xmm, mm/m64*

NOTES:
*Operation is different for different operand sets; see the Description section.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Converts two packed signed doubleword integers in the source operand (second operand) to two packed double-precision floating-point values in the destination operand (first operand).

The source operand can be an MMX technology register or a 64-bit memory location. The destination operand is an XMM register. In addition, depending on the operand configuration:

- **For operands xmm, mm:** the instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTPI2PD instruction is executed.

- **For operands xmm, m64:** the instruction does not cause a transition to MMX technology and does not take x87 FPU exceptions.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Operation

DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[31:0]);
DEST[127:64] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[63:32]);

Intel C/C++ Compiler Intrinsic Equivalent

CVTPI2PD: __m128d __mm_cvtpi32_pd(__m64 a)
SIMD Floating-Point Exceptions

Precision.

Other Exceptions

See Table 22-6, "Exception Conditions for Legacy SIMD/MMX Instructions with XMM and without FP Exception," in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B.*
CVTPi2Ps—Convert Packed Dword Integers to Packed Single-Precision FP Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 2A /r CVTPi2Ps xmm, m64</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Convert two signed doubleword integers from xmm/m64 to two single-precision floating-point values in xmm.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM reg (w)</td>
<td>ModRM r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Converts two packed signed doubleword integers in the source operand (second operand) to two packed single-precision floating-point values in the destination operand (first operand).

The source operand can be an MMX technology register or a 64-bit memory location. The destination operand is an XMM register. The results are stored in the low quadword of the destination operand, and the high quadword remains unchanged. When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTPi2Ps instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[31:0]);
DEST[63:32] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[63:32]);

(*) High quadword of destination unchanged *)

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTPi2Ps: _mm128_mm_cvtpi32_ps(_m128 a, _m64 b)
SIMD Floating-Point Exceptions

Precision.

Other Exceptions

See Table 22-5, "Exception Conditions for Legacy SIMD/MMX Instructions with XMM and FP Exception," in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B.
CVTPS2DQ—Convert Packed Single-Precision FP Values to Packed Dword Integers

**Opcode/Instruction**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 5B /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Convert four packed single-precision floating-point values from xmm2/m128 to four packed signed doubleword integers in xmm1.</td>
</tr>
<tr>
<td>CVTPS2DQ xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F:W1G 5B /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert eight packed single precision floating-point values from ymm2/mem to eight packed signed doubleword values in ymm1.</td>
</tr>
<tr>
<td>VCVTPS2DQ ymm1, ymm2/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Converts four or eight packed single-precision floating-point values in the source operand to four or eight signed doubleword integers in the destination operand.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source operand is an XMM register or 128-bit memory location. The destination operation is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: The source operand is an XMM register or 128-bit memory location. The destination operation is a YMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.
VEX.256 encoded version: The source operand is a YMM register or 256-bit memory location. The destination operation is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

**CVTPS2DQ (128-bit Legacy SSE version)**

DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0])
DEST[63:32] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[63:32])
DEST[95:64] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[95:64])
DEST[127:96] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[127:96])
DEST[VLMAX-1:128] (unmodified)

**VCVTPS2DQ (VEX.128 encoded version)**

DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0])
DEST[63:32] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[63:32])
DEST[95:64] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[95:64])
DEST[127:96] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[127:96])
DEST[VLMAX-1:128] ← 0

**VCVTPS2DQ (VEX.256 encoded version)**

DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0])
DEST[63:32] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[63:32])
DEST[95:64] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[95:64])
DEST[127:96] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[127:96])
DEST[159:128] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[159:128])
DEST[191:160] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[191:160])
DEST[223:192] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[223:192])
DEST[255:224] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[255:224])

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTPS2DQ:  __m128i _mm_cvtps_epi32(__m128 a)
VCVTPS2DQ:  __m256i _mm256_cvtps_epi32 (__m256 a)

**SIMD Floating-Point Exceptions**

Invalid, Precision.

**Other Exceptions**

See Exceptions Type 2; additionally

#UD          If VEX.vvvv != 1111B.
CVTPS2PD—Convert Packed Single-Precision FP Values to Packed Double-Precision FP Values

**Opcode/Instruction** | Op/En | 64/32-bit Mode | CPUID Feature Flag | Description
--- | --- | --- | --- | ---
0F 5A /r CVTPS2PD xmm1, xmm2/m64 | RM V/V | SSE2 | Convert two packed single-precision floating-point values in xmm2/m64 to two packed double-precision floating-point values in xmm1.
VEX.128.0F:WIG 5A /r VCVTPS2PD xmm1, xmm2/m64 | RM V/V | AVX | Convert two packed single-precision floating-point values in xmm2/m64 to two packed double-precision floating-point values in xmm1.
VEX.256.0F:WIG 5A /r VCVTPS2PD ymm1, xmm2/m128 | RM V/V | AVX | Convert four packed single-precision floating-point values in xmm2/m128 to four packed double-precision floating-point values in ymm1.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Converts two or four packed single-precision floating-point values in the source operand (second operand) to two or four packed double-precision floating-point values in the destination operand (first operand).

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source operand is an XMM register or 64-bit memory location. The destination operation is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: The source operand is an XMM register or 64-bit memory location. The destination operation is a YMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.
INSTRUCTION SET REFERENCE, A-L

VEX.256 encoded version: The source operand is an XMM register or 128-bit memory location. The destination operation is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

**CVTPS2PD (128-bit Legacy SSE version)**

\[
\text{DEST}[63:0] \leftarrow \text{Convert Single Precision To Double Precision Floating Point}(\text{SRC}[31:0])
\]

\[
\text{DEST}[127:64] \leftarrow \text{Convert Single Precision To Double Precision Floating Point}(\text{SRC}[63:32])
\]

\[
\text{DEST}[\text{VLMAX}-1:128] \text{(unmodified)}
\]

**VCVTPS2PD (VEX.128 encoded version)**

\[
\text{DEST}[63:0] \leftarrow \text{Convert Single Precision To Double Precision Floating Point}(\text{SRC}[31:0])
\]

\[
\text{DEST}[127:64] \leftarrow \text{Convert Single Precision To Double Precision Floating Point}(\text{SRC}[63:32])
\]

\[
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0
\]

**VCVTPS2PD (VEX.256 encoded version)**

\[
\text{DEST}[63:0] \leftarrow \text{Convert Single Precision To Double Precision Floating Point}(\text{SRC}[31:0])
\]

\[
\text{DEST}[127:64] \leftarrow \text{Convert Single Precision To Double Precision Floating Point}(\text{SRC}[63:32])
\]

\[
\text{DEST}[191:128] \leftarrow \text{Convert Single Precision To Double Precision Floating Point}(\text{SRC}[95:64])
\]

\[
\text{DEST}[255:192] \leftarrow \text{Convert Single Precision To Double Precision Floating Point}(\text{SRC}[127:96])
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTPS2PD: \texttt{__m128d _mm_cvtps_pd(__m128 a)}

VCVTPS2PD: \texttt{__m256d _mm256_cvtps_pd (__m128 a)}
**SIMD Floating-Point Exceptions**
Invalid, Denormal.

**Other Exceptions**
See Exceptions Type 3; additionally

#UDIf VEX.vvvv != 1111B.
CVTPS2PI—Convert Packed Single-Precision FP Values to Packed Dword Integers

**Description**

Converts two packed single-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand).

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an MMX technology register. When the source operand is an XMM register, the two single-precision floating-point values are contained in the low quadword of the register. When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

CVTPS2PI causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTPS2PI instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\text{DEST}[31:0] \leftarrow \text{Convert Single-Precision Floating Point To Integer}(\text{SRC}[31:0]); \\
\text{DEST}[63:32] \leftarrow \text{Convert Single-Precision Floating Point To Integer}(\text{SRC}[63:32]);
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTPS2PI: __m64 _mm_cvtps_pi32(__m128 a)
SIMD Floating-Point Exceptions
Invalid, Precision.

Other Exceptions
See Table 22-5, “Exception Conditions for Legacy SIMD/MMX Instructions with XMM and FP Exception,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B.
CVTSD2SI—Convert Scalar Double-Precision FP Value to Integer

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 2D /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Convert one double-precision floating-point value from xmm/m64 to one signed doubleword integer r32.</td>
</tr>
<tr>
<td>CVTSD2SI r32, xmm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F2 REX.W 0F 2D /r</td>
<td>RM</td>
<td>V/N.E.</td>
<td>SSE2</td>
<td>Convert one double-precision floating-point value from xmm/m64 to one signed quadword integer sign-extended into r64.</td>
</tr>
<tr>
<td>CVTSD2SI r64, xmm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F2.0F.W0 2D /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert one double precision floating-point value from xmm1/m64 to one signed doubleword integer r32.</td>
</tr>
<tr>
<td>VCVTSD2SI r32, xmm1/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F2.0F.W1 2D /r</td>
<td>RM</td>
<td>V/N.E. 1</td>
<td>AVX</td>
<td>Convert one double precision floating-point value from xmm1/m64 to one signed quadword integer sign-extended into r64.</td>
</tr>
<tr>
<td>VCVTSD2SI r64, xmm1/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. Encoding the VEX prefix with VEX.W=1 in non-64-bit mode is ignored.

Description
Converts a double-precision floating-point value in the source operand (second operand) to a signed doubleword integer in the destination operand (first operand). The source operand can be an XMM register or a 64-bit memory location. The destination operand is a general-purpose register. When the source operand is an XMM register, the double-precision floating-point value is contained in the low quadword of the register.
When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operation. See the summary chart at the beginning of this section for encoding data and limits.

Legacy SSE instructions: Use of the REX.W prefix promotes the instruction to 64-bit operation. See the summary chart at the beginning of this section for encoding data and limits.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

**Operation**

IF 64-Bit Mode and OperandSize = 64
    THEN
        DEST[63:0] ← Convert_Double_Precision_Floating_Point_To_Integer64(SRC[63:0]);
    ELSE
        DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer32(SRC[63:0]);
FI;

**Intel C/C++ Compiler Intrinsic Equivalent**

int _mm_cvtsd_si32(__m128d a)  
__int64 _mm_cvtsd_si64(__m128d a)

**SIMD Floating-Point Exceptions**

Invalid, Precision.

**Other Exceptions**

See Exceptions Type 3; additionally

#UD If VEX.vvvv != 1111B.
CVTSD2SS—Convert Scalar Double-Precision FP Value to Scalar Single-Precision FP Value

**Instruction**

```
CVTSD2SS xmm1, xmm2/m64
```

**VEX.NDS.LIG.F2.0F.WIG 5A /r**

```
VCVTSD2SS xmm1,xmm2, xmm3/m64
```

**Description**

Converts a double-precision floating-point value in the source operand (second operand) to a single-precision floating-point value in the destination operand (first operand).

The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. When the source operand is an XMM register, the double-precision floating-point value is contained in the low quadword of the register. The result is stored in the low doubleword of the destination operand, and the upper 3 doublewords are left unchanged. When the conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:64) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed.
Operation

**CVTSD2SS (128-bit Legacy SSE version)**
DEST[31:0] ← Convert_Double_Precision_To_Single_Precision_Floating_Point(SRC[63:0]);
(* DEST[VLMAX-1:32] Unmodified *)

**VCVTSD2SS (VEX.128 encoded version)**
DEST[31:0] ← Convert_Double_Precision_To_Single_Precision_Floating_Point(SRC2[63:0]);
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**
CVTSD2SS: __m128 _mm_cvtsd_ss(__m128 a, __m128d b)

**SIMD Floating-Point Exceptions**
Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**
See Exceptions Type 3.
INSTRUCTION SET REFERENCE, A-L

CVTSI2SD—Convert Dword Integer to Scalar Double-Precision FP Value

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 2A /r CVTSI2SD xmm, r/m32</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Convert one signed doubleword integer from r/m32 to one double-precision floating-point value in xmm.</td>
<td></td>
</tr>
<tr>
<td>F2 REX.W 0F 2A /r CVTSI2SD xmm, r/m64</td>
<td>RM V/N.E.</td>
<td>SSE2</td>
<td>Convert one signed quadword integer from r/m64 to one double-precision floating-point value in xmm.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F.W0 2A /r VCVTSI2SD xmm1, xmm2, r/m32</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Convert one signed doubleword integer from r/m32 to one double-precision floating-point value in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F.W1 2A /r VCVTSI2SD xmm1, xmm2, r/m64</td>
<td>RVM V/N.E.</td>
<td>AVX</td>
<td>Convert one signed quadword integer from r/m64 to one double-precision floating-point value in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. Encoding the VEX prefix with VEX.W=1 in non-64-bit mode is ignored.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Converts a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the second source operand to a double-precision floating-point value in the destination operand. The result is stored in the low quadword of the destination operand, and the high quadword left unchanged. When conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.
CVTSI2SD—Convert Dword Integer to Scalar Double-Precision FP Value

Legacy SSE instructions: Use of the REX.W prefix promotes the instruction to 64-bit operands. See the summary chart at the beginning of this section for encoding data and limits.

The second source operand can be a general-purpose register or a 32/64-bit memory location. The first source and destination operands are XMM registers.

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VLMAX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:64) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Operation

CVTSI2SD
IF 64-Bit Mode And OperandSize = 64
THEN
  DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[63:0]);
ELSE
  DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC[31:0]);
FI;
DEST[VLMAX-1:64] (Unmodified)

VCVTSI2SD
IF 64-Bit Mode And OperandSize = 64
THEN
  DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC2[63:0]);
ELSE
  DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC2[31:0]);
FI;
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent

CVTSI2SD: __m128d _mm_cvtsi32_sd(__m128d a, int b)
CVTSI2SD: __m128d _mm_cvtsi64_sd(__m128d a, __int64 b)

SIMD Floating-Point Exceptions

Precision.

Other Exceptions
See Exceptions Type 3.
CVTSI2SS—Convert Dword Integer to Scalar Single-Precision FP Value

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 2A /r CVTSI2SS xmm, r/m32</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Convert one signed doubleword integer from r/m32 to one single-precision floating-point value in xmm.</td>
<td></td>
</tr>
<tr>
<td>F3 REX.W 0F 2A /r CVTSI2SS xmm, r/m64</td>
<td>RM V/N.E.</td>
<td>SSE</td>
<td>Convert one signed quadword integer from r/m64 to one single-precision floating-point value in xmm.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.W0 2A /r VCVTSI2SS xmm1, xmm2, r/m32</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Convert one signed doubleword integer from r/m32 to one single-precision floating-point value in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.W1 2A /r VCVTSI2SS xmm1, xmm2, r/m64</td>
<td>RVM V/N.E.¹</td>
<td>AVX</td>
<td>Convert one signed quadword integer from r/m64 to one single-precision floating-point value in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. Encoding the VEX prefix with VEX.W=1 in non-64-bit mode is ignored.

InstructionOperand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM/reg (w)</td>
<td>ModRM/r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM/reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM/r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Converts a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the source operand (second operand) to a single-precision floating-point value in the destination operand (first operand). The source operand can be a general-purpose register or a memory location. The destination operand is an XMM register. The result is stored in the low doubleword of the destination operand, and the upper three doublewords are left unchanged. When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register.
Legacy SSE instructions: In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operands. See the summary chart at the beginning of this section for encoding data and limits.

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:32) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

**CVTSI2SS (128-bit Legacy SSE version)**

IF 64-Bit Mode And OperandSize = 64
THEN
   DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[63:0]);
ELSE
   DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[31:0]);
FI;
DEST[VLMAX-1:32] (Unmodified)

**VCVTSI2SS (VEX.128 encoded version)**

IF 64-Bit Mode And OperandSize = 64
THEN
   DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[63:0]);
ELSE
   DEST[31:0] ← Convert_Integer_To_Single_Precision_Floating_Point(SRC[31:0]);
FI;
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTSI2SS:  __m128  _mm_cvtsi32_ss(__m128  a, int b)
CVTSI2SS:  __m128  _mm_cvtsi64_ss(__m128  a, __int64 b)

**SIMD Floating-Point Exceptions**

Precision.

**Other Exceptions**

See Exceptions Type 3.
CVTSS2SD—Convert Scalar Single-Precision FP Value to Scalar Double-Precision FP Value

### Opcode/Description

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 OF 5A /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Convert one single-precision floating-point value in xmm2/m32 to one double-precision floating-point value in xmm1.</td>
</tr>
<tr>
<td>CVTSS2SD xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.WIG 5A /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert one single-precision floating-point value in xmm3/m32 to one double-precision floating-point value and merge with high bits of xmm2.</td>
</tr>
<tr>
<td>VCVTSS2SD xmm1, xmm2, xmm3/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Converts a single-precision floating-point value in the source operand (second operand) to a double-precision floating-point value in the destination operand (first operand). The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. When the source operand is an XMM register, the single-precision floating-point value is contained in the low doubleword of the register. The result is stored in the low quadword of the destination operand, and the high quadword is left unchanged.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VMAX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:64) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VMAX-1:128) of the destination YMM register are zeroed.

### Operation

**CVTSS2SD (128-bit Legacy SSE version)**
**CVTSS2SD** (VEX.128 encoded version)

DEST[63:0] ← Convert_Single_Precision_To_Double_Precision_Floating_Point(SRC[31:0])

DEST[VLMAX-1:64] (Unmodified)

DEST[63:0] ← Convert_Single_Precision_To_Double_Precision_Floating_Point(SRC2[31:0])

DEST[127:64] ← SRC1[127:64]

DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTSS2SD: _m128d _mm_cvtss_sd(_m128d a, _m128d b)

**SIMD Floating-Point Exceptions**

Invalid, Denormal.

**Other Exceptions**

See Exceptions Type 3.
**CVTSS2SI—Convert Scalar Single-Precision FP Value to Dword Integer**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 2D /r CVTSS2SI r32, xmm/m32</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Convert one single-precision floating-point value from xmm/m32 to one signed doubleword integer in r32.</td>
</tr>
<tr>
<td>F3 REX.W 0F 2D /r CVTSS2SI r64, xmm/m32</td>
<td>RM</td>
<td>V/N.E.</td>
<td>SSE</td>
<td>Convert one single-precision floating-point value from xmm/m32 to one signed quadword integer in r64.</td>
</tr>
<tr>
<td>VEX.LIG.F3.0F.W0 2D /r VCVTSS2SI r32, xmm1/m32</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert one single-precision floating-point value from xmm1/m32 to one signed doubleword integer in r32.</td>
</tr>
<tr>
<td>VEX.LIG.F3.0F.W1 2D /r VCVTSS2SI r64, xmm1/m32</td>
<td>RM</td>
<td>V/N.E.</td>
<td>AVX</td>
<td>Convert one single-precision floating-point value from xmm1/m32 to one signed quadword integer in r64.</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Encoding the VEX prefix with VEX.W=1 in non-64-bit mode is ignored.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

**Description**

Converts a single-precision floating-point value in the source operand (second operand) to a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the destination operand (first operand). The source operand can be an XMM register or a memory location. The destination operand is a general-purpose register. When the source operand is an XMM register, the single-precision floating-point value is contained in the low doubleword of the register.

When a conversion is inexact, the value returned is rounded according to the rounding control bits in the MXCSR register. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the
INSTRUCTION SET REFERENCE, A-L

CVTSS2SI—Convert Scalar Single-Precision FP Value to Dword Integer

Instruction to 64-bit operands. See the summary chart at the beginning of this section for encoding data and limits.

Legacy SSE instructions: In 64-bit mode, Use of the REX.W prefix promotes the instruction to 64-bit operands. See the summary chart at the beginning of this section for encoding data and limits.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

Operation

IF 64-bit Mode and OperandSize = 64
    THEN
        DEST[64:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0]);
    ELSE
        DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer(SRC[31:0]);
    FI;

Intel C/C++ Compiler Intrinsic Equivalent

int _mm_cvtss_si32(__m128d a)
__int64 _mm_cvtss_si64(__m128d a)

SIMD Floating-Point Exceptions

Invalid, Precision.

Other Exceptions

See Exceptions Type 3; additionally

#UD If VEX.vvvv != 1111B.
**CVTTPD2DQ—Convert with Truncation Packed Double-Precision FP Values to Packed Dword Integers**

### Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F E6</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Convert two packed double-precision floating-point values from <code>xmm2/m128</code> to two packed signed doubleword integers in <code>xmm1</code> using truncation.</td>
</tr>
<tr>
<td>VEX.128.66.0F.WIG E6 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert two packed double-precision floating-point values in <code>xmm2/mem</code> to two signed doubleword integers in <code>xmm1</code> using truncation.</td>
</tr>
<tr>
<td>VEX.256.66.0F.WIG E6 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert four packed double-precision floating-point values in <code>ymm2/mem</code> to four signed doubleword integers in <code>xmm1</code> using truncation.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Converts two or four packed double-precision floating-point values in the source operand (second operand) to two or four packed signed doubleword integers in the destination operand (first operand).

When a conversion is inexact, a truncated (round toward zero) value is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source operand is an XMM register or 128-bit memory location. The destination operation is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified.
VEX.128 encoded version: The source operand is an XMM register or 128-bit memory location. The destination operation is a YMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or 256-bit memory location. The destination operation is an XMM register. The upper bits (255:128) of the corresponding YMM register destination are zeroed.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

**Figure 3-14. VCVTTPD2DQ (VEX.256 encoded version)**

**Operation**

**VCVTTPD2DQ (128-bit Legacy SSE version)**

DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[63:0])
DEST[63:32] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[127:64])
DEST[127:64] ← 0
DEST[VLMAX-1:128] (unmodified)

**VCVTTPD2DQ (VEX.128 encoded version)**

DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[63:0])
DEST[63:32] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[127:64])
DEST[VLMAX-1:128] ← 0

**VCVTTPD2DQ (VEX.256 encoded version)**

DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[63:0])
DEST[63:32] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[127:64])
DEST[95:64] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[191:128])
DEST[127:96] ← Convert_Double_Precision_Floating_Point_To_Integer_Truncate(SRC[255:192])

CVTTPD2DQ—Convert with Truncation Packed Double-Precision FP Values to Packed Dword Integers
INSTRUCTION SET REFERENCE, A-L

DEST[255:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**
CVTTPD2DQ:  _m128i _mm_cvttpd_epi32(_m128d a)
VCVTTPD2DQ:  _m128i _mm256_cvttpd_epi32 (__m256d src)

**SIMD Floating-Point Exceptions**
Invalid, Precision.

**Other Exceptions**
See Exceptions Type 2; additionally
#UD               If VEX.vvvv != 1111B.
**CVTTPD2PI—Convert with Truncation Packed Double-Precision FP Values to Packed Dword Integers**

**Description**

Converts two packed double-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand). The source operand can be an XMM register or a 128-bit memory location. The destination operand is an MMX technology register.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTTPD2PI instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer32_Truncate(SRC[63:0]);
DEST[63:32] ← Convert_Double_Precision_Floating_Point_To_Integer32_Truncate(SRC[127:64]);

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTTPD1PI: __m64_mm_cvtpdp_pi32(__m128d a)
**SIMD Floating-Point Exceptions**
Invalid, Precision.

**Other Mode Exceptions**
See Table 22-4, "Exception Conditions for Legacy SIMD/MMX Instructions with FP Exception and 16-Byte Alignment," in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B.
CVTTPS2DQ—Convert with Truncation Packed Single-Precision FP Values to Packed Dword Integers

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 5B /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Convert four single-precision floating-point values from xmm2/m128 to four signed doubleword integers in xmm1 using truncation.</td>
</tr>
<tr>
<td>VEX.128.F3.0F:W1G 5B /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert four packed single precision floating-point values from xmm2/mem to four packed signed doubleword values in xmm1 using truncation.</td>
</tr>
<tr>
<td>VEX.256.F3.0F:W1G 5B /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert eight packed single precision floating-point values from ymm2/mem to eight packed signed doubleword values in ymm1 using truncation.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Converts four or eight packed single-precision floating-point values in the source operand to four or eight signed doubleword integers in the destination operand.

When a conversion is inexact, a truncated (round toward zero) value is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source operand is an XMM register or 128-bit memory location. The destination operation is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.
VEX.128 encoded version: The source operand is an XMM register or 128-bit memory location. The destination operation is a YMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or 256-bit memory location. The destination operation is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

Operation

CVTTPS2DQ (128-bit Legacy SSE version)
\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[127:96]) \\
\text{DEST}[VLMAX-1:128] & \text{(unmodified)}
\end{align*}
\]

VCVTTPS2DQ (VEX.128 encoded version)
\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[127:96]) \\
\text{DEST}[VLMAX-1:128] & \leftarrow 0
\end{align*}
\]

VCVTTPS2DQ (VEX.256 encoded version)
\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[127:96]) \\
\text{DEST}[159:128] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[159:128]) \\
\text{DEST}[191:160] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[191:160]) \\
\text{DEST}[223:192] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[223:192]) \\
\text{DEST}[255:224] & \leftarrow \text{Convert\_Single\_Precision\_Floating\_Point\_To\_Integer\_Truncate}(\text{SRC}[255:224])
\end{align*}
\]

Intel C/C++ Compiler Intrinsic Equivalent

CVTTPS2DQ: __m128i _mm_cvtpps_epi32(__m128 a)
VCVTTPS2DQ: __m256i _mm256_cvtpps_epi32 (__m256 a)

SIMD Floating-Point Exceptions

Invalid, Precision.
Other Exceptions
See Exceptions Type 2; additionally
#UD If VEX.vvvv != 1111B.
CVTTPS2PI—Convert with Truncation Packed Single-Precision FP Values to Packed Dword Integers

**Description**

Converts two packed single-precision floating-point values in the source operand (second operand) to two packed signed doubleword integers in the destination operand (first operand). The source operand can be an XMM register or a 64-bit memory location. The destination operand is an MMX technology register. When the source operand is an XMM register, the two single-precision floating-point values are contained in the low quadword of the register.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-point invalid exception is raised, and if this exception is masked, the indefinite integer value (80000000H) is returned.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the CVTTPS2PI instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\text{DEST}[31:0] \leftarrow \text{Convert Single-Precision Floating Point To Integer Truncate(SRC[31:0])}; \\
\text{DEST}[63:32] \leftarrow \text{Convert Single-Precision Floating Point To Integer Truncate(SRC[63:32])};
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

CVTTPS2PI: __m64 _mm_cvttps_pi32(__m128 a)
**SIMD Floating-Point Exceptions**

Invalid, Precision.

**Other Exceptions**

See Table 22-5, "Exception Conditions for Legacy SIMD/MMX Instructions with XMM and FP Exception," in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*. 
CVTTSD2SI—Convert with Truncation Scalar Double-Precision FP Value to Signed Integer

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 2C /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Convert one double-precision floating-point value from xmm/m64 to one signed doubleword integer in r32 using truncation.</td>
</tr>
<tr>
<td>CVTTSD2SI r32, xmm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F2 REX.W 0F 2C /r</td>
<td>RM</td>
<td>V/N.E.</td>
<td>SSE2</td>
<td>Convert one double precision floating-point value from xmm/m64 to one signed quadword integer in r64 using truncation.</td>
</tr>
<tr>
<td>CVTTSD2SI r64, xmm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F2.0F.W0 2C /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert one double-precision floating-point value from xmm1/m64 to one signed doubleword integer in r32 using truncation.</td>
</tr>
<tr>
<td>VCVTTSD2SI r32, xmm1/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F2.0F.W1 2C /r</td>
<td>RM</td>
<td>V/N.E.</td>
<td>AVX</td>
<td>Convert one double-precision floating-point value from xmm1/m64 to one signed quadword integer in r64 using truncation.</td>
</tr>
<tr>
<td>VCVTTSD2SI r64, xmm1/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. Encoding the VEX prefix with VEX.W=1 in non-64-bit mode is ignored.

## Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

## Description

Converts a double-precision floating-point value in the source operand (second operand) to a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the destination operand (first operand). The source operand can be an XMM register or a 64-bit memory location. The destination operand is a general...
purpose register. When the source operand is an XMM register, the double-precision floating-point value is contained in the low quadword of the register.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating point invalid exception is raised. If this exception is masked, the indefinite integer value (80000000H) is returned.

Legacy SSE instructions: In 64-bit mode, Use of the REX.W prefix promotes the instruction to 64-bit operation. See the summary chart at the beginning of this section for encoding data and limits.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

Operation

IF 64-Bit Mode and OperandSize = 64
THEN
  DEST[63:0] ← Convert_Double_Precision_Floating_Point_To_Integer64_Truncate(SRC[63:0]);
ELSE
  DEST[31:0] ← Convert_Double_Precision_Floating_Point_To_Integer32_Truncate(SRC[63:0]);
FI;

Intel C/C++ Compiler Intrinsic Equivalent

int _mm_cvttsd_si32(__m128d a)
__int64 _mm_cvttsd_si64(__m128d a)

SIMD Floating-Point Exceptions

Invalid, Precision.

Other Exceptions

See Exceptions Type 3; additionally

#UD If VEX.vvvv != 1111B.
INSTRUCTION SET REFERENCE, A-L

CVTTSS2SI—Convert with Truncation Scalar Single-Precision FP Value to Dword Integer

### Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 2C /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Convert one single-precision floating-point value from xmm/m32 to one signed doubleword integer in r32 using truncation.</td>
</tr>
<tr>
<td>CVTTSS2SI r32, xmm/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F3 REX.W 0F 2C /r</td>
<td>RM</td>
<td>V/N.E.</td>
<td>SSE</td>
<td>Convert one single-precision floating-point value from xmm/m32 to one signed quadword integer in r64 using truncation.</td>
</tr>
<tr>
<td>CVTTSS2SI r64, xmm/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F3.0F.W0 2C /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert one single-precision floating-point value from xmm1/m32 to one signed doubleword integer in r32 using truncation.</td>
</tr>
<tr>
<td>VCVTSS2SI r32, xmm1/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F3.0F.W1 2C /r</td>
<td>RM</td>
<td>V/N.E.¹</td>
<td>AVX</td>
<td>Convert one single-precision floating-point value from xmm1/m32 to one signed quadword integer in r64 using truncation.</td>
</tr>
<tr>
<td>VCVTSS2SI r64, xmm1/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Notes:

1. Encoding the VEX prefix with VEX.W=1 in non-64-bit mode is ignored.

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Converts a single-precision floating-point value in the source operand (second operand) to a signed doubleword integer (or signed quadword integer if operand size is 64 bits) in the destination operand (first operand). The source operand can be an XMM register or a 32-bit memory location. The destination operand is a general-purpose register. When the source operand is an XMM register, the single-precision floating-point value is contained in the low doubleword of the register.

When a conversion is inexact, a truncated (round toward zero) result is returned. If a converted result is larger than the maximum signed doubleword integer, the floating-
point invalid exception is raised. If this exception is masked, the indefinite integer value (80000000H) is returned.

Legacy SSE instructions: In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. Use of the REX.W prefix promotes the instruction to 64-bit operation. See the summary chart at the beginning of this section for encoding data and limits.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

**Operation**

IF 64-Bit Mode and OperandSize = 64
    THEN
    DEST[63:0] ← Convert_Single_Precision_Floating_Point_To_Integer_Truncate(SRC[31:0]);
    ELSE
    DEST[31:0] ← Convert_Single_Precision_Floating_Point_To_Integer_Truncate(SRC[31:0]);
    FI;

**Intel C/C++ Compiler Intrinsic Equivalent**

```
int_mm_cvttss_si32(__m128d a)
__int64 _mm_cvttss_si64(__m128d a)
```

**SIMD Floating-Point Exceptions**

Invalid, Precision.

**Other Exceptions**

See Exceptions Type 3; additionally

#UD If VEX.vvvv != 1111B.
CWD/CDQ/CQO—Convert Word to Doubleword/Convert Doubleword to Quadword

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>99</td>
<td>CWD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>DX:AX ← sign-extend of AX.</td>
</tr>
<tr>
<td>99</td>
<td>CDQ</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>EDX:EAX ← sign-extend of EAX.</td>
</tr>
<tr>
<td>REX.W + 99</td>
<td>CQO</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>RDX:RAX ← sign-extend of RAX.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Doubles the size of the operand in register AX, EAX, or RAX (depending on the operand size) by means of sign extension and stores the result in registers DX:AX, EDX:EAX, or RDX:RAX, respectively. The CWD instruction copies the sign (bit 15) of the value in the AX register into every bit position in the DX register. The CDQ instruction copies the sign (bit 31) of the value in the EAX register into every bit position in the EDX register. The CQO instruction (available in 64-bit mode only) copies the sign (bit 63) of the value in the RAX register into every bit position in the RDX register.

The CWD instruction can be used to produce a doubleword dividend from a word before word division. The CDQ instruction can be used to produce a quadword dividend from a doubleword before doubleword division. The CQO instruction can be used to produce a double quadword dividend from a quadword before a quadword division.

The CWD and CDQ mnemonics reference the same opcode. The CWD instruction is intended for use when the operand-size attribute is 16 and the CDQ instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when CWD is used and to 32 when CDQ is used. Others may treat these mnemonics as synonyms (CWD/CDQ) and use the current setting of the operand-size attribute to determine the size of values to be converted, regardless of the mnemonic used.

In 64-bit mode, use of the REX.W prefix promotes operation to 64 bits. The CQO mnemonics reference the same opcode as CWD/CDQ. See the summary chart at the beginning of this section for encoding data and limits.
Operation

IF OperandSize = 16 (* CWD instruction *)
    THEN
        DX ← SignExtend(AX);
    ELSE IF OperandSize = 32 (* CDQ instruction *)
        EDX ← SignExtend(EAX); FI;
    ELSE IF 64-Bit Mode and OperandSize = 64 (* CQO instruction *)
        RDX ← SignExtend(RAX); FI;
    FI;

Flags Affected

None.

Exceptions (All Operating Modes)

#UD If the LOCK prefix is used.
DAA—Decimal Adjust AL after Addition

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Adjusts the sum of two packed BCD values to create a packed BCD result. The AL register is the implied source and destination operand. The DAA instruction is only useful when it follows an ADD instruction that adds (binary addition) two 2-digit, packed BCD values and stores a byte result in the AL register. The DAA instruction then adjusts the contents of the AL register to contain the correct 2-digit, packed BCD result. If a decimal carry is detected, the CF and AF flags are set accordingly.

This instruction executes as described above in compatibility mode and legacy mode. It is not valid in 64-bit mode.

### Operation

IF 64-Bit Mode
THEN
#UD;
ELSE
old_AL ← AL;
old_CF ← CF;
CF ← 0;
IF (((AL AND 0FH) > 9) or AF = 1)
THEN
    AL ← AL + 6;
    CF ← old_CF or (Carry from AL ← AL + 6);
    AF ← 1;
ELSE
    AF ← 0;
FI;
IF (old_AL > 99H) or (old_CF = 1))
THEN
    AL ← AL + 60H;
    CF ← 1;
ELSE
    CF ← 0;
FI;
FI;

Example
ADD     AL, BL    Before: AL=79H BL=35H EFLAGS(OSZAPC)=XXXXXX
          After: AL=AEH BL=35H EFLAGS(OSZAPC)=110000
DAA      Before: AL=AEH BL=35H EFLAGS(OSZAPC)=110000
          After: AL=14H BL=35H EFLAGS(OSZAPC)=X00111
DAA      Before: AL=2EH BL=35H EFLAGS(OSZAPC)=110000
          After: AL=34H BL=35H EFLAGS(OSZAPC)=X00101

Flags Affected
The CF and AF flags are set if the adjustment of the value results in a decimal carry in either digit of the result (see the “Operation” section above). The SF, ZF, and PF flags are set according to the result. The OF flag is undefined.

Protected Mode Exceptions
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
#UD If the LOCK prefix is used.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
INSTRUCTION SET REFERENCE, A-L

DAS—Decimal Adjust AL after Subtraction

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2F</td>
<td>DAS</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Decimal adjust AL after subtraction.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Adjusts the result of the subtraction of two packed BCD values to create a packed BCD result. The AL register is the implied source and destination operand. The DAS instruction is only useful when it follows a SUB instruction that subtracts (binary subtraction) one 2-digit, packed BCD value from another and stores a byte result in the AL register. The DAS instruction then adjusts the contents of the AL register to contain the correct 2-digit, packed BCD result. If a decimal borrow is detected, the CF and AF flags are set accordingly.

This instruction executes as described above in compatibility mode and legacy mode. It is not valid in 64-bit mode.

Operation

IF 64-Bit Mode
THEN
   #UD;
ELSE
   old_AL ← AL;
   old_CF ← CF;
   CF ← 0;
   IF (((AL AND 0FH) > 9) or AF = 1)
   THEN
      AL ← AL - 6;
      CF ← old_CF or (Borrow from AL ← AL − 6);
      AF ← 1;
   ELSE
      AF ← 0;
   FI;
   IF ((old_AL > 99H) or (old_CF = 1))
   THEN
      AL ← AL − 60H;
DAS—Decimal Adjust AL after Subtraction

```
DAD ← 1;
F1;
F1;
```

**Example**

**SUB** AL, BL  
Before: AL = 35H, BL = 47H, EFLAGS(OSZAPC) = XXXXXX  
After: AL = EEH, BL = 47H, EFLAGS(OSZAPC) = 010111

**DAA**  
Before: AL = EEH, BL = 47H, EFLAGS(OSZAPC) = 010111  
After: AL = 88H, BL = 47H, EFLAGS(OSZAPC) = X10111

**Flags Affected**

The CF and AF flags are set if the adjustment of the value results in a decimal borrow in either digit of the result (see the "Operation" section above). The SF, ZF, and PF flags are set according to the result. The OF flag is undefined.

**Protected Mode Exceptions**

#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**

#UD If the LOCK prefix is used.

**64-Bit Mode Exceptions**

#UD If in 64-bit mode.
**DEC—Decrement by 1**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE /1</td>
<td>DEC r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement r/m8 by 1.</td>
</tr>
<tr>
<td>REX + FE /1</td>
<td>DEC r/m8'</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Decrement r/m8 by 1.</td>
</tr>
<tr>
<td>FF /1</td>
<td>DEC r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement r/m16 by 1.</td>
</tr>
<tr>
<td>REX. W + FF /1</td>
<td>DEC r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Decrement r/m64 by 1.</td>
</tr>
<tr>
<td>48+rw</td>
<td>DEC r16</td>
<td>O</td>
<td>N.E.</td>
<td>Valid</td>
<td>Decrement r16 by 1.</td>
</tr>
<tr>
<td>48+rd</td>
<td>DEC r32</td>
<td>O</td>
<td>N.E.</td>
<td>Valid</td>
<td>Decrement r32 by 1.</td>
</tr>
</tbody>
</table>

**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRMrs/m (r, w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>O</td>
<td>opcode + rd (r, w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Subtracts 1 from the destination operand, while preserving the state of the CF flag. The destination operand can be a register or a memory location. This instruction allows a loop counter to be updated without disturbing the CF flag. (To perform a decrement operation that updates the CF flag, use a SUB instruction with an immediate operand of 1.)

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, DEC r16 and DEC r32 are not encodable (because opcodes 48H through 4FH are REX prefixes). Otherwise, the instruction’s 64-bit mode default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits.

See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[ \text{DEST} \leftarrow \text{DEST} - 1; \]
Flags Affected
The CF flag is not affected. The OF, SF, ZF, AF, and PF flags are set according to the result.

Protected Mode Exceptions
#GP(0) If the destination operand is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used but the destination is not a memory operand.
**DIV—Unsigned Divide**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /6</td>
<td>DIV r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned divide AX by r/m8, with result stored in AL ← Quotient, AH ← Remainder.</td>
</tr>
<tr>
<td>REX + F6 /6</td>
<td>DIV r/m8^*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide AX by r/m8, with result stored in AL ← Quotient, AH ← Remainder.</td>
</tr>
<tr>
<td>F7 /6</td>
<td>DIV r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned divide DX:AX by r/m16, with result stored in AX ← Quotient, DX ← Remainder.</td>
</tr>
<tr>
<td>F7 /6</td>
<td>DIV r/m32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned divide EDX:EAX by r/m32, with result stored in EAX ← Quotient, EDX ← Remainder.</td>
</tr>
<tr>
<td>REX.W + F7 /6</td>
<td>DIV r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide RDX:RAX by r/m64, with result stored in RAX ← Quotient, RDX ← Remainder.</td>
</tr>
</tbody>
</table>

**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

DIVides unsigned the value in the AX, DX:AX, EDX:EAX, or RDX:RAX registers (dividend) by the source operand (divisor) and stores the result in the AX (AH:AL), DX:AX, EDX:EAX, or RDX:RAX registers. The source operand can be a general-purpose register or a memory location. The action of this instruction depends on the operand size (dividend/divisor). Division using 64-bit operand is available only in 64-bit mode.

Non-integral results are truncated (chopped) towards 0. The remainder is always less than the divisor in magnitude. Overflow is indicated with the #DE (divide error) exception rather than with the CF flag.
In 64-bit mode, the instruction's default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. In 64-bit mode when REX.W is applied, the instruction divides the unsigned value in RDX:RAX by the source operand and stores the quotient in RAX, the remainder in RDX.

See the summary chart at the beginning of this section for encoding data and limits. See Table 3-25.

**Table 3-25. DIV Action**

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Dividend</th>
<th>Divisor</th>
<th>Quotient</th>
<th>Remainder</th>
<th>Maximum Quotient</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word/byte AX</td>
<td>r/m8</td>
<td>AL</td>
<td>AH</td>
<td></td>
<td>255</td>
</tr>
<tr>
<td>Doubleword/word DX:AX</td>
<td>r/m16</td>
<td>AX</td>
<td>DX</td>
<td></td>
<td>65,535</td>
</tr>
<tr>
<td>Quadword/doubleword EDX:EAX</td>
<td>r/m32</td>
<td>EAX</td>
<td>EDX</td>
<td></td>
<td>$2^{32} - 1$</td>
</tr>
<tr>
<td>Doublequadword/quadword RDX:RAX</td>
<td>r/m64</td>
<td>RAX</td>
<td>RDX</td>
<td></td>
<td>$2^{64} - 1$</td>
</tr>
</tbody>
</table>

**Operation**

IF SRC = 0
    THEN #DE; Fl; (* Divide Error *)
IF OperandSize = 8 (* Word/Byte Operation *)
    THEN
        temp ← AX / SRC;
        IF temp > FFH
            THEN #DE; (* Divide error *)
            ELSE
                AL ← temp;
                AH ← AX MOD SRC;
        FI;
    ELSE IF OperandSize = 16 (* Doubleword/word operation *)
        THEN
            temp ← DX:AX / SRC;
            IF temp > FFFFH
                THEN #DE; (* Divide error *)
                ELSE
                    AX ← temp;
                    DX ← DX:AX MOD SRC;
            FI;
        ELSE IF OperandSize = 32 (* Quadword/doubleword operation *)
            THEN
                temp ← EDX:EAX / SRC;
IF temp > FFFFFFFFFH
    THEN #DE; (* Divide error *)
ELSE
    EAX ← temp;
    EDX ← EDX:EAX MOD SRC;
FI;
FI;
ELSE IF 64-Bit Mode and Operandsize = 64 (* Doublequadword/quadword operation *)
THEN
    temp ← RDX:RAX / SRC;
    IF temp > FFFFFFFFFFFFFFFFFH
        THEN #DE; (* Divide error *)
    ELSE
        RAX ← temp;
        RDX ← RDX:RAX MOD SRC;
    FI;
FI;

Flags Affected
The CF, OF, SF, ZF, AF, and PF flags are undefined.

Protected Mode Exceptions
#DE If the source operand (divisor) is 0
    If the quotient is too large for the designated register.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#DE If the source operand (divisor) is 0.
    If the quotient is too large for the designated register.
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#DE If the source operand (divisor) is 0.
If the quotient is too large for the designated register.

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#DE If the source operand (divisor) is 0
If the quotient is too large for the designated register.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
DIVPD—Divide Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 5E /r DIVPD xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Divide packed double-precision floating-point values in xmm1 by packed double-precision floating-point values xmm2/m128.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 5E /r VDIVPD xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Divide packed double-precision floating-point values in xmm2 by packed double-precision floating-point values in xmm3/mem.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 5E /r VDIVPD ymm1, ymm2, ymm3/m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Divide packed double-precision floating-point values in ymm2 by packed double-precision floating-point values in ymm3/mem.</td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Performs an SIMD divide of the two or four packed double-precision floating-point values in the first source operand by the two or four packed double-precision floating-point values in the second source operand. See Chapter 11 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an overview of a SIMD double-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.
INSTRUCTION SET REFERENCE, A-L

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Operation

DIVPD (128-bit Legacy SSE version)
DEST[63:0] ← SRC1[63:0] / SRC2[63:0]
DEST[VLMAX-1:128] (Unmodified)

VDIVPD (VEX.128 encoded version)
DEST[63:0] ← SRC1[63:0] / SRC2[63:0]
DEST[VLMAX-1:128] ← 0

VDIVPD (VEX.256 encoded version)
DEST[63:0] ← SRC1[63:0] / SRC2[63:0]

Intel C/C++ Compiler Intrinsic Equivalent
DIVPD: __m128d _mm_div_pd(__m128d a, __m128d b)
VDIVPD: __m256d _mm256_div_pd (__m256d a, __m256d b);

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Divide-by-Zero, Precision, Denormal.

Other Exceptions
See Exceptions Type 2.
DIVPS—Divide Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
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<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 5E /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Divide packed single-precision floating-point values in xmm1 by packed single-precision floating-point values xmm2/m128.</td>
</tr>
<tr>
<td>DIVPS xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 5E /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Divide packed single-precision floating-point values in xmm2 by packed double-precision floating-point values in xmm3/mem.</td>
</tr>
<tr>
<td>VDIVPS xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 5E /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Divide packed single-precision floating-point values in ymm2 by packed double-precision floating-point values in ymm3/mem.</td>
</tr>
<tr>
<td>VDIVPS ymm1, ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

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<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an SIMD divide of the four or eight packed single-precision floating-point values in the first source operand by the four or eight packed single-precision floating-point values in the second source operand. See Chapter 10 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an overview of a SIMD single-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**DIVPS (128-bit Legacy SSE version)**

DEST[31:0] ← SRC1[31:0] / SRC2[31:0]
DEST[95:64] ← SRC1[95:64] / SRC2[95:64]
DEST[VLMAX-1:128] (Unmodified)

**VDIVPS (VEX.128 encoded version)**

DEST[31:0] ← SRC1[31:0] / SRC2[31:0]
DEST[95:64] ← SRC1[95:64] / SRC2[95:64]
DEST[VLMAX-1:128] ← 0

**VDIVPS (VEX.256 encoded version)**

DEST[31:0] ← SRC1[31:0] / SRC2[31:0]
DEST[95:64] ← SRC1[95:64] / SRC2[95:64]

**Intel C/C++ Compiler Intrinsic Equivalent**

DIVPS: __m128 _mm_div_ps(__m128 a, __m128 b)
VDIVPS: __m256 _mm256_div_ps (__m256 a, __m256 b);

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Divide-by-Zero, Precision, Denormal.

**Other Exceptions**

See Exceptions Type 2.
DIVSD—Divide Scalar Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
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<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 5E /r DIVSD xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Divide low double-precision floating-point value in xmm1 by low double-precision floating-point value in xmm2/mem64.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F:WIG 5E /r VDIVSD xmm1, xmm2, xmm3/m64</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Divide low double-precision floating-point value in xmm2 by low double-precision floating-point value in xmm3/mem64.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
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<tr>
<th>Op/En</th>
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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Divides the low double-precision floating-point value in the first source operand by the low double-precision floating-point value in the second source operand, and stores the double-precision floating-point result in the destination operand. The second source operand can be an XMM register or a 64-bit memory location. The first source and destination hyperions are XMM registers. The high quadword of the destination operand is copied from the high quadword of the first source operand. See Chapter 11 in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for an overview of a scalar double-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Operation

**DIVSD (128-bit Legacy SSE version)**

DEST[63:0] ← DEST[63:0] / SRC[63:0]
DIVSD—Divide Scalar Double-Precision Floating-Point Values

DEST[VLMAX-1:64] (Unmodified)

VDIVSD (VEX.128 encoded version)
DEST[63:0] ← SRC1[63:0] / SRC2[63:0]
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
DIVSD: __m128d _mm_div_sd (m128d a, m128d b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Divide-by-Zero, Precision, Denormal.

Other Exceptions
See Exceptions Type 3.
DIVSS—Divide Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
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<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 5E /r DIVSS xmm1, xmm2/m32</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Divide low single-precision floating-point value in xmm1 by low single-precision floating-point value in xmm2/m32.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F:WIG 5E /r VDIVSS xmm1, xmm2, xmm3/m32</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Divide low single-precision floating point value in xmm2 by low single precision floating-point value in xmm3/m32.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>Instruction Operand Encoding</th>
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<tbody>
<tr>
<td>Op/En</td>
</tr>
<tr>
<td>RM</td>
</tr>
<tr>
<td>RVM</td>
</tr>
</tbody>
</table>

Description

Divides the low single-precision floating-point value in the first source operand by the low single-precision floating-point value in the second source operand, and stores the single-precision floating-point result in the destination operand. The second source operand can be an XMM register or a 32-bit memory location. The first source and destination operands are XMM registers. The three high-order doublewords of the destination are copied from the same dwords of the first source operand. See Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an overview of a scalar single-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Operation

DIVSS (128-bit Legacy SSE version)
DEST[31:0] ← DEST[31:0] / SRC[31:0]
DIVSS—Divide Scalar Single-Precision Floating-Point Values

DEST[VLMAX-1:32] (Unmodified)

VDIVSS (VEX.128 encoded version)
DEST[31:0] ← SRC1[31:0] / SRC2[31:0]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
DIVSS: __m128 _mm_div_ss(__m128 a, __m128 b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Divide-by-Zero, Precision, Denormal.

Other Exceptions
See Exceptions Type 3.
**DPPD — Dot Product of Packed Double Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
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<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 41 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Selectively multiply packed DP floating-point values from xmm1 with packed DP floating-point values from xmm2, add and selectively store the packed DP floating-point values to xmm1.</td>
</tr>
<tr>
<td>DPPD xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.WIG 41 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Selectively multiply packed DP floating-point values from xmm2 with packed DP floating-point values from xmm3, add and selectively store the packed DP floating-point values to xmm1.</td>
</tr>
<tr>
<td>VDPPD xmm1,xmm2, xmm3/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

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<th>Operand 4</th>
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</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

**Description**

Conditionally multiplies the packed double-precision floating-point values in the destination operand (first operand) with the packed double-precision floating-point values in the source (second operand) depending on a mask extracted from bits [5:4] of the immediate operand (third operand). If a condition mask bit is zero, the corresponding multiplication is replaced by a value of 0.0.

The two resulting double-precision values are summed into an intermediate result. The intermediate result is conditionally broadcasted to the destination using a broadcast mask specified by bits [1:0] of the immediate byte.

If a broadcast mask bit is "1", the intermediate result is copied to the corresponding qword element in the destination operand. If a broadcast mask bit is zero, the corresponding element in the destination is set to zero.

DPPS follows the NaN forwarding rules stated in the Software Developer’s Manual, vol. 1, table 4.7. These rules do not cover horizontal prioritization of NaNs. Horizontal propagation of NaNs to the destination and the positioning of those NaNs in the desti-
nation is implementation dependent. NaNs on the input sources or computationally
generated NaNs will have at least one NaN propagated to the destination.

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit
memory location. The destination is not distinct from the first source XMM register
and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are
unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit
memory location. The destination operand is an XMM register. The upper bits
(VLMAX-1:128) of the corresponding YMM register destination are zeroed.

If VDPPD is encoded with VEX.L=1, an attempt to execute the instruction encoded
with VEX.L=1 will cause an #UD exception.

Operation

DP_primitive (SRC1, SRC2)
IF (imm8[4] = 1)
  THEN Temp1[63:0] ← DEST[63:0] * SRC[63:0];
  ELSE Temp1[63:0] ← +0.0; Fl;
IF (imm8[5] = 1)
  THEN Temp1[127:64] ← DEST[127:64] * SRC[127:64];
  ELSE Temp1[127:64] ← +0.0; Fl;

Temp2[63:0] ← Temp1[63:0] + Temp1[127:64];

IF (imm8[0] = 1)
  THEN DEST[63:0] ← Temp2[63:0];
  ELSE DEST[63:0] ← +0.0; Fl;
IF (imm8[1] = 1)
  THEN DEST[127:64] ← Temp2[63:0];
  ELSE DEST[127:64] ← +0.0; Fl;

DPPD (128-bit Legacy SSE version)
DEST[127:0] ← DP_Primitive(SRC1[127:0], SRC2[127:0]);
DEST[VLMAX-1:128] (Unmodified)

VDPPD (VEX.128 encoded version)
DEST[127:0] ← DP_Primitive(SRC1[127:0], SRC2[127:0]);
DEST[VLMAX-1:128] ← 0

Flags Affected
None
Intel C/C++ Compiler Intrinsic Equivalent

DPPD: __m128d _mm_dp_pd ( __m128d a, __m128d b, const int mask);

SIMD Floating-Point Exceptions

Overflow, Underflow, Invalid, Precision, Denormal
Exceptions are determined separately for each add and multiply operation.
Unmasked exceptions will leave the destination untouched.

Other Exceptions

See Exceptions Type 2; additionally

#UD If VEX.L = 1.
DPPS — Dot Product of Packed Single Precision Floating-Point Values

<table>
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<tbody>
<tr>
<td>66 0F 3A 40 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Selectively multiply packed SP floating-point values from <code>xmm1</code> with packed SP floating-point values from <code>xmm2</code>, add and selectively store the packed SP floating-point values or zero values to <code>xmm1</code>.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.WIG 40 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply packed SP floating point values from <code>xmm1</code> with packed SP floating point values from <code>xmm2/mem</code> selectively add and store to <code>xmm1</code>.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F3A.WIG 40 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply packed single-precision floating-point values from <code>ymm2</code> with packed SP floating point values from <code>ymm3/mem</code>, selectively add pairs of elements and store to <code>ymm1</code>.</td>
</tr>
</tbody>
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<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Conditionally multiplies the packed single precision floating-point values in the destination operand (first operand) with the packed single-precision floats in the source (second operand) depending on a mask extracted from the high 4 bits of the immediate byte (third operand). If a condition mask bit in Imm8[7:4] is zero, the corresponding multiplication is replaced by a value of 0.0.

The four resulting single-precision values are summed into an intermediate result. The intermediate result is conditionally broadcasted to the destination using a broadcast mask specified by bits [3:0] of the immediate byte.
If a broadcast mask bit is "1", the intermediate result is copied to the corresponding dword element in the destination operand. If a broadcast mask bit is zero, the corresponding element in the destination is set to zero.

DPPS follows the NaN forwarding rules stated in the Software Developer’s Manual, vol. 1, table 4.7. These rules do not cover horizontal prioritization of NaNs. Horizontal propagation of NaNs to the destination and the positioning of those NaNs in the destination is implementation dependent. NaNs on the input sources or computationally generated NaNs will have at least one NaN propagated to the destination.

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Operation

\textbf{DP\_primitive (SRC1, SRC2)}

\textbf{IF (imm8[4] = 1)}
\hspace{1em}THEN Temp1[31:0] \leftarrow \text{DEST}[31:0] \times \text{SRC}[31:0];
\hspace{1em}ELSE Temp1[31:0] \leftarrow +0.0; \text{Ft};
\textbf{FI;}

\textbf{IF (imm8[5] = 1)}
\hspace{1em}THEN Temp1[63:32] \leftarrow \text{DEST}[63:32] \times \text{SRC}[63:32];
\hspace{1em}ELSE Temp1[63:32] \leftarrow +0.0; \text{Ft};
\textbf{FI;}

\textbf{IF (imm8[6] = 1)}
\hspace{1em}THEN Temp1[95:64] \leftarrow \text{DEST}[95:64] \times \text{SRC}[95:64];
\hspace{1em}ELSE Temp1[95:64] \leftarrow +0.0; \text{Ft};
\textbf{FI;}

\textbf{IF (imm8[7] = 1)}
\hspace{1em}THEN Temp1[127:96] \leftarrow \text{DEST}[127:96] \times \text{SRC}[127:96];
\hspace{1em}ELSE Temp1[127:96] \leftarrow +0.0; \text{Ft};
\textbf{FI;}

Temp2[31:0] \leftarrow \text{Temp1}[31:0] + \text{Temp1}[63:32];
Temp3[31:0] \leftarrow \text{Temp1}[95:64] + \text{Temp1}[127:96];
Temp4[31:0] \leftarrow \text{Temp2}[31:0] + \text{Temp3}[31:0];

\textbf{IF (imm8[0] = 1)}
\hspace{1em}THEN DEST[31:0] \leftarrow \text{Temp4}[31:0];
\hspace{1em}ELSE DEST[31:0] \leftarrow +0.0; \text{Ft};
\textbf{FI;}

\textbf{IF (imm8[1] = 1)}
THEN DEST[63:32] ← Temp4[31:0];
ELSE DEST[63:32] ← +0.0; Fl;
IF (imm8[2] = 1)
    THEN DEST[95:64] ← Temp4[31:0];
    ELSE DEST[95:64] ← +0.0; Fl;
IF (imm8[3] = 1)
    THEN DEST[127:96] ← Temp4[31:0];
    ELSE DEST[127:96] ← +0.0; Fl;

DPPS (128-bit Legacy SSE version)
DEST[127:0]←DP_Primitive(SRC1[127:0], SRC2[127:0]);
DEST[VLMAX-1:128] (Unmodified)

VDPPS (VEX.128 encoded version)
DEST[127:0]←DP_Primitive(SRC1[127:0], SRC2[127:0]);
DEST[VLMAX-1:128] ← 0

VDPPS (VEX.256 encoded version)
DEST[127:0]←DP_Primitive(SRC1[127:0], SRC2[127:0]);

Intel C/C++ Compiler Intrinsic Equivalent
(V)DPPS: __m128 _mm_dp_ps (__m128 a, __m128 b, const int mask);
VDPPS: __m256 _mm256_dp_ps ( __m256 a, __m256 b, const int mask);

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal
Exceptions are determined separately for each add and multiply operation, in the order of their execution. Unmasked exceptions will leave the destination operands unchanged.

Other Exceptions
See Exceptions Type 2.
EMMS—Empty MMX Technology State

**Opcode Instruction Op/ En 64-Bit Mode Compat/ Leg Mode Description**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 77</td>
<td>EMMS</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Set the x87 FPU tag word to empty.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Sets the values of all the tags in the x87 FPU tag word to empty (all 1s). This operation marks the x87 FPU data registers (which are aliased to the MMX technology registers) as available for use by x87 FPU floating-point instructions. (See Figure 8-7 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for the format of the x87 FPU tag word.) All other MMX instructions (other than the EMMS instruction) set all the tags in x87 FPU tag word to valid (all 0s).

The EMMS instruction must be used to clear the MMX technology state at the end of all MMX technology procedures or subroutines and before calling other procedures or subroutines that may execute x87 floating-point instructions. If a floating-point instruction loads one of the registers in the x87 FPU data register stack before the x87 FPU tag word has been reset by the EMMS instruction, an x87 floating-point register stack overflow can occur that will result in an x87 floating-point exception or incorrect result.

EMMS operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

x87FPUTagWord ← FFFFH;

**Intel C/C++ Compiler Intrinsic Equivalent**

void _mm_empty()

**Flags Affected**

None.

**Protected Mode Exceptions**

#UD If CR0.EM[bit 2] = 1.

#NM If CR0.TS[bit 3] = 1.
#MF If there is a pending FPU exception.
#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**
Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**
Same exceptions as in protected mode.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
Same exceptions as in protected mode.
ENTER—Make Stack Frame for Procedure Parameters

Description

Creates a stack frame for a procedure. The first operand (size operand) specifies the size of the stack frame (that is, the number of bytes of dynamic storage allocated on the stack for the procedure). The second operand (nesting level operand) gives the lexical nesting level (0 to 31) of the procedure. The nesting level determines the number of stack frame pointers that are copied into the “display area” of the new stack frame from the preceding frame. Both of these operands are immediate values.

The stack-size attribute determines whether the BP (16 bits), EBP (32 bits), or RBP (64 bits) register specifies the current frame pointer and whether SP (16 bits), ESP (32 bits), or RSP (64 bits) specifies the stack pointer. In 64-bit mode, stack-size attribute is always 64-bits.

The ENTER and companion LEAVE instructions are provided to support block structured languages. The ENTER instruction (when used) is typically the first instruction in a procedure and is used to set up a new stack frame for a procedure. The LEAVE instruction is then used at the end of the procedure (just before the RET instruction) to release the stack frame.

If the nesting level is 0, the processor pushes the frame pointer from the BP/EBP/RBP register onto the stack, copies the current stack pointer from the SP/ESP/RSP register into the BP/EBP/RBP register, and loads the SP/ESP/RSP register with the current stack-pointer value minus the value in the size operand. For nesting levels of 1 or greater, the processor pushes additional frame pointers on the stack before adjusting the stack pointer. These additional frame pointers provide the called procedure with access points to other nested frames on the stack. See “Procedure Calls for Block-Structured Languages” in Chapter 6 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information about the actions of the ENTER instruction.
The ENTER instruction causes a page fault whenever a write using the final value of
the stack pointer (within the current stack segment) would do so.
In 64-bit mode, default operation size is 64 bits; 32-bit operation size cannot be
encoded.

**Operation**

NestingLevel ← NestingLevel MOD 32
IF 64-Bit Mode (StackSize = 64)
    THEN
        Push(RBP);
        FrameTemp ← RSP;
    ELSE IF StackSize = 32
        THEN
            Push(EBP);
            FrameTemp ← ESP;
    FI;
    ELSE (* StackSize = 16 *)
        Push(BP);
        FrameTemp ← SP;
    FI;
    IF NestingLevel = 0
        THEN GOTO CONTINUE;
    FI;
    IF (NestingLevel > 1)
        THEN FOR i ← 1 to (NestingLevel - 1)
            DO
                IF 64-Bit Mode (StackSize = 64)
                    THEN
                        RBP ← RBP - 8;
                        Push([RBP]); (* Quadword push *)
                    ELSE IF OperandSize = 32
                        THEN
                            IF StackSize = 32
                                EBP ← EBP - 4;
                                Push([EBP]); (* Doubleword push *)
                            ELSE (* StackSize = 16 *)
                                BP ← BP - 4;
                                Push([BP]); (* Doubleword push *)
                            FI;
                            FI;
                            ELSE (* OperandSize = 16 *)
                                IF StackSize = 32
                                    THEN
                                        Push([BP]); (* Doubleword push *)
                                    ELSE (* StackSize = 16 *)
                                        FrameTemp ← SP;
                                        Push([FrameTemp]); (* Doubleword push *)
                                    FI;
                                FI;
                ELSE (* OperandSize = 16 *)
                    IF StackSize = 32
                        THEN
                            Push([BP]); (* Doubleword push *)
                        ELSE (* StackSize = 16 *)
                            FrameTemp ← SP;
                            Push([FrameTemp]); (* Doubleword push *)
                        FI;
                    FI;
            FI;
        FI;
    FI;
ENTER—Make Stack Frame for Procedure Parameters

\begin{verbatim}
EBP ← EBP - 2;
PUSH([EBP]); (* Word push *)
ELSE (* StackSize = 16 *)
BP ← BP - 2;
PUSH([BP]); (* Word push *)
FI;
FI;
OD;
FI;
IF 64-Bit Mode (StackSize = 64)
THEN
  PUSH(FrameTemp); (* Quadword push *)
ELSE IF OperandSize = 32
  THEN
    PUSH(FrameTemp); FI; (* Doubleword push *)
ELSE (* OperandSize = 16 *)
  PUSH(FrameTemp); (* Word push *)
FI;
CONTINUE:
IF 64-Bit Mode (StackSize = 64)
THEN
  RBP ← FrameTemp;
  RSP ← RSP – Size;
ELSE IF StackSize = 32
  THEN
    EBP ← FrameTemp;
    ESP ← ESP – Size; FI;
ELSE (* StackSize = 16 *)
  BP ← FrameTemp;
  SP ← SP – Size;
FI;
END;

Flags Affected
None.

Protected Mode Exceptions

#SS(0) If the new value of the SP or ESP register is outside the stack segment limit.
\end{verbatim}
#PF(fault-code) If a page fault occurs or if a write using the final value of the stack pointer (within the current stack segment) would cause a page fault.

#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#SS If the new value of the SP or ESP register is outside the stack segment limit.

#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#SS(0) If the new value of the SP or ESP register is outside the stack segment limit.

#PF(fault-code) If a page fault occurs or if a write using the final value of the stack pointer (within the current stack segment) would cause a page fault.

#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If the stack address is in a non-canonical form.

#PF(fault-code) If a page fault occurs or if a write using the final value of the stack pointer (within the current stack segment) would cause a page fault.

#UD If the LOCK prefix is used.
EXTRACTPS — Extract Packed Single Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 17 /r ib</td>
<td>MRI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Extract a single-precision floating-point value from xmm2 at the source offset specified by imm8 and store the result to reg or m32. The upper 32 bits of r64 is zeroed if reg is r64.</td>
</tr>
<tr>
<td>EXTRACTPS reg/m32, xmm2, imm8</td>
<td>MRI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F3A.WIG 17 /r ib</td>
<td>MRI</td>
<td>V/V</td>
<td>AVX</td>
<td>Extract one single-precision floating-point value from xmm1 at the offset specified by imm8 and store the result in reg or m32. Zero extend the results in 64-bit register if applicable.</td>
</tr>
<tr>
<td>VEXTRACTPS r/m32, xmm1, imm8</td>
<td>MRI</td>
<td>V/V</td>
<td>AVX</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MRI</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Extracts a single-precision floating-point value from the source operand (second operand) at the 32-bit offset specified from imm8. Immediate bits higher than the most significant offset for the vector length are ignored.

The extracted single-precision floating-point value is stored in the low 32-bits of the destination operand.

In 64-bit mode, destination register operand has default operand size of 64 bits. The upper 32-bits of the register are filled with zero. REX.W is ignored.

128-bit Legacy SSE version: When a REX.W prefix is used in 64-bit mode with a general purpose register (GPR) as a destination operand, the packed single quantity is zero extended to 64 bits.

VEX.128 encoded version: When VEX.128.66.0F3A.W1 17 form is used in 64-bit mode with a general purpose register (GPR) as a destination operand, the packed single quantity is zero extended to 64 bits. VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

The source register is an XMM register. Imm8[1:0] determine the starting DWORD offset from which to extract the 32-bit floating-point value.
INSTRUCTION SET REFERENCE, A-L

If VEXTRACTPS is encoded with VEX.L = 1, an attempt to execute the instruction encoded with VEX.L = 1 will cause an #UD exception.

Operation

VEXTRACTPS (128-bit Legacy SSE version)

\[
\text{SRC OFFSET} \leftarrow \text{IMM8}[1:0]
\]

\[
\text{IF (64-Bit Mode and DEST is register)}
\]

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow (\text{SRC}[127:0] \gg (\text{SRC_OFFSET} \times 32)) \text{ AND } 0xFFFFFFFFh \\
\text{DEST}[63:32] & \leftarrow 0
\end{align*}
\]

\[
\text{ELSE}
\]

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow (\text{SRC}[127:0] \gg (\text{SRC_OFFSET} \times 32)) \text{ AND } 0xFFFFFFFFh \\
\text{DEST}[63:32] & \leftarrow 0
\end{align*}
\]

\[
\text{FI}
\]

VEXTRACTPS (VEX.128 encoded version)

\[
\text{SRC OFFSET} \leftarrow \text{IMM8}[1:0]
\]

\[
\text{IF (64-Bit Mode and DEST is register)}
\]

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow (\text{SRC}[127:0] \gg (\text{SRC_OFFSET} \times 32)) \text{ AND } 0xFFFFFFFFh \\
\text{DEST}[63:32] & \leftarrow 0
\end{align*}
\]

\[
\text{ELSE}
\]

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow (\text{SRC}[127:0] \gg (\text{SRC_OFFSET} \times 32)) \text{ AND } 0xFFFFFFFFh \\
\text{DEST}[63:32] & \leftarrow 0
\end{align*}
\]

\[
\text{FI}
\]

Intel C/C++ Compiler Intrinsic Equivalent

\begin{align*}
\text{EXTRACTPS:} & \quad \text{__m128 \_mm\_extract\_ps (__m128 a, const int nidx);} \\
\text{EXTRACTPS:} & \quad \text{__m128 \_mm\_extract\_ps (__m128 a, const int nidx)};
\end{align*}

SIMD Floating-Point Exceptions

None

Other Exceptions

See Exceptions Type 5; additionally

#UD \quad \text{If VEX.L = 1.}
F2XM1—Compute $2^x - 1$

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Comp/F Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F0</td>
<td>F2XM1</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(0) with $(2^{ST(0)} - 1)$.</td>
</tr>
</tbody>
</table>

Description

Computes the exponential value of 2 to the power of the source operand minus 1. The source operand is located in register ST(0) and the result is also stored in ST(0). The value of the source operand must lie in the range $-1.0$ to $+1.0$. If the source value is outside this range, the result is undefined.

The following table shows the results obtained when computing the exponential value of various classes of numbers, assuming that neither overflow nor underflow occurs.

<table>
<thead>
<tr>
<th>Table 3-26. Results Obtained from F2XM1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ST(0) SRC</strong></td>
</tr>
<tr>
<td>----------------</td>
</tr>
<tr>
<td>$-1.0$ to $-0$</td>
</tr>
<tr>
<td>$-0$</td>
</tr>
<tr>
<td>$+0$</td>
</tr>
<tr>
<td>$+0$ to $+1.0$</td>
</tr>
</tbody>
</table>

Values other than 2 can be exponentiated using the following formula:

$$x^y \leftarrow 2^{(y + \log_2 x)}$$

This instruction's operation is the same in non-64-bit modes and 64-bit mode.

Operation

$$ST(0) \leftarrow (2^{ST(0)} - 1);$$

FPU Flags Affected

C1  Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.

C0, C2, C3 Undefined.

Floating-Point Exceptions

#IS Stack underflow occurred.
#IA Source operand is an SNaN value or unsupported format.
#D Source is a denormal value.
INSTRUCTION SET REFERENCE, A-L

#U Result is too small for destination format.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FABS—Absolute Value

Description
Clears the sign bit of ST(0) to create the absolute value of the operand. The following table shows the results obtained when creating the absolute value of various classes of numbers.

<table>
<thead>
<tr>
<th>Table 3-27. Results Obtained from FABS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) SRC</td>
</tr>
<tr>
<td>− ∞</td>
</tr>
<tr>
<td>− F</td>
</tr>
<tr>
<td>− 0</td>
</tr>
<tr>
<td>+ 0</td>
</tr>
<tr>
<td>+ F</td>
</tr>
<tr>
<td>+ ∞</td>
</tr>
<tr>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
ST(0) ← |ST(0)|;

FPU Flags Affected
C1 Set to 0.
C0, C2, C3 Undefined.

Floating-Point Exceptions
#IS Stack underflow occurred.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, A-L

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FADD/FADDP/FIADD—Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /0</td>
<td>FADD m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Add m32fp to ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC /0</td>
<td>FADD m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Add m64fp to ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>D8 C0+i</td>
<td>FADD ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Add ST(0) to ST(i) and store result in ST(0).</td>
</tr>
<tr>
<td>DC C0+i</td>
<td>FADD ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Add ST(i) to ST(0) and store result in ST(i).</td>
</tr>
<tr>
<td>DE C0+i</td>
<td>FADDP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Add ST(i) to ST(0), store result in ST(i), and pop the register stack.</td>
</tr>
<tr>
<td>DE C1</td>
<td>FADDP</td>
<td>Valid</td>
<td>Valid</td>
<td>Add ST(0) to ST(1), store result in ST(1), and pop the register stack.</td>
</tr>
<tr>
<td>DA /0</td>
<td>FIADD m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Add m32int to ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DE /0</td>
<td>FIADD m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Add m16int to ST(0) and store result in ST(0).</td>
</tr>
</tbody>
</table>

Description

Adds the destination and source operands and stores the sum in the destination location. The destination operand is always an FPU register; the source operand can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format or in word or doubleword integer format.

The no-operand version of the instruction adds the contents of the ST(0) register to the ST(1) register. The one-operand version adds the contents of a memory location (either a floating-point or an integer value) to the contents of the ST(0) register. The two-operand version, adds the contents of the ST(0) register to the ST(i) register or vice versa. The value in ST(0) can be doubled by coding:

FADD ST(0), ST(0);

The FADDP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. (The no-operand version of the floating-point add instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FADD rather than FADDP.)

The FIADD instructions convert an integer source operand to double extended-precision floating-point format before performing the addition.
The table on the following page shows the results obtained when adding various classes of numbers, assuming that neither overflow nor underflow occurs.

When the sum of two operands with opposite signs is 0, the result is +0, except for the round toward $-\infty$ mode, in which case the result is $-0$. When the source operand is an integer 0, it is treated as a +0.

When both operands are infinities of the same sign, the result is $\infty$ of the expected sign. If both operands are infinities of opposite signs, an invalid-operation exception is generated. See Table 3-28.

### Table 3-28. FADD/FADDP/FIADD Results

<table>
<thead>
<tr>
<th>SRC</th>
<th>$-\infty$</th>
<th>$-F$</th>
<th>$-0$</th>
<th>$+0$</th>
<th>$+F$</th>
<th>$+\infty$</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>NaN</td>
<td>NaN</td>
</tr>
<tr>
<td>$-F$ or $-I$</td>
<td>$-F$</td>
<td>SRC</td>
<td>$\pm F$ or $\pm 0$</td>
<td>$+\infty$</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
<tr>
<td>$-0$</td>
<td>$-\infty$</td>
<td>DEST</td>
<td>$\pm 0$</td>
<td>DEST</td>
<td>$+\infty$</td>
<td>NaN</td>
<td>NaN</td>
</tr>
<tr>
<td>$+0$</td>
<td>$-\infty$</td>
<td>DEST</td>
<td>$\pm 0$</td>
<td>DEST</td>
<td>$+\infty$</td>
<td>NaN</td>
<td>NaN</td>
</tr>
<tr>
<td>$+F$ or $+I$</td>
<td>$-\infty$</td>
<td>$\pm F$ or $\pm 0$</td>
<td>SRC</td>
<td>SRC</td>
<td>$+F$</td>
<td>$+\infty$</td>
<td>NaN</td>
</tr>
<tr>
<td>$+\infty$</td>
<td>*</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>NaN</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

- F Means finite floating-point value.
- I Means integer.
- * Indicates floating-point invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

### Operation

IF Instruction = FIADD

THEN

    DEST ← DEST + ConvertToDoubleExtendedPrecisionFP(SRC);
ELSE (* Source operand is floating-point value *)
    DEST ← DEST + SRC;
FI;

IF Instruction = FADDP

THEN

    PopRegisterStack;
FI;

3-330 Vol. 2A FADD/FADDP/FIADD—Add
FPU Flags Affected
C1 Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
C0, C2, C3 Undefined.

Floating-Point Exceptions
#IS Stack underflow occurred.
#IA Operand is an SNaN value or unsupported format.
    Operands are infinities of unlike sign.
#D Source operand is a denormal value.
#U Result is too small for destination format.
#O Result is too large for destination format.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS,
    ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment
    selector.
#SS(0) If a memory operand effective address is outside the SS
    segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory
    reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS,
    ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS
    segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS,
    ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS
    segment limit.
INSTRUCTION SET REFERENCE, A-L

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
**FBLD—Load Binary Coded Decimal**

**Description**
Converts the BCD source operand into double extended-precision floating-point format and pushes the value onto the FPU stack. The source operand is loaded without rounding errors. The sign of the source operand is preserved, including that of -0.

The packed BCD digits are assumed to be in the range 0 through 9; the instruction does not check for invalid digits (AH through FH). Attempting to load an invalid encoding produces an undefined result.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**
TOP ← TOP – 1;
ST(0) ← ConvertToDoubleExtendedPrecisionFP(SRC);

**FPU Flags Affected**
C1 Set to 1 if stack overflow occurred; otherwise, set to 0.
C0, C2, C3 Undefined.

**Floating-Point Exceptions**
#IS Stack overflow occurred.

**Protected Mode Exceptions**
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FBSTP—Store BCD Integer and Pop

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /6</td>
<td>FBSTP m80bcd</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m80bcd and pop ST(0).</td>
</tr>
</tbody>
</table>

Description

Converts the value in the ST(0) register to an 18-digit packed BCD integer, stores the result in the destination operand, and pops the register stack. If the source value is a non-integral value, it is rounded to an integer value, according to rounding mode specified by the RC field of the FPU control word. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

The destination operand specifies the address where the first byte destination value is to be stored. The BCD value (including its sign bit) requires 10 bytes of space in memory.

The following table shows the results obtained when storing various classes of numbers in packed BCD format.

Table 3-29. FBSTP Results

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>− ∞ or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>F ≤ −1</td>
<td>− D</td>
</tr>
<tr>
<td>−1 &lt; F &lt; 0</td>
<td>**</td>
</tr>
<tr>
<td>0</td>
<td>− 0</td>
</tr>
<tr>
<td>+ 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ 0 &lt; F &lt; 1</td>
<td>**</td>
</tr>
<tr>
<td>F ≥ 1</td>
<td>+ D</td>
</tr>
<tr>
<td>+ ∞ or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>*</td>
</tr>
</tbody>
</table>

NOTES:

F Means finite floating-point value.
D Means packed-BCD number.
* Indicates floating-point invalid-operation (#IA) exception.
** ±0 or ±1, depending on the rounding mode.

If the converted value is too large for the destination format, or if the source operand is an −∞, SNaN, QNaN, or is in an unsupported format, an invalid-arithmetic-operand condition is signaled. If the invalid-operation exception is not masked, an invalid-arithmetic-operand exception (#IA) is generated and no value is stored in the desti-
nation operand. If the invalid-operation exception is masked, the packed BCD indefinite value is stored in memory.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{DEST} \leftarrow \text{BCD(ST(0))}; \\
\text{PopRegisterStack};
\]

**FPU Flags Affected**

- **C1**: Set to 0 if stack underflow occurred.
- **C0**, **C2**, **C3**: Undefined.

**Floating-Point Exceptions**

- **#IS**: Stack underflow occurred.
- **#IA**: Converted value that exceeds 18 BCD digits in length. Source operand is an SNaN, QNaN, ±\(\infty\), or in an unsupported format.
- **#P**: Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **#GP(0)**: If a segment register is being loaded with a segment selector that points to a non-writable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS**: If a memory operand effective address is outside the SS segment limit.
FBSTP—Store BCD Integer and Pop

#NM \( \text{CR0.EM}[\text{bit 2}] \) or \( \text{CR0.TS}[\text{bit 3}] = 1 \).
#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM \( \text{CR0.EM}[\text{bit 2}] \) or \( \text{CR0.TS}[\text{bit 3}] = 1 \).
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM \( \text{CR0.EM}[\text{bit 2}] \) or \( \text{CR0.TS}[\text{bit 3}] = 1 \).
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FCHS—Change Sign

Description
Complements the sign bit of ST(0). This operation changes a positive value into a negative value of equal magnitude or vice versa. The following table shows the results obtained when changing the sign of various classes of numbers.

Table 3-30. FCHS Results

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>+∞</td>
</tr>
<tr>
<td>−F</td>
<td>+F</td>
</tr>
<tr>
<td>−0</td>
<td>+0</td>
</tr>
<tr>
<td>+0</td>
<td>−0</td>
</tr>
<tr>
<td>+F</td>
<td>−F</td>
</tr>
<tr>
<td>+∞</td>
<td>−∞</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
* F means finite floating-point value.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
SignBit(ST(0)) ← NOT (SignBit(ST(0)));

FPU Flags Affected
C1 Set to 0.
C0, C2, C3 Undefined.

Floating-Point Exceptions
#IS Stack underflow occurred.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.
Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**FCLEX/FNCLEX—Clear Exceptions**

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DB E2</td>
<td>FCLEX</td>
<td>Valid</td>
<td>Valid</td>
<td>Clear floating-point exception flags after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DB E2</td>
<td>FNCLEX*</td>
<td>Valid</td>
<td>Valid</td>
<td>Clear floating-point exception flags without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.

**Description**
Cleans the floating-point exception flags (PE, UE, OE, ZE, DE, and IE), the exception summary status flag (ES), the stack fault flag (SF), and the busy flag (B) in the FPU status word. The FCLEX instruction checks for and handles any pending unmasked floating-point exceptions before clearing the exception flags; the FNCLEX instruction does not.

The assembler issues two instructions for the FCLEX instruction (an FWAIT instruction followed by an FNCLEX instruction), and the processor executes each of these instructions separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

**IA-32 Architecture Compatibility**
When operating a Pentium or Intel486 processor in MS-DOS* compatibility mode, it is possible (under unusual circumstances) for an FNCLEX instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled “No-Wait FPU Instructions Can Get FPU Interrupt in Window” in Appendix D of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a description of these circumstances. An FNCLEX instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

This instruction affects only the x87 FPU floating-point exception flags. It does not affect the SIMD floating-point exception flags in the MXCRS register.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{FPUStatusWord}[0:7] \leftarrow 0; \\
\text{FPUStatusWord}[15] \leftarrow 0;
\]
FPU Flags Affected
The PE, UE, OE, ZE, DE, IE, ES, SF, and B flags in the FPU status word are cleared. The C0, C1, C2, and C3 flags are undefined.

Floating-Point Exceptions
None.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FCMOVcc—Floating-Point Conditional Move

**Description**
Tests the status flags in the EFLAGS register and moves the source operand (second operand) to the destination operand (first operand) if the given test condition is true. The condition for each mnemonic is given in the Description column above and in Chapter 8 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*. The source operand is always in the ST(i) register and the destination operand is always ST(0).

The FCMOVcc instructions are useful for optimizing small IF constructions. They also help eliminate branching overhead for IF operations and the possibility of branch mispredictions by the processor.

A processor may not support the FCMOVcc instructions. Software can check if the FCMOVcc instructions are supported by checking the processor's feature information with the CPUID instruction (see "COMISS—Compare Scalar Ordered Single-Precision Floating-Point Values and Set EFLAGS" in this chapter). If both the CMOV and FPU feature bits are set, the FCMOVcc instructions are supported.

This instruction's operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**
The FCMOVcc instructions were introduced to the IA-32 Architecture in the P6 family processors and are not available in earlier IA-32 processors.

---

**Opcode** | **Instruction** | **64-Bit Mode** | **Compat/ Leg Mode** | **Description**
--- | --- | --- | --- | ---
DA C0+i | FCMOVB ST(0), ST(i) | Valid | Valid | Move if below (CF=1).
DA C8+i | FCMOVE ST(0), ST(i) | Valid | Valid | Move if equal (ZF=1).
DA D0+i | FCMOVBE ST(0), ST(i) | Valid | Valid | Move if below or equal (CF=1 or ZF=1).
DA DB+i | FCMOVU ST(0), ST(i) | Valid | Valid | Move if unordered (PF=1).
DB C0+i | FCMOVNB ST(0), ST(i) | Valid | Valid | Move if not below (CF=0).
DB C8+i | FCMOVNE ST(0), ST(i) | Valid | Valid | Move if not equal (ZF=0).
DB D0+i | FCMOVNBE ST(0), ST(i) | Valid | Valid | Move if not below or equal (CF=0 and ZF=0).
DB DB+i | FCMOVNU ST(0), ST(i) | Valid | Valid | Move if not unordered (PF=0).

**NOTES:**
* See IA-32 Architecture Compatibility section below.
Operation

IF condition TRUE
    THEN ST(0) ← ST(i);
FI;

FPU Flags Affected
C1                  Set to 0 if stack underflow occurred.
C0, C2, C3          Undefined.

Floating-Point Exceptions
#IS                  Stack underflow occurred.

Integer Flags Affected
None.

Protected Mode Exceptions
#NM                  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD                  If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-L

FCOM/FCOMP/FCOMPP—Compare Floating Point Values

Description

Compares the contents of register ST(0) and source value and sets condition code flags C0, C2, and C3 in the FPU status word according to the results (see the table below). The source operand can be a data register or a memory location. If no source operand is given, the value in ST(0) is compared with the value in ST(1). The sign of zero is ignored, so that –0.0 is equal to +0.0.

This instruction checks the class of the numbers being compared (see "FXAM—Examine ModR/M" in this chapter). If either operand is a NaN or is in an unsupported format, an invalid-arithmetic-operand exception (#IA) is raised and, if the exception is masked, the condition flags are set to “unordered.” If the invalid-arithmetic-operand exception is unmasked, the condition code flags are not set.

Table 3-31. FCOM/FCOMP/FCOMPP Results

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; SRC</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; SRC</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = SRC</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered*</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTES:

* Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.

Opcode Instruction 64-Bit Mode Compat/ Leg Mode Description

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /2</td>
<td>FCOM m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with m32fp.</td>
</tr>
<tr>
<td>DC /2</td>
<td>FCOM m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with m64fp.</td>
</tr>
<tr>
<td>D8 D0+i</td>
<td>FCOM ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(i).</td>
</tr>
<tr>
<td>D8 D1</td>
<td>FCOM</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(1).</td>
</tr>
<tr>
<td>D8 /3</td>
<td>FCOMP m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with m32fp and pop register stack.</td>
</tr>
<tr>
<td>DC /3</td>
<td>FCOMP m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with m64fp and pop register stack.</td>
</tr>
<tr>
<td>D8 D8+i</td>
<td>FCOMP ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(i) and pop register stack.</td>
</tr>
<tr>
<td>D8 D9</td>
<td>FCOMP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(1) and pop register stack.</td>
</tr>
<tr>
<td>DE D9</td>
<td>FCOMPP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare ST(0) with ST(1) and pop register stack twice.</td>
</tr>
</tbody>
</table>
The FCOMP instruction pops the register stack following the comparison operation and the FCOMPP instruction pops the register stack twice following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

The FCOM instructions perform the same operation as the FUCOM instructions. The only difference is how they handle QNaN operands. The FCOM instructions raise an invalid-arithmetic-operand exception (#IA) when either or both of the operands is a NaN value or is in an unsupported format. The FUCOM instructions perform the same operation as the FCOM instructions, except that they do not generate an invalid-arithmetic-operand exception for QNaNs.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

CASE (relation of operands) OF

$$\begin{align*}
\text{ST > SRC}: & \quad C3, C2, C0 \leftarrow 000; \\
\text{ST < SRC}: & \quad C3, C2, C0 \leftarrow 001; \\
\text{ST = SRC}: & \quad C3, C2, C0 \leftarrow 100; \\
\text{ESAC};
\end{align*}$$

IF ST(0) or SRC = NaN or unsupported format

THEN

#IA

IF FPUControlWord.IM = 1

THEN

$$\begin{align*}
C3, C2, C0 & \leftarrow 111; \\
\text{FI};
\end{align*}$$

FI;

IF Instruction = FCOMP

THEN

PopRegisterStack;

FI;

IF Instruction = FCOMPP

THEN

PopRegisterStack;

PopRegisterStack;

FI;

**FPU Flags Affected**

C1 \hspace{1cm} Set to 0.

C0, C2, C3 \hspace{1cm} See table on previous page.
Floating-Point Exceptions

#IS Stack underflow occurred.
#IA One or both operands are NaN values or have unsupported formats.
#D One or both operands are denormal values.

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

- **#SS(0)**: If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)**: If the memory address is in a non-canonical form.
- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#MF**: If there is a pending x87 FPU exception.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used.
FCOMI/FCOMIP/FUCOMI/FUCOMIP—Compare Floating Point Values and Set EFLAGS

Description
Performs an unordered comparison of the contents of registers ST(0) and ST(i) and sets the status flags ZF, PF, and CF in the EFLAGS register according to the results (see the table below). The sign of zero is ignored for comparisons, so that –0.0 is equal to +0.0.

Table 3-32. FCOMI/FCOMIP/ FUCOMI/FUCOMIP Results

<table>
<thead>
<tr>
<th>Comparison Results*</th>
<th>ZF</th>
<th>PF</th>
<th>CF</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST0 &gt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST0 &lt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST0 = ST(i)</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered**</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTES:
* See the IA-32 Architecture Compatibility section below.
** Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.

An unordered comparison checks the class of the numbers being compared (see “FXAM—Examine ModR/M” in this chapter). The FUCOMI/FUCOMIP instructions perform the same operations as the FCOMI/FCOMIP instructions. The only difference is that the FUCOMI/FUCOMIP instructions raise the invalid-arithmetic-operand exception (#IA) only when either or both operands are an SNaN or are in an unsupported format; QNaNs cause the condition code flags to be set to unordered, but do not cause an exception to be generated. The FCOMI/FCOMIP instructions raise an invalid-operation exception when either or both of the operands are a NaN value of any kind or are in an unsupported format.
If the operation results in an invalid-arithmetic-operand exception being raised, the status flags in the EFLAGS register are set only if the exception is masked.

The FCOMI/FCOMIP and FUCOMI/FUCOMIP instructions set the OF, SF and AF flags to zero in the EFLAGS register (regardless of whether an invalid-operation exception is detected).

The FCOMI and FUCOMI instructions also pop the register stack following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

The FCOMI/FCOMIP/FUCOMI/FUCOMIP instructions were introduced to the IA-32 Architecture in the P6 family processors and are not available in earlier IA-32 processors.

**Operation**

CASE (relation of operands) OF

- \( \text{ST}(0) > \text{ST}(i) \):
  - \( \text{ZF, PF, CF} \leftarrow 000; \)

- \( \text{ST}(0) < \text{ST}(i) \):
  - \( \text{ZF, PF, CF} \leftarrow 001; \)

- \( \text{ST}(0) = \text{ST}(i) \):
  - \( \text{ZF, PF, CF} \leftarrow 100; \)

ESAC;

IF Instruction is FCOMI or FCOMIP

- IF \( \text{ST}(0) \) or \( \text{ST}(i) \) = NaN or unsupported format
  - THEN
    - \#IA
      - IF FPUControlWord.IM = 1
        - THEN
          - \( \text{ZF, PF, CF} \leftarrow 111; \)
    - FI;
  - FI;

IF Instruction is FUCOMI or FUCOMIP

- IF \( \text{ST}(0) \) or \( \text{ST}(i) \): QNaN, but not SNaN or unsupported format
  - THEN
    - \( \text{ZF, PF, CF} \leftarrow 111; \)
  - ELSE (* \( \text{ST}(0) \) or \( \text{ST}(i) \) is SNaN or unsupported format *)
    - \#IA;
  - IF FPUControlWord.IM = 1

---

FCOMI/FCOMIP/ FUCOMI/FUCOMIP—Compare Floating Point Values and Set EFLAGS
THEN
ZF, PF, CF ← 111;
Ft;
FI;
FI;
FI;

IF Instruction is FCOMIP or FUCOMIP
THEN
PopRegisterStack;
FI;

**FPU Flags Affected**
C1 Set to 0.
C0, C2, C3 Not affected.

**Floating-Point Exceptions**
#IS Stack underflow occurred.
#IA (FCOMI or FCOMIP instruction) One or both operands are NaN values or have unsupported formats.
( FUCOMI or FUCOMIP instruction) One or both operands are SNaN values (but not QNaNs) or have undefined formats. Detection of a QNaN value does not raise an invalid-operand exception.

**Protected Mode Exceptions**
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**
Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**
Same exceptions as in protected mode.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
Same exceptions as in protected mode.
**FCOS—Cosine**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 FF</td>
<td>FCOS</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(0) with its cosine.</td>
</tr>
</tbody>
</table>

**Description**

Computes the cosine of the source operand in register ST(0) and stores the result in ST(0). The source operand must be given in radians and must be within the range $-2^{63}$ to $+2^{63}$. The following table shows the results obtained when taking the cosine of various classes of numbers.

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>$*$</td>
</tr>
<tr>
<td>$-F$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$-0$</td>
<td>$+1$</td>
</tr>
<tr>
<td>$+0$</td>
<td>$+1$</td>
</tr>
<tr>
<td>$+F$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$+\infty$</td>
<td>$*$</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.

* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range $-2^{63}$ to $+2^{63}$ can be reduced to the range of the instruction by subtracting an appropriate integer multiple of $2\pi$ or by using the FPREM instruction with a divisor of $2\pi$. See the section titled “Pi” in Chapter 8 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a discussion of the proper value to use for $\pi$ in performing such reductions.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF $|ST(0)| < 2^{63}$
THEN

$C2 \leftarrow 0;$
ST(0) ← cosine(ST(0));
ELSE (* Source operand is out-of-range *)
    C2 ← 1;
FI;

FPU Flags Affected
C1  Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
    Undefined if C2 is 1.
C2  Set to 1 if outside range (-2^{63} < source operand < +2^{63}); otherwise, set to 0.
C0, C3 Undefined.

Floating-Point Exceptions
#IS  Stack underflow occurred.
#IA  Source operand is an SNaN value, \(\infty\), or unsupported format.
#D   Source is a denormal value.
#P   Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF  If there is a pending x87 FPU exception.
#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FDECSTP—Decrement Stack-Top Pointer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F6</td>
<td>FDECSTP</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement TOP field in FPU status word.</td>
</tr>
</tbody>
</table>

Description
Subtracts one from the TOP field of the FPU status word (decrements the top-of-stack pointer). If the TOP field contains a 0, it is set to 7. The effect of this instruction is to rotate the stack by one position. The contents of the FPU data registers and tag register are not affected.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
IF TOP = 0
  THEN TOP ← 7;
  ELSE TOP ← TOP - 1;
FI;

FPU Flags Affected
The C1 flag is set to 0. The C0, C2, and C3 flags are undefined.

Floating-Point Exceptions
None.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FDIV/FDIVP/FIDIV—Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /6</td>
<td>FDIV m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by m32fp and store result in ST(0).</td>
</tr>
<tr>
<td>DC /6</td>
<td>FDIV m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by m64fp and store result in ST(0).</td>
</tr>
<tr>
<td>D8 F0+i</td>
<td>FDIV ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by ST(i) and store result in ST(0).</td>
</tr>
<tr>
<td>DC F8+i</td>
<td>FDIV ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(i) by ST(0) and store result in ST(i).</td>
</tr>
<tr>
<td>DE F8+i</td>
<td>FDIVP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(i) by ST(0), store result in ST(i), and pop the register stack.</td>
</tr>
<tr>
<td>DE F9</td>
<td>FDIVP</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(1) by ST(0), store result in ST(1), and pop the register stack.</td>
</tr>
<tr>
<td>DA /6</td>
<td>FIDIV m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by m32int and store result in ST(0).</td>
</tr>
<tr>
<td>DE /6</td>
<td>FIDIV m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by m64int and store result in ST(0).</td>
</tr>
</tbody>
</table>

Description

Divides the destination operand by the source operand and stores the result in the destination location. The destination operand (dividend) is always in an FPU register; the source operand (divisor) can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format, word or doubleword integer format.

The no-operand version of the instruction divides the contents of the ST(1) register by the contents of the ST(0) register. The one-operand version divides the contents of the ST(0) register by the contents of a memory location (either a floating-point or an integer value). The two-operand version, divides the contents of the ST(0) register by the contents of the ST(i) register or vice versa.

The FDIVP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point divide instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FDIV rather than FDIVP.

The FIDIV instructions convert an integer source operand to double extended-precision floating-point format before performing the division. When the source operand is an integer 0, it is treated as a +0.
If an unmasked divide-by-zero exception (#Z) is generated, no result is stored; if the exception is masked, an ∞ of the appropriate sign is stored in the destination operand.

The following table shows the results obtained when dividing various classes of numbers, assuming that neither overflow nor underflow occurs.

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>−∞</th>
<th>−F</th>
<th>−0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>−∞</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>−0</td>
<td>−0</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>+∞</td>
<td>+F</td>
<td>+0</td>
<td>−0</td>
<td>−F</td>
<td>+∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−1</td>
<td>+∞</td>
<td>+F</td>
<td>+0</td>
<td>−0</td>
<td>−F</td>
<td>+∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>+∞</td>
<td>**</td>
<td>*</td>
<td>*</td>
<td>**</td>
<td>+∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>−∞</td>
<td>**</td>
<td>*</td>
<td>*</td>
<td>**</td>
<td>+∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+1</td>
<td>−∞</td>
<td>−F</td>
<td>−0</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>−∞</td>
<td>−F</td>
<td>−0</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
<td>−0</td>
<td>−0</td>
<td>+0</td>
<td>+0</td>
<td>+∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
I Means integer.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.
** Indicates floating-point zero-divide (#Z) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

IF SRC = 0
    THEN
        #Z;
    ELSE
        IF Instruction is FIDIV
            THEN
                DEST ← DEST / ConvertToDoubleExtendedPrecisionFP(SRC);
            ELSE (* Source operand is floating-point value *)
                DEST ← DEST / SRC;
        FL;
    FI;
FL;
IF Instruction = FDIVP
   THEN
       PopRegisterStack;
   FI;

**FPU Flags Affected**

- C1: Set to 0 if stack underflow occurred.
  Set if result was rounded up; cleared otherwise.
- C0, C2, C3: Undefined.

**Floating-Point Exceptions**

- #IS: Stack underflow occurred.
- #IA: Operand is an SNaN value or unsupported format.
  ±∞ / ±∞; ±0 / ±0
- #D: Source is a denormal value.
- #Z: DEST / ±0, where DEST is not equal to ±0.
- #U: Result is too small for destination format.
- #O: Result is too large for destination format.
- #P: Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- #GP(0): If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  If the DS, ES, FS, or GS register contains a NULL segment selector.
- #SS(0): If a memory operand effective address is outside the SS segment limit.
- #NM: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #PF(fault-code): If a page fault occurs.
- #AC(0): If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD: If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- #GP: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS: If a memory operand effective address is outside the SS segment limit.
- #NM: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #UD: If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FDIVR/FDIVRP/FIDIVR—Reverse Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /7</td>
<td>FDIVR m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide m32fp by ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC /7</td>
<td>FDIVR m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide m64fp by ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>D8 F8+i</td>
<td>FDIVR ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(i) by ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC F0+i</td>
<td>FDIVR ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by ST(i) and store result in ST(i).</td>
</tr>
<tr>
<td>DE F0+i</td>
<td>FDIVRP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by ST(i), store result in ST(i), and pop the register stack.</td>
</tr>
<tr>
<td>DE F1</td>
<td>FDIVRP</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide ST(0) by ST(1), store result in ST(1), and pop the register stack.</td>
</tr>
<tr>
<td>DA /7</td>
<td>FIDIVR m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide m32int by ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DE /7</td>
<td>FIDIVR m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Divide m16int by ST(0) and store result in ST(0).</td>
</tr>
</tbody>
</table>

Description

Divides the source operand by the destination operand and stores the result in the destination location. The destination operand (divisor) is always in an FPU register; the source operand (dividend) can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format, word or doubleword integer format.

These instructions perform the reverse operations of the FDIV, FDIVP, and FIDIV instructions. They are provided to support more efficient coding.

The no-operand version of the instruction divides the contents of the ST(0) register by the contents of the ST(1) register. The one-operand version divides the contents of a memory location (either a floating-point or an integer value) by the contents of the ST(0) register. The two-operand version, divides the contents of the ST(i) register by the contents of the ST(0) register or vice versa.

The FDIVRP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point divide instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FDIVR rather than FDIVRP.
The FIDIVR instructions convert an integer source operand to double extended-precision floating-point format before performing the division.

If an unmasked divide-by-zero exception (#Z) is generated, no result is stored; if the exception is masked, an \( \infty \) of the appropriate sign is stored in the destination operand.

The following table shows the results obtained when dividing various classes of numbers, assuming that neither overflow nor underflow occurs.

Table 3-35. FDIVR/FDIVRP/FIDIVR Results

<table>
<thead>
<tr>
<th>SRC</th>
<th>−∞</th>
<th>−F</th>
<th>−0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
<td>+∞</td>
<td>+∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>+0</td>
<td>+F</td>
<td>**</td>
<td>**</td>
<td>−F</td>
<td>−0</td>
<td>NaN</td>
</tr>
<tr>
<td>−I</td>
<td>+0</td>
<td>+F</td>
<td>**</td>
<td>**</td>
<td>−F</td>
<td>−0</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>−0</td>
<td>−0</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>−0</td>
<td>−0</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+I</td>
<td>−0</td>
<td>−F</td>
<td>**</td>
<td>**</td>
<td>+F</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>−0</td>
<td>−F</td>
<td>**</td>
<td>**</td>
<td>+F</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
<td>−∞</td>
<td>−∞</td>
<td>+∞</td>
<td>+∞</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
I Means integer.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.
** Indicates floating-point zero-divide (#Z) exception.

When the source operand is an integer 0, it is treated as a +0. This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

IF DEST = 0
THEN
#Z;
ELSE
IF Instruction = FIDIVR
THEN
DEST ← ConvertToDoubleExtendedPrecisionFP(SRC) / DEST;
ELSE (* Source operand is floating-point value *)
DEST ← SRC / DEST;
Ft;
Ft;
IF Instruction = FDIVRP
    THEN
        PopRegisterStack;
    Ft;

FPU Flags Affected
C1
    Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
C0, C2, C3
    Undefined.

Floating-Point Exceptions
#IS
    Stack underflow occurred.
#IA
    Operand is an SNaN value or unsupported format.
    ±∞ / ±∞; ±0 / ±0
#D
    Source is a denormal value.
#Z
    SRC / ±0, where SRC is not equal to ±0.
#U
    Result is too small for destination format.
#O
    Result is too large for destination format.
#P
    Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#GP(0)
    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0)
    If a memory operand effective address is outside the SS segment limit.
#NM
    CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code)
    If a page fault occurs.
#AC(0)
    If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD
    If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP
    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, A-L

#SS If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
**FFREE—Free Floating-Point Register**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DD C0+i</td>
<td>FFREE ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Sets tag for ST(i) to empty.</td>
</tr>
</tbody>
</table>

**Description**

Sets the tag in the FPU tag register associated with register ST(i) to empty (11B). The contents of ST(i) and the FPU stack-top pointer (TOP) are not affected. This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

TAG(i) ← 11B;

**FPU Flags Affected**

C0, C1, C2, C3 undefined.

**Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #MF If there is a pending x87 FPU exception.
- #UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
FICOM/FICOMP—Compare Integer

Description

Compares the value in ST(0) with an integer source operand and sets the condition code flags C0, C2, and C3 in the FPU status word according to the results (see table below). The integer value is converted to double extended-precision floating-point format before the comparison is made.

Table 3-36. FICOM/FICOMP Results

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; SRC</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; SRC</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = SRC</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

These instructions perform an “unordered comparison.” An unordered comparison also checks the class of the numbers being compared (see “FXAM—Examine ModR/M” in this chapter). If either operand is a NaN or is in an undefined format, the condition flags are set to “unordered.”

The sign of zero is ignored, so that –0.0 ← +0.0.

The FICOMP instructions pop the register stack following the comparison. To pop the register stack, the processor marks the ST(0) register empty and increments the stack pointer (TOP) by 1.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

CASE (relation of operands) OF

ST(0) > SRC: C3, C2, C0 ← 000;
ST(0) < SRC: C3, C2, C0 ← 001;
ST(0) = SRC: C3, C2, C0 ← 100;
Unordered: C3, C2, C0 ← 111;
ESAC;

IF Instruction = FICOMP
  THEN
    PopRegisterStack;
FI;

**FPU Flags Affected**

C1           Set to 0.
C0, C2, C3   See table on previous page.

**Floating-Point Exceptions**

#IS         Stack underflow occurred.
#IA         One or both operands are NaN values or have unsupported formats.
#D          One or both operands are denormal values.

**Protected Mode Exceptions**

#GP(0)      If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
            If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0)      If a memory operand effective address is outside the SS segment limit.
#NM         CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0)      If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD         If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP         If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS         If a memory operand effective address is outside the SS segment limit.
#NM         CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD         If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0)      If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

FICOM/FICOMP—Compare Integer
INSTRUCTION SET REFERENCE, A-L

#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**FILD—Load Integer**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /0</td>
<td>FILD m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Push m16int onto the FPU register stack.</td>
</tr>
<tr>
<td>DB /0</td>
<td>FILD m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Push m32int onto the FPU register stack.</td>
</tr>
<tr>
<td>DF /5</td>
<td>FILD m64int</td>
<td>Valid</td>
<td>Valid</td>
<td>Push m64int onto the FPU register stack.</td>
</tr>
</tbody>
</table>

**Description**

Converts the signed-integer source operand into double extended-precision floating-point format and pushes the value onto the FPU register stack. The source operand can be a word, doubleword, or quadword integer. It is loaded without rounding errors. The sign of the source operand is preserved.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{TOP} \leftarrow \text{TOP} - 1; \\
\text{ST}(0) \leftarrow \text{ConvertToDoubleExtendedPrecisionFP}(\text{SRC});
\]

**FPU Flags Affected**

- C1: Set to 1 if stack overflow occurred; set to 0 otherwise.
- C0, C2, C3: Undefined.

**Floating-Point Exceptions**

- #IS: Stack overflow occurred.

**Protected Mode Exceptions**

- #GP(0): If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0): If a memory operand effective address is outside the SS segment limit.
- #NM: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #PF(fault-code): If a page fault occurs.
- #AC(0): If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made.
- #UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- #SS(0) If a memory address referencing the SS segment is in a non-canonical form.
- #GP(0) If the memory address is in a non-canonical form.
- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #MF If there is a pending x87 FPU exception.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD If the LOCK prefix is used.
FINCSTP—Increment Stack-Top Pointer

Description
Adds one to the TOP field of the FPU status word (increments the top-of-stack pointer). If the TOP field contains a 7, it is set to 0. The effect of this instruction is to rotate the stack by one position. The contents of the FPU data registers and tag register are not affected. This operation is not equivalent to popping the stack, because the tag for the previous top-of-stack register is not marked empty.

This instruction's operation is the same in non-64-bit modes and 64-bit mode.

Operation
IF TOP = 7
    THEN TOP ← 0;
    ELSE TOP ← TOP + 1;
FI;

FPU Flags Affected
The C1 flag is set to 0. The C0, C2, and C3 flags are undefined.

Floating-Point Exceptions
None.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-L

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FINIT/FNINIT—Initialize Floating-Point Unit

**Description**

Sets the FPU control, status, tag, instruction pointer, and data pointer registers to their default states. The FPU control word is set to 037FH (round to nearest, all exceptions masked, 64-bit precision). The status word is cleared (no exception flags set, TOP is set to 0). The data registers in the register stack are left unchanged, but they are all tagged as empty (11B). Both the instruction and data pointers are cleared.

The FINIT instruction checks for and handles any pending unmasked floating-point exceptions before performing the initialization; the FNINIT instruction does not.

The assembler issues two instructions for the FINIT instruction (an FWAIT instruction followed by an FNINIT instruction), and the processor executes each of these instructions in separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNINIT instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled “No-Wait FPU Instructions Can Get FPU Interrupt in Window” in Appendix D of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a description of these circumstances. An FNINIT instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

In the Intel387 math coprocessor, the FINIT/FNINIT instruction does not clear the instruction and data pointers.

This instruction affects only the x87 FPU. It does not affect the XMM and MXCSR registers.

---

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DB E3</td>
<td>FINIT</td>
<td>Valid</td>
<td>Valid</td>
<td>Initialize FPU after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DB E3</td>
<td>FNINIT*</td>
<td>Valid</td>
<td>Valid</td>
<td>Initialize FPU without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

**NOTES:**

* See IA-32 Architecture Compatibility section below.
INSTRUCTION SET REFERENCE, A-L

Operation
FPUControlWord ← 037FH;
FPUStatusWord ← 0;
FPUTagWord ← FFFFH;
FPUDataPointer ← 0;
FPUInstructionPointer ← 0;
FPULastInstructionOpcode ← 0;

FPU Flags Affected
C0, C1, C2, C3 set to 0.

Floating-Point Exceptions
None.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FIST/FISTP—Store Integer

The FIST instruction converts the value in the ST(0) register to a signed integer and stores the result in the destination operand. Values can be stored in word or double-word integer format. The destination operand specifies the address where the first byte of the destination value is to be stored.

The FISTP instruction performs the same operation as the FIST instruction and then pops the register stack. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The FISTP instruction also stores values in quadword integer format.

The following table shows the results obtained when storing various classes of numbers in integer format.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /2</td>
<td>FIST m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m16int.</td>
</tr>
<tr>
<td>DB /2</td>
<td>FIST m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m32int.</td>
</tr>
<tr>
<td>DF /3</td>
<td>FISTP m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m16int and pop register stack.</td>
</tr>
<tr>
<td>DB /3</td>
<td>FISTP m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m32int and pop register stack.</td>
</tr>
<tr>
<td>DF /7</td>
<td>FISTP m64int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m64int and pop register stack.</td>
</tr>
</tbody>
</table>

**Description**

The FIST instruction converts the value in the ST(0) register to a signed integer and stores the result in the destination operand. Values can be stored in word or double-word integer format. The destination operand specifies the address where the first byte of the destination value is to be stored.

The FISTP instruction performs the same operation as the FIST instruction and then pops the register stack. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The FISTP instruction also stores values in quadword integer format.

The following table shows the results obtained when storing various classes of numbers in integer format.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$ or Value Too Large for DEST Format</td>
<td>$*$</td>
</tr>
<tr>
<td>$F \leq -1$</td>
<td>$-1$</td>
</tr>
<tr>
<td>$-1 &lt; F &lt; -0$</td>
<td>$**$</td>
</tr>
<tr>
<td>$-0$</td>
<td>$0$</td>
</tr>
<tr>
<td>$+0$</td>
<td>$0$</td>
</tr>
<tr>
<td>$+0 &lt; F &lt; +1$</td>
<td>$**$</td>
</tr>
<tr>
<td>$F \geq +1$</td>
<td>$+1$</td>
</tr>
<tr>
<td>$+\infty$ or Value Too Large for DEST Format</td>
<td>$*$</td>
</tr>
</tbody>
</table>
If the source value is a non-integral value, it is rounded to an integer value, according to the rounding mode specified by the RC field of the FPU control word.

If the converted value is too large for the destination format, or if the source operand is an $\infty$, SNaN, QNAN, or is in an unsupported format, an invalid-arithmetic-operand condition is signaled. If the invalid-operation exception is not masked, an invalid-arithmetic-operand exception (#IA) is generated and no value is stored in the destination operand. If the invalid-operation exception is masked, the integer indefinite value is stored in memory.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

DEST ← Integer(ST(0));

IF Instruction = FISTP
  THEN
    PopRegisterStack;
  FI;

**FPU Flags Affected**

C1          Set to 0 if stack underflow occurred.

Indicates rounding direction of if the inexact exception (#P) is generated: 0 ← not roundup; 1 ← roundup.

Set to 0 otherwise.

C0, C2, C3  Undefined.

**Floating-Point Exceptions**

#IS          Stack underflow occurred.

#IA          Converted value is too large for the destination format.

Source operand is an SNaN, QNaN, ±$\infty$, or unsupported format.

#P            Value cannot be represented exactly in destination format.
Protected Mode Exceptions

#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.
INSTRUCTION SET REFERENCE, A-L

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF  If there is a pending x87 FPU exception.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.
FISTTP—Store Integer with Truncation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compatt/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /1</td>
<td>FISTTP m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m16int with truncation.</td>
</tr>
<tr>
<td>DB /1</td>
<td>FISTTP m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m32int with truncation.</td>
</tr>
<tr>
<td>DD /1</td>
<td>FISTTP m64int</td>
<td>Valid</td>
<td>Valid</td>
<td>Store ST(0) in m64int with truncation.</td>
</tr>
</tbody>
</table>

Description

FISTTP converts the value in ST into a signed integer using truncation (chop) as rounding mode, transfers the result to the destination, and pop ST. FISTTP accepts word, short integer, and long integer destinations.

The following table shows the results obtained when storing various classes of numbers in integer format.

Table 3-38. FISTTP Results

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞ or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>F ≤ −1</td>
<td>−1</td>
</tr>
<tr>
<td>−1 &lt; F &lt; +1</td>
<td>0</td>
</tr>
<tr>
<td>F ≥ +1</td>
<td>+1</td>
</tr>
<tr>
<td>+∞ or Value Too Large for DEST Format</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>*</td>
</tr>
</tbody>
</table>

NOTES:
- F Means finite floating-point value.
- I Means integer.
- * Indicates floating-point invalid-operation (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

DEST ← ST;
pop ST;

Flags Affected

C1 is cleared; C0, C2, C3 undefined.
Numeric Exceptions
Invalid, Stack Invalid (stack underflow), Precision.

Protected Mode Exceptions
#GP(0) If the destination is in a nonwritable segment.
    For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#NM If CR0.EM[bit 2] = 1.
    If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.SSE3[bit 0] = 0.
    If the LOCK prefix is used.

Real Address Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
#NM If CR0.EM[bit 2] = 1.
    If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.SSE3[bit 0] = 0.
    If the LOCK prefix is used.

Virtual 8086 Mode Exceptions
GP(0) If any part of the operand would lie outside of the effective address space from 0 to 0FFFFH.
#NM If CR0.EM[bit 2] = 1.
    If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.SSE3[bit 0] = 0.
    If the LOCK prefix is used.
#PF(fault-code) For a page fault.
#AC(0) For unaligned memory reference if the current privilege is 3.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
If the LOCK prefix is used.
FLD—Load Floating Point Value

**Description**

Pushes the source operand onto the FPU register stack. The source operand can be in single-precision, double-precision, or double extended-precision floating-point format. If the source operand is in single-precision or double-precision floating-point format, it is automatically converted to the double extended-precision floating-point format before being pushed on the stack.

The FLD instruction can also push the value in a selected FPU register [ST(i)] onto the stack. Here, pushing register ST(0) duplicates the stack top.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\begin{align*}
\text{IF SRC is ST}(i) & \rightarrow \\
& \text{temp} \leftarrow \text{ST}(i);
\end{align*}
\]

\[
\begin{align*}
& \text{Ft} \leftarrow \text{TOP} \rightarrow 1;
\end{align*}
\]

\[
\begin{align*}
\text{IF SRC is memory-operand} & \rightarrow \\
& \text{ST}(0) \leftarrow \text{ConvertToDoubleExtendedPrecisionFP}(\text{SRC});
\end{align*}
\]

\[
\begin{align*}
\text{ELSE (* SRC is ST}(i) *) & \rightarrow \\
& \text{ST}(0) \leftarrow \text{temp};
\end{align*}
\]

**FPU Flags Affected**

- C1: Set to 1 if stack overflow occurred; otherwise, set to 0.
- C0, C2, C3: Undefined.

**Floating-Point Exceptions**

- #IS: Stack underflow or overflow occurred.
#IA Source operand is an SNaN. Does not occur if the source operand is in double extended-precision floating-point format (FLD m80fp or FLD ST(i)).

#D Source operand is a denormal value. Does not occur if the source operand is in double extended-precision floating-point format.

Protected Mode Exceptions
#GP(0) If destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.


**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
FLD1/FLDL2T/FLDL2E/FLDPI/FLDLG2/FLDLN2/FLDZ—Load Constant

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 EB</td>
<td>FLD1</td>
<td>Valid</td>
<td>Valid</td>
<td>Push +1.0 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 E9</td>
<td>FLDL2T</td>
<td>Valid</td>
<td>Valid</td>
<td>Push log₂10 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EA</td>
<td>FLDL2E</td>
<td>Valid</td>
<td>Valid</td>
<td>Push log₂e onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EB</td>
<td>FLDPi</td>
<td>Valid</td>
<td>Valid</td>
<td>Push π onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EC</td>
<td>FLDLG2</td>
<td>Valid</td>
<td>Valid</td>
<td>Push log₁₀₂ onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 ED</td>
<td>FLDLN2</td>
<td>Valid</td>
<td>Valid</td>
<td>Push logₑ₂ onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EE</td>
<td>FLDZ</td>
<td>Valid</td>
<td>Valid</td>
<td>Push +0.0 onto the FPU register stack.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.

**Description**

Push one of seven commonly used constants (in double extended-precision floating-point format) onto the FPU register stack. The constants that can be loaded with these instructions include +1.0, +0.0, log₂10, log₂e, π, log₁₀₂, and logₑ₂. For each constant, an internal 66-bit constant is rounded (as specified by the RC field in the FPU control word) to double extended-precision floating-point format. The inexact-result exception (#P) is not generated as a result of the rounding, nor is the C1 flag set in the x87 FPU status word if the value is rounded up.

See the section titled “Pi” in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a description of the π constant.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

When the RC field is set to round-to-nearest, the FPU produces the same constants that is produced by the Intel 8087 and Intel 287 math coprocessors.

**Operation**

TOP ← TOP — 1;
ST(0) ← CONSTANT;

**FPU Flags Affected**

C1 Set to 1 if stack overflow occurred; otherwise, set to 0.
C0, C2, C3 Undefined.
INSTRUCTION SET REFERENCE, A-L

Floating-Point Exceptions

#IS Stack overflow occurred.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FLDCW—Load x87 FPU Control Word

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /5</td>
<td>FLDCW m2byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FPU control word from m2byte.</td>
</tr>
</tbody>
</table>

**Description**

Loads the 16-bit source operand into the FPU control word. The source operand is a memory location. This instruction is typically used to establish or change the FPU’s mode of operation.

If one or more exception flags are set in the FPU status word prior to loading a new FPU control word and the new control word unmasks one or more of those exceptions, a floating-point exception will be generated upon execution of the next floating-point instruction (except for the no-wait floating-point instructions, see the section titled “Software Exception Handling” in Chapter 8 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*). To avoid raising exceptions when changing FPU operating modes, clear any pending exceptions (using the FCLEX or FNCLEX instruction) before loading the new control word.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{FPUCW ControlWord} \leftarrow \text{SRC};
\]

**FPU Flags Affected**

C0, C1, C2, C3 undefined.

**Floating-Point Exceptions**

None; however, this operation might unmask a pending exception in the FPU status word. That exception is then generated upon execution of the next “waiting” floating-point instruction.

**Protected Mode Exceptions**

- #GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0)  If a memory operand effective address is outside the SS segment limit.
- #NM     CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #PF(fault-code) If a page fault occurs.
INSTRUCTION SET REFERENCE, A-L

#AC(0)  If alignment checking is enabled and an unaligned memory
reference is made while the current privilege level is 3.
#UD    If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP     If a memory operand effective address is outside the CS, DS,
        ES, FS, or GS segment limit.
#SS     If a memory operand effective address is outside the SS
        segment limit.
#NM     CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD    If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0)  If a memory operand effective address is outside the CS, DS,
        ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS
        segment limit.
#NM     CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made.
#UD    If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-
canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#NM     CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF     If there is a pending x87 FPU exception.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made while the current privilege level is 3.
#UD    If the LOCK prefix is used.
FLDENV—Load x87 FPU Environment

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /4</td>
<td>FLDENV</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FPU environment from m14byte or m28byte.</td>
</tr>
</tbody>
</table>

Description

Loads the complete x87 FPU operating environment from memory into the FPU registers. The source operand specifies the first byte of the operating-environment data in memory. This data is typically written to the specified memory location by a FSTENV or FNSTENV instruction.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. Figures 8-9 through 8-12 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, show the layout in memory of the loaded environment, depending on the operating mode of the processor (protected or real) and the current operand-size attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used.

The FLDENV instruction should be executed in the same operating mode as the corresponding FSTENV/FNSTENV instruction.

If one or more unmasked exception flags are set in the new FPU status word, a floating-point exception will be generated upon execution of the next floating-point instruction (except for the no-wait floating-point instructions, see the section titled "Software Exception Handling" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). To avoid generating exceptions when loading a new environment, clear all the exception flags in the FPU status word that is being loaded.

If a page or limit fault occurs during the execution of this instruction, the state of the x87 FPU registers as seen by the fault handler may be different than the state being loaded from memory. In such situations, the fault handler should ignore the status of the x87 FPU registers, handle the fault, and return. The FLDENV instruction will then complete the loading of the x87 FPU registers with no resulting context inconsistency.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

FPUCtrlWord ← SRC[FPUCtrlWord];
FPUStWord ← SRC[FPUStWord];
FPUTagWord ← SRC[FPUTagWord];
FPUD ataPointer ← SRC[FPUD ataPointer];
FPUInstrPointer ← SRC[FPUInstrPointer];
FPULastInstructionOpcode ← SRC[FPULastInstructionOpcode];
FPU Flags Affected
The C0, C1, C2, C3 flags are loaded.

Floating-Point Exceptions
None; however, if an unmasked exception is loaded in the status word, it is generated upon execution of the next “waiting” floating-point instruction.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
       If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.
**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#MF If there is a pending x87 FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
**FMUL/FMULP/FIMUL—Multiply**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /1</td>
<td>FMUL m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by m32fp and store result in ST(0).</td>
</tr>
<tr>
<td>DC /1</td>
<td>FMUL m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by m64fp and store result in ST(0).</td>
</tr>
<tr>
<td>D8 C8+i</td>
<td>FMUL ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by ST(i) and store result in ST(0).</td>
</tr>
<tr>
<td>DC C8+i</td>
<td>FMUL ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(i) by ST(0) and store result in ST(i).</td>
</tr>
<tr>
<td>DE C8+i</td>
<td>FMULP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(i) by ST(0), store result in ST(i), and pop the register stack.</td>
</tr>
<tr>
<td>DE C9</td>
<td>FMULP</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(1) by ST(0), store result in ST(1), and pop the register stack.</td>
</tr>
<tr>
<td>DA /1</td>
<td>FIMUL m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by m32int and store result in ST(0).</td>
</tr>
<tr>
<td>DE /1</td>
<td>FIMUL m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply ST(0) by m16int and store result in ST(0).</td>
</tr>
</tbody>
</table>

**Description**

Multiples the destination and source operands and stores the product in the destination location. The destination operand is always an FPU data register; the source operand can be an FPU data register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format or in word or doubleword integer format.

The no-operand version of the instruction multiplies the contents of the ST(1) register by the contents of the ST(0) register and stores the product in the ST(1) register. The one-operand version multiplies the contents of the ST(0) register by the contents of a memory location (either a floating point or an integer value) and stores the product in the ST(0) register. The two-operand version, multiplies the contents of the ST(0) register by the contents of the ST(i) register, or vice versa, with the result being stored in the register specified with the first operand (the destination operand).

The FMULP instructions perform the additional operation of popping the FPU register stack after storing the product. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point multiply instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FMUL rather than FMULP.
The FIMUL instructions convert an integer source operand to double extended-precision floating-point format before performing the multiplication.

The sign of the result is always the exclusive-OR of the source signs, even if one or more of the values being multiplied is 0 or ∞. When the source operand is an integer 0, it is treated as a +0.

The following table shows the results obtained when multiplying various classes of numbers, assuming that neither overflow nor underflow occurs.

**Table 3-39. FMUL/FMULP/FIMUL Results**

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>− ∞</th>
<th>− F</th>
<th>− 0</th>
<th>+ 0</th>
<th>+ F</th>
<th>+ ∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>− ∞</td>
<td>− ∞</td>
<td>+ ∞</td>
<td>*</td>
<td>*</td>
<td>− ∞</td>
<td>− ∞</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>− F</td>
<td>+ ∞</td>
<td>+ F</td>
<td>+ 0</td>
<td>− 0</td>
<td>− F</td>
<td>− ∞</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>− I</td>
<td>+ ∞</td>
<td>+ F</td>
<td>+ 0</td>
<td>− 0</td>
<td>− F</td>
<td>− ∞</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>− 0</td>
<td>*</td>
<td>+ 0</td>
<td>+ 0</td>
<td>− 0</td>
<td>− 0</td>
<td>*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+ 0</td>
<td>*</td>
<td>− 0</td>
<td>− 0</td>
<td>+ 0</td>
<td>+ 0</td>
<td>*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+ I</td>
<td>− ∞</td>
<td>− F</td>
<td>− 0</td>
<td>+ 0</td>
<td>+ F</td>
<td>+ ∞</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+ F</td>
<td>− ∞</td>
<td>− F</td>
<td>− 0</td>
<td>+ 0</td>
<td>+ F</td>
<td>+ ∞</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+ ∞</td>
<td>− ∞</td>
<td>− ∞</td>
<td>*</td>
<td>*</td>
<td>+ ∞</td>
<td>+ ∞</td>
<td>NaN</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
- F Means finite floating-point value.
- I Means Integer.
- * Indicates invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF Instruction = FIMUL
    THEN
        DEST ← DEST * ConvertToDoubleExtendedPrecisionFP(SRC);
    ELSE (* Source operand is floating-point value *)
        DEST ← DEST * SRC;
    FI;

IF Instruction = FMULP
    THEN
        PopRegisterStack;
    FI;

**FMUL/FMULP/FIMUL—Multiply**
FPU Flags Affected
C1 Set to 0 if stack underflow occurred.
    Set if result was rounded up; cleared otherwise.
C0, C2, C3 Undefined.

Floating-Point Exceptions
#IS Stack underflow occurred.
#IA Operand is an SNaN value or unsupported format.
    One operand is ±0 and the other is ±∞.
#D Source operand is a denormal value.
#U Result is too small for destination format.
#O Result is too large for destination format.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
INSTRUCTION SET REFERENCE, A-L

FMUL/FMULP/FIMUL—Multiply

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FNOP—No Operation

Description
Performs no FPU operation. This instruction takes up space in the instruction stream but does not affect the FPU or machine context, except the EIP register.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

FPU Flags Affected

C0, C1, C2, C3 undefined.

Floating-Point Exceptions

None.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

Same exceptions as in protected mode.
**FPATAN—Partial Arctangent**

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F3</td>
<td>FPATAN</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(1) with arctan(ST(1)/ST(0)) and pop the register stack.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.

**Description**

Computes the arctangent of the source operand in register ST(1) divided by the source operand in register ST(0), stores the result in ST(1), and pops the FPU register stack. The result in register ST(0) has the same sign as the source operand ST(1) and a magnitude less than \( +\pi \).

The FPATAN instruction returns the angle between the X axis and the line from the origin to the point (X,Y), where Y (the ordinate) is ST(1) and X (the abscissa) is ST(0). The angle depends on the sign of X and Y independently, not just on the sign of the ratio Y/X. This is because a point (−X,Y) is in the second quadrant, resulting in an angle between \( \pi/2 \) and \( \pi \), while a point (X,−Y) is in the fourth quadrant, resulting in an angle between 0 and −\( \pi/2 \). A point (−X,−Y) is in the third quadrant, giving an angle between −\( \pi/2 \) and −\( \pi \).

The following table shows the results obtained when computing the arctangent of various classes of numbers, assuming that underflow does not occur.
There is no restriction on the range of source operands that FPATAN can accept. This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

The source operands for this instruction are restricted for the 80287 math coprocessor to the following range:

\[ 0 \leq |ST(1)| < |ST(0)| < +\infty \]

**Operation**

\[ ST(1) \leftarrow \arctan(ST(1) / ST(0)); \]

\[ \text{PopRegisterStack}; \]

---

**Table 3-40. FPATAN Results**

<table>
<thead>
<tr>
<th>ST(1)</th>
<th>ST(0)</th>
<th>−∞</th>
<th>−F</th>
<th>−0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>−3π/4*</td>
<td>−π/2</td>
<td>−π/2</td>
<td>−π/2</td>
<td>−π/2</td>
<td>−π/2</td>
<td>−π/4*</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>−p</td>
<td>−π to −π/2</td>
<td>−π/2</td>
<td>−π/2</td>
<td>−π/2</td>
<td>−π/2 to −0</td>
<td>−0</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>−p</td>
<td>−p</td>
<td>−p*</td>
<td>−0*</td>
<td>−0</td>
<td>−0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+0</td>
<td>+p</td>
<td>+p</td>
<td>+π*</td>
<td>+0*</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+F</td>
<td>+p</td>
<td>+π to +π/2</td>
<td>+π/2</td>
<td>+π/2</td>
<td>+π/2 to +0</td>
<td>+0</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+∞</td>
<td>+3π/4*</td>
<td>+π/2</td>
<td>+π/2</td>
<td>+π/2</td>
<td>+π/2</td>
<td>+π/4*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.

* Table 8-10 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, specifies that the ratios 0/0 and ∞/∞ generate the floating-point invalid arithmetic-operation exception and, if this exception is masked, the floating-point QNaN indefinite value is returned. With the FPATAN instruction, the 0/0 or ∞/∞ value is actually not calculated using division. Instead, the arctangent of the two variables is derived from a standard mathematical formulation that is generalized to allow complex numbers as arguments. In this complex variable formulation, arctangent(0,0) etc. has well defined values. These values are needed to develop a library to compute transcendental functions with complex arguments, based on the FPU functions that only allow floating-point values as arguments.

There is no restriction on the range of source operands that FPATAN can accept.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
FPATAN—Partial Arctangent

FPU Flags Affected
C1 Set to 0 if stack underflow occurred.
Set if result was rounded up; cleared otherwise.
C0, C2, C3 Undefined.

Floating-Point Exceptions
#IS Stack underflow occurred.
#IA Source operand is an SNaN value or unsupported format.
#D Source operand is a denormal value.
#U Result is too small for destination format.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FPREM—Partial Remainder

Description

Computes the remainder obtained from dividing the value in the ST(0) register (the dividend) by the value in the ST(1) register (the divisor or modulus), and stores the result in ST(0). The remainder represents the following value:

\[ \text{Remainder} \leftarrow \text{ST}(0) - (Q \times \text{ST}(1)) \]

Here, \( Q \) is an integer value that is obtained by truncating the floating-point number quotient of \([\text{ST}(0) / \text{ST}(1)]\) toward zero. The sign of the remainder is the same as the sign of the dividend. The magnitude of the remainder is less than that of the modulus, unless a partial remainder was computed (as described below).

This instruction produces an exact result; the inexact-result exception does not occur and the rounding control has no effect. The following table shows the results obtained when computing the remainder of various classes of numbers, assuming that underflow does not occur.

Table 3-41. FPREM Results

<table>
<thead>
<tr>
<th>ST(1)</th>
<th>-∞</th>
<th>-F</th>
<th>-0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-∞</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>-F</td>
<td>ST(0)</td>
<td>-F or -0</td>
<td>**</td>
<td>**</td>
<td>-F or -0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>-0</td>
<td>-0</td>
<td>-0</td>
<td>*</td>
<td>*</td>
<td>-0</td>
<td>-0</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>ST(0)</td>
<td>+F or +0</td>
<td>**</td>
<td>**</td>
<td>+F or +0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:

F Means finite floating-point value.

* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

** Indicates floating-point zero-divide (#Z) exception.

When the result is 0, its sign is the same as that of the dividend. When the modulus is \( \infty \), the result is equal to the value in ST(0).
The FPREM instruction does not compute the remainder specified in IEEE Std 754. The IEEE specified remainder can be computed with the FPREM1 instruction. The FPREM instruction is provided for compatibility with the Intel 8087 and Intel287 math coprocessors.

The FPREM instruction gets its name "partial remainder" because of the way it computes the remainder. This instruction arrives at a remainder through iterative subtraction. It can, however, reduce the exponent of ST(0) by no more than 63 in one execution of the instruction. If the instruction succeeds in producing a remainder that is less than the modulus, the operation is complete and the C2 flag in the FPU status word is cleared. Otherwise, C2 is set, and the result in ST(0) is called the partial remainder. The exponent of the partial remainder will be less than the exponent of the original dividend by at least 32. Software can re-execute the instruction (using the partial remainder in ST(0) as the dividend) until C2 is cleared. (Note that while executing such a remainder-computation loop, a higher-priority interrupting routine that needs the FPU can force a context switch in-between the instructions in the loop.)

An important use of the FPREM instruction is to reduce the arguments of periodic functions. When reduction is complete, the instruction stores the three least-significant bits of the quotient in the C3, C1, and C0 flags of the FPU status word. This information is important in argument reduction for the tangent function (using a modulus of π/4), because it locates the original angle in the correct one of eight sectors of the unit circle.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
D \leftarrow \text{exponent}(\text{ST}(0)) - \text{exponent}(\text{ST}(1));
\]

**IF** \( D < 64 \)

**THEN**

\[
Q \leftarrow \text{Integer}(\text{TruncateTowardZero}(\text{ST}(0) / \text{ST}(1))); \\
\text{ST}(0) \leftarrow \text{ST}(0) - (\text{ST}(1) \times Q); \\
C2 \leftarrow 0; \\
C0, C3, C1 \leftarrow \text{LeastSignificantBits}(Q); (* Q2, Q1, Q0 *)
\]

**ELSE**

\[
C2 \leftarrow 1; \\
N \leftarrow \text{An implementation-dependent number between 32 and 63}; \\
QQ \leftarrow \text{Integer}(\text{TruncateTowardZero}((\text{ST}(0) / \text{ST}(1)) / 2^{(D - N)})); \\
\text{ST}(0) \leftarrow \text{ST}(0) - (\text{ST}(1) \times QQ \times 2^{(D - N)});
\]

**FI**
FPU Flags Affected

- C0: Set to bit 2 (Q2) of the quotient.
- C1: Set to 0 if stack underflow occurred; otherwise, set to least significant bit of quotient (Q0).
- C2: Set to 0 if reduction complete; set to 1 if incomplete.
- C3: Set to bit 1 (Q1) of the quotient.

Floating-Point Exceptions

- #IS: Stack underflow occurred.
- #IA: Source operand is an SNaN value, modulus is 0, dividend is $\infty$, or unsupported format.
- #D: Source operand is a denormal value.
- #U: Result is too small for destination format.

Protected Mode Exceptions

- #NM: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #MF: If there is a pending x87 FPU exception.
- #UD: If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**FPREM1—Partial Remainder**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F5</td>
<td>FPREM1</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(0) with the IEEE remainder obtained from dividing ST(0) by ST(1).</td>
</tr>
</tbody>
</table>

**Description**

Computes the IEEE remainder obtained from dividing the value in the ST(0) register (the dividend) by the value in the ST(1) register (the divisor or *modulus*), and stores the result in ST(0). The remainder represents the following value:

\[
\text{Remainder} \leftarrow ST(0) - (Q \times ST(1))
\]

Here, Q is an integer value that is obtained by rounding the floating-point number quotient of \([ST(0) / ST(1)]\) toward the nearest integer value. The magnitude of the remainder is less than or equal to half the magnitude of the modulus, unless a partial remainder was computed (as described below).

This instruction produces an exact result; the precision (inexact) exception does not occur and the rounding control has no effect. The following table shows the results obtained when computing the remainder of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>−∞</th>
<th>−F</th>
<th>−0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>ST(0)</td>
<td>±F or −0</td>
<td>**</td>
<td>**</td>
<td>±F or −0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>−0</td>
<td>−0</td>
<td>*</td>
<td>*</td>
<td>−0</td>
<td>-0</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>ST(0)</td>
<td>±F or +0</td>
<td>**</td>
<td>**</td>
<td>±F or +0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
</tbody>
</table>

| NaN   | NaN | NaN | NaN | NaN | NaN | NaN |

**NOTES:**

- **F** Means finite floating-point value.
- * Indicates floating-point invalid-arithmetic-operand (#IA) exception.
- **Indicates floating-point zero-divide (#Z) exception.

When the result is 0, its sign is the same as that of the dividend. When the modulus is \(∞\), the result is equal to the value in ST(0).
The FPREM1 instruction computes the remainder specified in IEEE Standard 754. This instruction operates differently from the FPREM instruction in the way that it rounds the quotient of ST(0) divided by ST(1) to an integer (see the "Operation" section below).

Like the FPREM instruction, FPREM1 computes the remainder through iterative subtraction, but can reduce the exponent of ST(0) by no more than 63 in one execution of the instruction. If the instruction succeeds in producing a remainder that is less than one half the modulus, the operation is complete and the C2 flag in the FPU status word is cleared. Otherwise, C2 is set, and the result in ST(0) is called the partial remainder. The exponent of the partial remainder will be less than the exponent of the original dividend by at least 32. Software can re-execute the instruction (using the partial remainder in ST(0) as the dividend) until C2 is cleared. (Note that while executing such a remainder-computation loop, a higher-priority interrupting routine that needs the FPU can force a context switch in-between the instructions in the loop.)

An important use of the FPREM1 instruction is to reduce the arguments of periodic functions. When reduction is complete, the instruction stores the three least-significant bits of the quotient in the C3, C1, and C0 flags of the FPU status word. This information is important in argument reduction for the tangent function (using a modulus of π/4), because it locates the original angle in the correct one of eight sectors of the unit circle.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[ D \leftarrow \text{exponent(ST(0))} - \text{exponent(ST(1))}; \]

IF \( D < 64 \)

THEN

\[ Q \leftarrow \text{Integer(RoundTowardNearestInteger(ST(0) / ST(1))));} \]
\[ \text{ST}(0) \leftarrow \text{ST}(0) - (\text{ST}(1) \times Q); \]
\[ C2 \leftarrow 0; \]
\[ C0, C3, C1 \leftarrow \text{LeastSignificantBits}(Q); (* Q2, Q1, Q0 *) \]

ELSE

\[ C2 \leftarrow 1; \]
\[ N \leftarrow \text{An implementation-dependent number between 32 and 63}; \]
\[ QQ \leftarrow \text{Integer(TruncateTowardZero((ST(0) / ST(1)) / 2^{(D - N)}));} \]
\[ \text{ST}(0) \leftarrow \text{ST}(0) - (\text{ST}(1) \times QQ \times 2^{(D - N)}); \]

FI;

**FPU Flags Affected**

C0 Set to bit 2 (Q2) of the quotient.

C1 Set to 0 if stack underflow occurred; otherwise, set to least significant bit of quotient (Q0).
C2 Set to 0 if reduction complete; set to 1 if incomplete.
C3 Set to bit 1 (Q1) of the quotient.

**Floating-Point Exceptions**

#IS Stack underflow occurred.
#IA Source operand is an SNaN value, modulus (divisor) is 0, dividend is $\infty$, or unsupported format.
#D Source operand is a denormal value.
#U Result is too small for destination format.

**Protected Mode Exceptions**

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
FPTAN—Partial Tangent

Description
Computes the tangent of the source operand in register ST(0), stores the result in ST(0), and pushes a 1.0 onto the FPU register stack. The source operand must be given in radians and must be less than ±2^63. The following table shows the unmasked results obtained when computing the partial tangent of various classes of numbers, assuming that underflow does not occur.

Table 3-43. FPTAN Results

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>− ∞</td>
<td>*</td>
</tr>
<tr>
<td>− F</td>
<td>− F to + F</td>
</tr>
<tr>
<td>− 0</td>
<td>- 0</td>
</tr>
<tr>
<td>+ 0</td>
<td>+ 0</td>
</tr>
<tr>
<td>+ F</td>
<td>− F to + F</td>
</tr>
<tr>
<td>+ ∞</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range −2^63 to +2^63 can be reduced to the range of the instruction by subtracting an appropriate integer multiple of 2π or by using the FPREM instruction with a divisor of 2π. See the section titled “Pi” in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for a discussion of the proper value to use for π in performing such reductions.

The value 1.0 is pushed onto the register stack after the tangent has been computed to maintain compatibility with the Intel 8087 and Intel287 math coprocessors. This operation also simplifies the calculation of other trigonometric functions. For instance, the cotangent (which is the reciprocal of the tangent) can be computed by executing a FDIVR instruction after the FPTAN instruction.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF \( ST(0) < 2^{63} \)

THEN

\[
C2 \leftarrow 0; \\
ST(0) \leftarrow \tan(ST(0)); \\
TOP \leftarrow TOP - 1; \\
ST(0) \leftarrow 1.0;
\]

ELSE (* Source operand is out-of-range *)

\[
C2 \leftarrow 1;
\]

FI;

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred; set to 1 if stack overflow occurred.
  
  Set if result was rounded up; cleared otherwise.

- **C2** Set to 1 if outside range \((-2^{63} < \text{source operand} < +2^{63})\); otherwise, set to 0.

- **C0, C3** Undefined.

**Floating-Point Exceptions**

- **#IS** Stack underflow or overflow occurred.
- **#IA** Source operand is an SNaN value, \(\infty\), or unsupported format.
- **#D** Source operand is a denormal value.
- **#U** Result is too small for destination format.
- **#P** Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **#NM** \(\text{CR0.EM}[\text{bit 2}] \text{ or CR0.TS}[\text{bit 3}] = 1\).
- **#MF** If there is a pending x87 FPU exception.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-L

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FRNDINT—Round to Integer

Description
Rounds the source value in the ST(0) register to the nearest integral value, depending on the current rounding mode (setting of the RC field of the FPU control word), and stores the result in ST(0).
If the source value is $\infty$, the value is not changed. If the source value is not an integral value, the floating-point inexact-result exception (#P) is generated.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
ST(0) ← RoundToIntegralValue(ST(0));

FPU Flags Affected
C1 Set to 0 if stack underflow occurred.
Set if result was rounded up; cleared otherwise.
C0, C2, C3 Undefined.

Floating-Point Exceptions
#IS Stack underflow occurred.
#IA Source operand is an SNaN value or unsupported format.
#D Source operand is a denormal value.
#P Source operand is not an integral value.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-L

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FRSTOR—Restore x87 FPU State

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DD /4</td>
<td>FRSTOR m94/108byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FPU state from m94byte or m108byte.</td>
</tr>
</tbody>
</table>

**Description**

Loads the FPU state (operating environment and register stack) from the memory area specified with the source operand. This state data is typically written to the specified memory location by a previous FSAVE/FNSAVE instruction.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. Figures 8-9 through 8-12 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, show the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the current operand-size attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used. The contents of the FPU register stack are stored in the 80 bytes immediately following the operating environment image.

The FRSTOR instruction should be executed in the same operating mode as the corresponding FSAVE/FNSAVE instruction.

If one or more unmasked exception bits are set in the new FPU status word, a floating-point exception will be generated. To avoid raising exceptions when loading a new operating environment, clear all the exception flags in the FPU status word that is being loaded.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

FPUControlWord ← SRC[FPUControlWord];
FPUStatusWord ← SRC[FPUStatusWord];
FPUTagWord ← SRC[FPUTagWord];
FPUDataPointer ← SRC[FPUDataPointer];
FPUIInstructionPointer ← SRC[FPUIInstructionPointer];
FPULastInstructionOpcode ← SRC[FPULastInstructionOpcode];

ST(0) ← SRC[ST(0)];
ST(1) ← SRC[ST(1)];
ST(2) ← SRC[ST(2)];
ST(3) ← SRC[ST(3)];
ST(4) ← SRC[ST(4)];
ST(5) ← SRC[ST(5)];
ST(6) ← SRC[ST(6)];
ST(7) ← SRC[ST(7)];

**FPU Flags Affected**
The C0, C1, C2, C3 flags are loaded.

**Floating-Point Exceptions**
None; however, this operation might unmask an existing exception that has been detected but not generated, because it was masked. Here, the exception is generated at the completion of the instruction.

**Protected Mode Exceptions**
- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**
- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#UD** If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**
- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)** If a page fault occurs.
INSTRUCTION SET REFERENCE, A-L

FRSTOR—Restore x87 FPU State

#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made.
#UD     If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-
        canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#NM     CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made while the current privilege level is 3.
#UD     If the LOCK prefix is used.
FSAVE/FNSAVE—Store x87 FPU State

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DD /6</td>
<td>FSAVE m94/108byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU state to m94byte or m108byte after checking for pending unmasked floating-point exceptions. Then re-initialize the FPU.</td>
</tr>
<tr>
<td>DD /6</td>
<td>FNSAVE m94/108byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU environment to m94byte or m108byte without checking for pending unmasked floating-point exceptions. Then re-initialize the FPU.</td>
</tr>
</tbody>
</table>

NOTES:

* See IA-32 Architecture Compatibility section below.

Description

Stores the current FPU state (operating environment and register stack) at the specified destination in memory, and then re-initializes the FPU. The FSAVE instruction checks for and handles pending unmasked floating-point exceptions before storing the FPU state; the FNSAVE instruction does not.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. Figures 8-9 through 8-12 in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, show the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the current operand-size attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used. The contents of the FPU register stack are stored in the 80 bytes immediately follow the operating environment image.

The saved image reflects the state of the FPU after all floating-point instructions preceding the FSAVE/FNSAVE instruction in the instruction stream have been executed.

After the FPU state has been saved, the FPU is reset to the same default values it is set to with the FINIT/FNINIT instructions (see "FINIT/FNINIT—Initialize Floating-Point Unit" in this chapter).

The FSAVE/FNSAVE instructions are typically used when the operating system needs to perform a context switch, an exception handler needs to use the FPU, or an application program needs to pass a “clean” FPU to a procedure.

The assembler issues two instructions for the FSAVE instruction (an FWAIT instruction followed by an FNSAVE instruction), and the processor executes each of these
instructions separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

For Intel math coprocessors and FPUs prior to the Intel Pentium processor, an FWAIT instruction should be executed before attempting to read from the memory image stored with a prior FSAVE/FNSAVE instruction. This FWAIT instruction helps ensure that the storage operation has been completed.

When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNSAVE instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled “No-Wait FPU Instructions Can Get FPU Interrupt in Window” in Appendix D of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a description of these circumstances. An FNSAVE instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

**Operation**

(* Save FPU State and Registers *)

DEST[FPUC] ← FPUC;
DEST[FPUSt] ← FPUSt;
DEST[FPUTag] ← FPUTag;
DEST[FPUDat] ← FPUDat;
DEST[FPUInstr] ← FPUInstr;
DEST[FPULast] ← FPULast;

DEST[ST(0)] ← ST(0);
DEST[ST(1)] ← ST(1);
DEST[ST(2)] ← ST(2);
DEST[ST(3)] ← ST(3);
DEST[ST(4)] ← ST(4);
DEST[ST(5)] ← ST(5);
DEST[ST(6)] ← ST(6);
DEST[ST(7)] ← ST(7);

(* Initialize FPU *)

FPUC ← 037FH;
FPUSt ← 0;
FPUTag ← FFFFH;
FPUDat ← 0;
FPUInstr ← 0;
FPULast ← 0;
FPU Flags Affected
The C0, C1, C2, and C3 flags are saved and then cleared.

Floating-Point Exceptions
None.

Protected Mode Exceptions
- **#GP(0)**: If destination is located in a non-writable segment.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used.

Real-Address Mode Exceptions
- **#GP**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS**: If a memory operand effective address is outside the SS segment limit.
- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#UD**: If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made.
- **#UD**: If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
FScale—Scale

**Description**
Truncates the value in the source operand (toward 0) to an integral value and adds that value to the exponent of the destination operand. The destination and source operands are floating-point values located in registers ST(0) and ST(1), respectively. This instruction provides rapid multiplication or division by integral powers of 2. The following table shows the results obtained when scaling various classes of numbers, assuming that neither overflow nor underflow occurs.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>−∞</th>
<th>−F</th>
<th>−0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>NaN</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>−0</td>
<td>−F</td>
<td>−F</td>
<td>−F</td>
<td>−F</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>−0</td>
<td>−0</td>
<td>−0</td>
<td>−0</td>
<td>+0</td>
<td>NaN</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>+0</td>
<td>+F</td>
<td>+F</td>
<td>+F</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>NaN</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**
- F Means finite floating-point value.

In most cases, only the exponent is changed and the mantissa (significand) remains unchanged. However, when the value being scaled in ST(0) is a denormal value, the mantissa is also changed and the result may turn out to be a normalized number. Similarly, if overflow or underflow results from a scale operation, the resulting mantissa will differ from the source’s mantissa.

The FSCALE instruction can also be used to reverse the action of the FXTRACT instruction, as shown in the following example:

```
FXTRACT;
FScale;
FSTP ST(1);
```

In this example, the FXTRACT instruction extracts the significand and exponent from the value in ST(0) and stores them in ST(0) and ST(1) respectively. The FSCALE then scales the significand in ST(0) by the exponent in ST(1), recreating the original value.
before the FXTRACT operation was performed. The FSTP ST(1) instruction overwrites the exponent (extracted by the FXTRACT instruction) with the recreated value, which returns the stack to its original state with only one register [ST(0)] occupied.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{ST}(0) \leftarrow \text{ST}(0) \times 2^{\text{RoundTowardZero}(\text{ST}(1))};
\]

**FPU Flags Affected**

- **C1**: Set to 0 if stack underflow occurred.
  - Set if result was rounded up; cleared otherwise.
- **C0, C2, C3**: Undefined.

**Floating-Point Exceptions**

- **#IS**: Stack underflow occurred.
- **#IA**: Source operand is an SNaN value or unsupported format.
- **#D**: Source operand is a denormal value.
- **#U**: Result is too small for destination format.
- **#O**: Result is too large for destination format.
- **#P**: Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#MF**: If there is a pending x87 FPU exception.
- **#UD**: If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
FSIN—Sine

Description
Computes the sine of the source operand in register ST(0) and stores the result in ST(0). The source operand must be given in radians and must be within the range \(-2^{63}\) to \(+2^{63}\). The following table shows the results obtained when taking the sine of various classes of numbers, assuming that underflow does not occur.

Table 3-45. FSIN Results

<table>
<thead>
<tr>
<th>SRC (ST(0))</th>
<th>DEST (ST(0))</th>
</tr>
</thead>
<tbody>
<tr>
<td>(-\infty)</td>
<td>*</td>
</tr>
<tr>
<td>(-F)</td>
<td>(-1) to (+1)</td>
</tr>
<tr>
<td>(-0)</td>
<td>(-0)</td>
</tr>
<tr>
<td>(+0)</td>
<td>(+0)</td>
</tr>
<tr>
<td>(+F)</td>
<td>(-1) to (+1)</td>
</tr>
<tr>
<td>(+\infty)</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range \(-2^{63}\) to \(+2^{63}\) can be reduced to the range of the instruction by subtracting an appropriate integer multiple of \(2\pi\) or by using the FPREM instruction with a divisor of \(2\pi\). See the section titled “Pi” in Chapter 8 of the Intel® 64 and IA-32Architectures Software Developer’s Manual, Volume 1, for a discussion of the proper value to use for \(\pi\) in performing such reductions.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

\[
\text{IF ST}(0) < 2^{63} \\
\quad \text{THEN} \\
\quad \quad \text{C2} \leftarrow 0;
\]
FSIN—Sine

ST(0) ← sin(ST(0));
ELSE (* Source operand out of range *)
    C2 ← 1;
FI;

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred.
  Set if result was rounded up; cleared otherwise.
- **C2** Set to 1 if outside range (−2^{63} < source operand < +2^{63}); otherwise, set to 0.
- **C0, C3** Undefined.

**Floating-Point Exceptions**

- #IS Stack underflow occurred.
- #IA Source operand is an SNaN value, ∞, or unsupported format.
- #D Source operand is a denormal value.
- #P Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #MF If there is a pending x87 FPU exception.
- #UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**
Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**
Same exceptions as in protected mode.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
Same exceptions as in protected mode.
FSINCOS—Sine and Cosine

**Description**

Computes both the sine and the cosine of the source operand in register ST(0), stores the sine in ST(0), and pushes the cosine onto the top of the FPU register stack. (This instruction is faster than executing the FSIN and FCOS instructions in succession.)

The source operand must be given in radians and must be within the range $-2^{63}$ to $+2^{63}$. The following table shows the results obtained when taking the sine and cosine of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>SRC</th>
<th>ST(0)</th>
<th>ST(1) Cosine</th>
<th>ST(0) Sine</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
</tr>
<tr>
<td>$-F$</td>
<td>$-1$ to $+1$</td>
<td>$-1$ to $+1$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$0$</td>
<td>$+1$</td>
<td>$0$</td>
<td>$0$</td>
</tr>
<tr>
<td>$+0$</td>
<td>$+1$</td>
<td>$+0$</td>
<td>$+0$</td>
</tr>
<tr>
<td>$+F$</td>
<td>$-1$ to $+1$</td>
<td>$-1$ to $+1$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range $-2^{63}$ to $+2^{63}$ can be reduced to the range of the instruction by subtracting an appropriate integer multiple of $2\pi$ or by using the FPREM instruction with a divisor of $2\pi$. See the section titled “Pi” in Chapter 8 of the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for a discussion of the proper value to use for $\pi$ in performing such reductions.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
Operation

IF \( ST(0) < 2^{63} \)
THEN
\[
\begin{align*}
C2 & \leftarrow 0; \\
\text{TEMP} & \leftarrow \cosine(ST(0)); \\
ST(0) & \leftarrow \sin(ST(0)); \\
\text{TOP} & \leftarrow \text{TOP} - 1; \\
ST(0) & \leftarrow \text{TEMP};
\end{align*}
\]
ELSE (* Source operand out of range *)
\[
C2 \leftarrow 1;
\]
FI;

FPU Flags Affected

- C1 Set to 0 if stack underflow occurred; set to 1 of stack overflow occurs.
- C2 Set to 1 if outside range \((-2^{63} < \text{source operand} < +2^{63})\); otherwise, set to 0.
- C0, C3 Undefined.

Floating-Point Exceptions

- #IS Stack underflow or overflow occurred.
- #IA Source operand is an SNaN value, \(\infty\), or unsupported format.
- #D Source operand is a denormal value.
- #U Result is too small for destination format.
- #P Value cannot be represented exactly in destination format.

Protected Mode Exceptions

- #NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- #MF If there is a pending x87 FPU exception.
- #UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FSQRT—Square Root

**Description**
Computes the square root of the source value in the ST(0) register and stores the result in ST(0).

The following table shows the results obtained when taking the square root of various classes of numbers, assuming that neither overflow nor underflow occurs.

**Table 3-47. FSQRT Results**

<table>
<thead>
<tr>
<th>SRC (ST(0))</th>
<th>DEST (ST(0))</th>
</tr>
</thead>
<tbody>
<tr>
<td>–∞</td>
<td>*</td>
</tr>
<tr>
<td>–F</td>
<td>*</td>
</tr>
<tr>
<td>–0</td>
<td>–0</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
</tr>
<tr>
<td>+F</td>
<td>+F</td>
</tr>
<tr>
<td>+∞</td>
<td>+∞</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**
F Means finite floating-point value.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

ST(0) ← SquareRoot(ST(0));

**FPU Flags Affected**

C1 Set to 0 if stack underflow occurred.
Set if result was rounded up; cleared otherwise.
C0, C2, C3 Undefined.

**Floating-Point Exceptions**

#IS Stack underflow occurred.
#IA Source operand is an SNaN value or unsupported format.
Source operand is a negative value (except for –0).

#D Source operand is a denormal value.

#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

Same exceptions as in protected mode.
## FST/FSTP—Store Floating Point Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /2</td>
<td>FST m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m32fp.</td>
</tr>
<tr>
<td>DD /2</td>
<td>FST m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m64fp.</td>
</tr>
<tr>
<td>DD D0+i</td>
<td>FST ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to ST(i).</td>
</tr>
<tr>
<td>D9 /3</td>
<td>FSTP m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m32fp and pop register stack.</td>
</tr>
<tr>
<td>DD /3</td>
<td>FSTP m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m64fp and pop register stack.</td>
</tr>
<tr>
<td>DB /7</td>
<td>FSTP m80fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to m80fp and pop register stack.</td>
</tr>
<tr>
<td>DD D8+i</td>
<td>FSTP ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Copy ST(0) to ST(i) and pop register stack.</td>
</tr>
</tbody>
</table>

### Description

The FST instruction copies the value in the ST(0) register to the destination operand, which can be a memory location or another register in the FPU register stack. When storing the value in memory, the value is converted to single-precision or double-precision floating-point format.

The FSTP instruction performs the same operation as the FST instruction and then pops the register stack. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The FSTP instruction can also store values in memory in double extended-precision floating-point format.

If the destination operand is a memory location, the operand specifies the address where the first byte of the destination value is to be stored. If the destination operand is a register, the operand specifies a register in the register stack relative to the top of the stack.

If the destination size is single-precision or double-precision, the significand of the value being stored is rounded to the width of the destination (according to the rounding mode specified by the RC field of the FPU control word), and the exponent is converted to the width and bias of the destination format. If the value being stored is too large for the destination format, a numeric overflow exception (#O) is generated and, if the exception is unmasked, no value is stored in the destination operand. If the value being stored is a denormal value, the denormal exception (#D) is not generated. This condition is simply signaled as a numeric underflow exception (#U) condition.

If the value being stored is ±0, ±∞, or a NaN, the least-significant bits of the significand and the exponent are truncated to fit the destination format. This operation preserves the value’s identity as a 0, ∞, or NaN.
If the destination operand is a non-empty register, the invalid-operation exception is not generated.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{DEST} \leftarrow \text{ST}(0);
\]

If \text{Instruction} = \text{FSTP}

\[
\text{THEN}
\]

PopRegisterStack;

\text{FI};

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred.
- Indicates rounding direction of if the floating-point inexact exception (\#P) is generated: 0 \leftarrow \text{not roundup}; 1 \leftarrow \text{roundup}.

- **C0, C2, C3** Undefined.

**Floating-Point Exceptions**

- **\#IS** Stack underflow occurred.
- **\#IA** Source operand is an SNaN value or unsupported format. Does not occur if the source operand is in double extended-precision floating-point format.
- **\#U** Result is too small for the destination format.
- **\#O** Result is too large for the destination format.
- **\#P** Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **\#GP(0)** If the destination is located in a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
- **\#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **\#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **\#PF(fault-code)** If a page fault occurs.
- **\#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **\#UD** If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**FSTCW/FNSTCW—Store x87 FPU Control Word**

**Description**
Stores the current value of the FPU control word at the specified destination in memory. The FSTCW instruction checks for and handles pending unmasked floating-point exceptions before storing the control word; the FNSTCW instruction does not.

The assembler issues two instructions for the FSTCW instruction (an FWAIT instruction followed by an FNSTCW instruction), and the processor executes each of these instructions in separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**
When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNSTCW instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled "No-Wait FPU Instructions Can Get FPU Interrupt in Window" in Appendix D of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a description of these circumstances. An FNSTCW instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

**Operation**

```
DEST ← FPUControlWord;
```

**FPU Flags Affected**
The C0, C1, C2, and C3 flags are undefined.

**Floating-Point Exceptions**
None.
Protected Mode Exceptions

#GP(0)  If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#UD  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

#UD  If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FSTENV/FNSTENV—Store x87 FPU Environment

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B D9 /6</td>
<td>FSTENV m14/28byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU environment to m14byte or m28byte after checking for pending unmasked floating-point exceptions. Then mask all floating-point exceptions.</td>
</tr>
<tr>
<td>D9 /6</td>
<td>FNSTENV* m14/28byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU environment to m14byte or m28byte without checking for pending unmasked floating-point exceptions. Then mask all floating-point exceptions.</td>
</tr>
</tbody>
</table>

NOTES:
* See IA-32 Architecture Compatibility section below.

Description

Saves the current FPU operating environment at the memory location specified with the destination operand, and then masks all floating-point exceptions. The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. Figures 8-9 through 8-12 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, show the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the current operand-size attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used.

The FSTENV instruction checks for and handles any pending unmasked floating-point exceptions before storing the FPU environment; the FNSTENV instruction does not. The saved image reflects the state of the FPU after all floating-point instructions preceding the FSTENV/FNSTENV instruction in the instruction stream have been executed.

These instructions are often used by exception handlers because they provide access to the FPU instruction and data pointers. The environment is typically saved in the stack. Masking all exceptions after saving the environment prevents floating-point exceptions from interrupting the exception handler.

The assembler issues two instructions for the FSTENV instruction (an FWAIT instruction followed by an FNSTENV instruction), and the processor executes each of these instructions separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
IA-32 Architecture Compatibility

When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNSTENV instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled "No-Wait FPU Instructions Can Get FPU Interrupt in Window" in Appendix D of the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for a description of these circumstances. An FNSTENV instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

Operation

\[
\begin{align*}
\text{DEST}[\text{FPUControlWord}] & \leftarrow \text{FPUControlWord;} \\
\text{DEST}[\text{FPUStatusWord}] & \leftarrow \text{FPUStatusWord;} \\
\text{DEST}[\text{FPUTagWord}] & \leftarrow \text{FPUTagWord;} \\
\text{DEST}[\text{FPUDataPointer}] & \leftarrow \text{FPUDataPointer;} \\
\text{DEST}[\text{FPUInstructionPointer}] & \leftarrow \text{FPUInstructionPointer;} \\
\text{DEST}[\text{FPULastInstructionOpcode}] & \leftarrow \text{FPULastInstructionOpcode;} \\
\end{align*}
\]

FPU Flags Affected

The C0, C1, C2, and C3 are undefined.

Floating-Point Exceptions

None.

Protected Mode Exceptions

- **#GP(0)** If the destination is located in a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#NM** CR0.E[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used.

Real-Address Mode Exceptions

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FSTSW/FNSTSW—Store x87 FPU Status Word

Description
Stores the current value of the x87 FPU status word in the destination location. The destination operand can be either a two-byte memory location or the AX register. The FSTSW instruction checks for and handles pending unmasked floating-point exceptions before storing the status word; the FNSTSW instruction does not.

The FNSTSW AX form of the instruction is used primarily in conditional branching (for instance, after an FPU comparison instruction or an FPREM, FPREM1, or FXAM instruction), where the direction of the branch depends on the state of the FPU condition code flags. (See the section titled "Branching and Conditional Moves on FPU Condition Codes" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.) This instruction can also be used to invoke exception handlers (by examining the exception flags) in environments that do not use interrupts. When the FNSTSW AX instruction is executed, the AX register is updated before the processor executes any further instructions. The status stored in the AX register is thus guaranteed to be from the completion of the prior FPU instruction.

The assembler issues two instructions for the FSTSW instruction (an FWAIT instruction followed by an FNSTSW instruction), and the processor executes each of these instructions separately. If an exception is generated for either of these instructions, the save EIP points to the instruction that caused the exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DD /7</td>
<td>FSTSW m2byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU status word at m2byte after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>9B DF E0</td>
<td>FSTSW AX</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU status word in AX register after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DD /7</td>
<td>FNSTSW m2byte</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU status word at m2byte without checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DF E0</td>
<td>FNSTSW AX</td>
<td>Valid</td>
<td>Valid</td>
<td>Store FPU status word in AX register without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

NOTES:
* See IA-32 Architecture Compatibility section below.
IA-32 Architecture Compatibility

When operating a Pentium or Intel486 processor in MS-DOS compatibility mode, it is possible (under unusual circumstances) for an FNSTSW instruction to be interrupted prior to being executed to handle a pending FPU exception. See the section titled "No-Wait FPU Instructions Can Get FPU Interrupt in Window" in Appendix D of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a description of these circumstances. An FNSTSW instruction cannot be interrupted in this way on a Pentium 4, Intel Xeon, or P6 family processor.

Operation

DEST ← FPUSstatusWord;

FPU Flags Affected

The C0, C1, C2, and C3 are undefined.

Floating-Point Exceptions

None.

Protected Mode Exceptions

- **#GP(0)**: If the destination is located in a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used.

Real-Address Mode Exceptions

- **#GP**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS**: If a memory operand effective address is outside the SS segment limit.
- **#NM**: CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
FSUB/FSUBP/FISUB—Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compata/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /4</td>
<td>FSUB m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract m32fp from ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC /4</td>
<td>FSUB m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract m64fp from ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>D8 E0+i</td>
<td>FSUB ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(i) from ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DC E8+i</td>
<td>FSUB ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from ST(i) and store result in ST(i).</td>
</tr>
<tr>
<td>DE E8+i</td>
<td>FSUBP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from ST(i), store result in ST(i), and pop register stack.</td>
</tr>
<tr>
<td>DE E9</td>
<td>FSUBP</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from ST(1), store result in ST(1), and pop register stack.</td>
</tr>
<tr>
<td>DA /4</td>
<td>FISUB m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract m32int from ST(0) and store result in ST(0).</td>
</tr>
<tr>
<td>DE /4</td>
<td>FISUB m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract m16int from ST(0) and store result in ST(0).</td>
</tr>
</tbody>
</table>

Description

Subtracts the source operand from the destination operand and stores the difference in the destination location. The destination operand is always an FPU data register; the source operand can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format or in word or doubleword integer format.

The no-operand version of the instruction subtracts the contents of the ST(0) register from the ST(1) register and stores the result in ST(1). The one-operand version subtracts the contents of a memory location (either a floating-point or an integer value) from the contents of the ST(0) register and stores the result in ST(0). The two-operand version, subtracts the contents of the ST(0) register from the ST(i) register or vice versa.

The FSUBP instructions perform the additional operation of popping the FPU register stack following the subtraction. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point subtract instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FSUB rather than FSUBP.
INSTRUCTION SET REFERENCE, A-L

The FISUB instructions convert an integer source operand to double extended-precision floating-point format before performing the subtraction.

Table 3-48 shows the results obtained when subtracting various classes of numbers from one another, assuming that neither overflow nor underflow occurs. Here, the SRC value is subtracted from the DEST value (DEST − SRC = result).

When the difference between two operands of like sign is 0, the result is +0, except for the round toward −∞ mode, in which case the result is −0. This instruction also guarantees that +0 − (−0) = +0, and that −0 − (+0) = −0. When the source operand is an integer 0, it is treated as a +0.

When one operand is −∞, the result is −∞ of the expected sign. If both operands are −∞ of the same sign, an invalid-operation exception is generated.

Table 3-48. FSUB/FSUBP/FISUB Results

<table>
<thead>
<tr>
<th>DEST</th>
<th>SRC</th>
<th>−∞</th>
<th>−F or −I</th>
<th>−0</th>
<th>+0</th>
<th>+F or +I</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>+∞</td>
<td>±F or ±0</td>
<td>DEST</td>
<td>DEST</td>
<td>−F</td>
<td>−∞</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>−0</td>
<td>+∞</td>
<td>−SRC</td>
<td>±0</td>
<td>−0</td>
<td>−SRC</td>
<td>−∞</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+0</td>
<td>+∞</td>
<td>−SRC</td>
<td>±0</td>
<td>−SRC</td>
<td>−∞</td>
<td>NaN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>+F</td>
<td>+∞</td>
<td>+F</td>
<td>DEST</td>
<td>DEST</td>
<td>±F or ±0</td>
<td>−∞</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
F Means finite floating-point value.
I Means integer.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
IF Instruction = FISUB
THEN
  DEST ← DEST − ConvertToDoubleExtendedPrecisionFP(SRC);
ELSE (* Source operand is floating-point value *)
  DEST ← DEST − SRC;
FI;
IF Instruction = FSUBP
    THEN
        PopRegisterStack;
FI;

**FPU Flags Affected**

C1          Set to 0 if stack underflow occurred.
            Set if result was rounded up; cleared otherwise.
C0, C2, C3   Undefined.

**Floating-Point Exceptions**

#IS          Stack underflow occurred.
#IA          Operand is an SNaN value or unsupported format.
            Operands are infinities of like sign.
#D           Source operand is a denormal value.
#U           Result is too small for destination format.
#O           Result is too large for destination format.
#P           Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#GP(0)       If a memory operand effective address is outside the CS, DS,
              ES, FS, or GS segment limit.
              If the DS, ES, FS, or GS register is used to access memory and it
              contains a NULL segment selector.
#SS(0)       If a memory operand effective address is outside the SS
              segment limit.
#NM          CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0)       If alignment checking is enabled and an unaligned memory
              reference is made while the current privilege level is 3.
#UD          If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP          If a memory operand effective address is outside the CS, DS,
              ES, FS, or GS segment limit.
#SS          If a memory operand effective address is outside the SS
              segment limit.
#NM          CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#UD          If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, A-L

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**FSUBR/FSUBRP/FISUBR—Reverse Subtract**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /5</td>
<td>FSUBR m32fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from m32fp and store result in ST(0).</td>
</tr>
<tr>
<td>DC /5</td>
<td>FSUBR m64fp</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from m64fp and store result in ST(0).</td>
</tr>
<tr>
<td>D8 E8+i</td>
<td>FSUBR ST(0), ST(i)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from ST(i) and store result in ST(0).</td>
</tr>
<tr>
<td>DC E0+i</td>
<td>FSUBR ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(i) from ST(0) and store result in ST(i).</td>
</tr>
<tr>
<td>DE E0+i</td>
<td>FSUBRP ST(i), ST(0)</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(i) from ST(0), store result in ST(i), and pop register stack.</td>
</tr>
<tr>
<td>DE E1</td>
<td>FSUBRP</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(1) from ST(0), store result in ST(1), and pop register stack.</td>
</tr>
<tr>
<td>DA /5</td>
<td>FISUBR m32int</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from m32int and store result in ST(0).</td>
</tr>
<tr>
<td>DE /5</td>
<td>FISUBR m16int</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract ST(0) from m16int and store result in ST(0).</td>
</tr>
</tbody>
</table>

**Description**

Subtracts the destination operand from the source operand and stores the difference in the destination location. The destination operand is always an FPU register; the source operand can be a register or a memory location. Source operands in memory can be in single-precision or double-precision floating-point format or in word or doubleword integer format.

These instructions perform the reverse operations of the FSUB, FSUBP, and FISUB instructions. They are provided to support more efficient coding.

The no-operand version of the instruction subtracts the contents of the ST(1) register from the ST(0) register and stores the result in ST(1). The one-operand version subtracts the contents of the ST(0) register from the contents of a memory location (either a floating-point or an integer value) and stores the result in ST(0). The two-operand version, subtracts the contents of the ST(i) register from the ST(0) register or vice versa.

The FSUBRP instructions perform the additional operation of popping the FPU register stack following the subtraction. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point reverse subtract instructions always results in
the register stack being popped. In some assemblers, the mnemonic for this instruction is FSUBR rather than FSUBRP.

The FISUBR instructions convert an integer source operand to double extended-precision floating-point format before performing the subtraction.

The following table shows the results obtained when subtracting various classes of numbers from one another, assuming that neither overflow nor underflow occurs. Here, the DEST value is subtracted from the SRC value (\( \text{SRC} - \text{DEST} = \text{result} \)).

When the difference between two operands of like sign is 0, the result is +0, except for the round toward \(-\infty\) mode, in which case the result is -0. This instruction also guarantees that \(+0 - (-0) = +0\), and that \(-0 - (+0) = -0\). When the source operand is an integer 0, it is treated as a +0.

When one operand is \(\infty\), the result is \(\infty\) of the expected sign. If both operands are \(\infty\) of the same sign, an invalid-operation exception is generated.

**Table 3-49. FSUBR/FSUBRP/FISUBR Results**

<table>
<thead>
<tr>
<th>DEST</th>
<th>-(\infty)</th>
<th>-F or (-I)</th>
<th>-0</th>
<th>+0</th>
<th>+F or +I</th>
<th>+(\infty)</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>-(\infty)</td>
<td>*</td>
<td>+(\infty)</td>
<td>+(\infty)</td>
<td>+(\infty)</td>
<td>+(\infty)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>- F</td>
<td>-(\infty)</td>
<td>(\pm F or \pm 0)</td>
<td>-DEST</td>
<td>-DEST</td>
<td>+ F</td>
<td>+ (\infty)</td>
<td>NaN</td>
</tr>
<tr>
<td>- 0</td>
<td>-(\infty)</td>
<td>SRC</td>
<td>(\pm 0)</td>
<td>+ 0</td>
<td>SRC</td>
<td>+ (\infty)</td>
<td>NaN</td>
</tr>
<tr>
<td>+ 0</td>
<td>-(\infty)</td>
<td>SRC</td>
<td>- 0</td>
<td>(\pm 0)</td>
<td>SRC</td>
<td>+ (\infty)</td>
<td>NaN</td>
</tr>
<tr>
<td>+ F</td>
<td>-(\infty)</td>
<td>- F</td>
<td>-DEST</td>
<td>-DEST</td>
<td>(\pm F or \pm 0)</td>
<td>+ (\infty)</td>
<td>NaN</td>
</tr>
<tr>
<td>+ (\infty)</td>
<td>-(\infty)</td>
<td>- F</td>
<td>-DEST</td>
<td>-DEST</td>
<td>(\pm F or \pm 0)</td>
<td>+ (\infty)</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.
I Means integer.
* Indicates floating-point invalid-arithmetic-operand (#IA) exception.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

IF Instruction = FISUBR
THEN
  DEST ← ConvertToDoubleExtendedPrecisionFP(SRC) - DEST;
ELSE (* Source operand is floating-point value *)
  DEST ← SRC - DEST; Fi;
IF Instruction = FSUBRP
THEN
    PopRegisterStack; FI;

**FPU Flags Affected**

C1 \hspace{1em} Set to 0 if stack underflow occurred. 
\hspace{1em} Set if result was rounded up; cleared otherwise. 
C0, C2, C3 \hspace{1em} Undefined.

**Floating-Point Exceptions**

#IS \hspace{1em} Stack underflow occurred. 
#IA \hspace{1em} Operand is an SNaN value or unsupported format. 
\hspace{1em} Operands are infinities of like sign. 
#D \hspace{1em} Source operand is a denormal value. 
#U \hspace{1em} Result is too small for destination format. 
#O \hspace{1em} Result is too large for destination format. 
#P \hspace{1em} Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#GP(0) \hspace{1em} If a memory operand effective address is outside the CS, DS, 
\hspace{1em} ES, FS, or GS segment limit. 
\hspace{1em} If the DS, ES, FS, or GS register is used to access memory and it 
\hspace{1em} contains a NULL segment selector. 
#SS(0) \hspace{1em} If a memory operand effective address is outside the SS 
\hspace{1em} segment limit. 
#NM \hspace{1em} CR0.EM[bit 2] or CR0.TS[bit 3] = 1. 
#PF(fault-code) \hspace{1em} If a page fault occurs. 
#AC(0) \hspace{1em} If alignment checking is enabled and an unaligned memory 
\hspace{1em} reference is made while the current privilege level is 3. 
#UD \hspace{1em} If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP \hspace{1em} If a memory operand effective address is outside the CS, DS, 
\hspace{1em} ES, FS, or GS segment limit. 
#SS \hspace{1em} If a memory operand effective address is outside the SS 
\hspace{1em} segment limit. 
#NM \hspace{1em} CR0.EM[bit 2] or CR0.TS[bit 3] = 1. 
#UD \hspace{1em} If the LOCK prefix is used.
Virtual-8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM     CR0.E[bit 2] or CR0.TS[bit 3] = 1.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
#UD     If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#NM     CR0.E[bit 2] or CR0.TS[bit 3] = 1.
#MF     If there is a pending x87 FPU exception.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD     If the LOCK prefix is used.
**FTST—TEST**

**Description**

Compares the value in the ST(0) register with 0.0 and sets the condition code flags C0, C2, and C3 in the FPU status word according to the results (see table below).

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; 0.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; 0.0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = 0.0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

This instruction performs an “unordered comparison.” An unordered comparison also checks the class of the numbers being compared (see “FXAM—Examine ModR/M” in this chapter). If the value in register ST(0) is a NaN or is in an undefined format, the condition flags are set to “unordered” and the invalid operation exception is generated.

The sign of zero is ignored, so that (– 0.0 ← +0.0).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

CASE (relation of operands) OF

   Not comparable: C3, C2, C0 ← 111;
   ST(0) > 0.0: C3, C2, C0 ← 000;
   ST(0) < 0.0: C3, C2, C0 ← 001;
   ST(0) = 0.0: C3, C2, C0 ← 100;

ESAC;

**FPU Flags Affected**

C1 Set to 0.
C0, C2, C3 See Table 3-50.

**Floating-Point Exceptions**

#IS Stack underflow occurred.

---

**Table 3-50. FTST Results**

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; 0.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; 0.0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = 0.0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-L

#IA The source operand is a NaN value or is in an unsupported format.
#D The source operand is a denormal value.

Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FUCOM/FUCOMP/FUCOMPP—Unordered Compare Floating Point Values

Description
Performs an unordered comparison of the contents of register ST(0) and ST(i) and sets condition code flags C0, C2, and C3 in the FPU status word according to the results (see the table below). If no operand is specified, the contents of registers ST(0) and ST(1) are compared. The sign of zero is ignored, so that –0.0 is equal to +0.0.

An unordered comparison checks the class of the numbers being compared (see “FXAM—Examine ModR/M” in this chapter). The FUCOM/FUCOMP/FUCOMPP instructions perform the same operations as the FCOM/FCOMP/FCOMPP instructions. The only difference is that the FUCOM/FUCOMP/FUCOMPP instructions raise the invalid-arithmetic-operand (#IA) only when either or both operands are an SNaN or are in an unsupported format; QNaNs cause the condition code flags to be set to unordered, but do not cause an exception to be generated. The FCOM/FCOMP/FCOMPP instructions raise an invalid-operation exception when either or both of the operands are a NaN value of any kind or are in an unsupported format. As with the FCOM/FCOMP/FCOMPP instructions, if the operation results in an invalid-arithmetic-operand exception being raised, the condition code flags are set only if the exception is masked.

Table 3-51. FUCOM/FUCOMP/FUCOMPP Results

<table>
<thead>
<tr>
<th>Comparison Results*</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST0 &gt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST0 &lt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST0 = ST(i)</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTES:
* Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.

FUCOM/FUCOMP/FUCOMPP—Unordered Compare Floating Point Values
The FUCOMP instruction pops the register stack following the comparison operation and the FUCOMPP instruction pops the register stack twice following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

CASE (relation of operands) OF

- ST > SRC: C3, C2, C0 ← 000;
- ST < SRC: C3, C2, C0 ← 001;
- ST = SRC: C3, C2, C0 ← 100;

ESAC;

IF ST(0) or SRC = QNaN, but not SNaN or unsupported format

THEN

C3, C2, C0 ← 111;

ELSE (* ST(0) or SRC is SNaN or unsupported format *)

#IA;

IF FPUControlWord.IM = 1

THEN

C3, C2, C0 ← 111;

FI;

FI;

IF Instruction = FUCOMP

THEN

PopRegisterStack;

FI;

IF Instruction = FUCOMPP

THEN

PopRegisterStack;

FI;

**FPU Flags Affected**

- C1 Set to 0 if stack underflow occurred.
- C0, C2, C3 See Table 3-51.

**Floating-Point Exceptions**

- #IS Stack underflow occurred.
FUCOM/FUCOMP/FUCOMPP—Unordered Compare Floating Point Values

INSTRUCTION SET REFERENCE, A-L

#IA One or both operands are SNaN values or have unsupported formats. Detection of a QNaN value in and of itself does not raise an invalid-operand exception.

#D One or both operands are denormal values.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

Same exceptions as in protected mode.
FXAM—Examine ModR/M

Description
Examines the contents of the ST(0) register and sets the condition code flags C0, C2, and C3 in the FPU status word to indicate the class of value or number in the register (see the table below).

<table>
<thead>
<tr>
<th>Class</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unsupported</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>NaN</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Normal finite number</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Infinity</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Zero</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Empty</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Denormal number</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The C1 flag is set to the sign of the value in ST(0), regardless of whether the register is empty or full.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation
C1 ← sign bit of ST; (* 0 for positive, 1 for negative *)

CASE (class of value or number in ST(0)) OF
  Unsupported: C3, C2, C0 ← 000;
  NaN: C3, C2, C0 ← 001;
  Normal: C3, C2, C0 ← 010;
  Infinity: C3, C2, C0 ← 011;
  Zero: C3, C2, C0 ← 100;
  Empty: C3, C2, C0 ← 101;
  Denormal: C3, C2, C0 ← 110;
ESAC;
FPU Flags Affected
C1  Sign of value in ST(0).
C0, C2, C3  See Table 3-52.

Floating-Point Exceptions
None.

Protected Mode Exceptions
#NM  CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF  If there is a pending x87 FPU exception.
#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
FXCH—Exchange Register Contents

Description
Exchanges the contents of registers ST(0) and ST(i). If no source operand is specified, the contents of ST(0) and ST(1) are exchanged.

This instruction provides a simple means of moving values in the FPU register stack to the top of the stack [ST(0)], so that they can be operated on by those floating-point instructions that can only operate on values in ST(0). For example, the following instruction sequence takes the square root of the third register from the top of the register stack:

```plaintext
FXCH ST(3);
FSQRT;
FXCH ST(3);
```

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

```plaintext
IF (Number-of-operands) is 1 THEN
    temp ← ST(0);
    ST(0) ← SRC;
    SRC ← temp;
ELSE
    temp ← ST(0);
    ST(0) ← ST(1);
    ST(1) ← temp;
FI;
```

FPU Flags Affected

C1 Set to 0 if stack underflow occurred; otherwise, set to 1.
C0, C2, C3 Undefined.

Floating-Point Exceptions

#IS Stack underflow occurred.
Protected Mode Exceptions
#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.


**FXRSTOR—Restore x87 FPU, MMX, XMM, and MXCSR State**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /1</td>
<td>FXRSTOR</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Restore the x87 FPU, MMX, XMM, and MXCSR register state from m512byte.</td>
</tr>
<tr>
<td>REX.W+ 0F AE /1</td>
<td>FXRSTOR64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Restore the x87 FPU, MMX, XMM, and MXCSR register state from m512byte.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Reloads the x87 FPU, MMX technology, XMM, and MXCSR registers from the 512-byte memory image specified in the source operand. This data should have been written to memory previously using the FXSAVE instruction, and in the same format as required by the operating modes. The first byte of the data should be located on a 16-byte boundary. There are three distinct layouts of the FXSAVE state map: one for legacy and compatibility mode, a second format for 64-bit mode FXSAVE/FXRSTOR with REX.W=0, and the third format is for 64-bit mode with FXSAVE64/FXRSTOR64. Table 3-53 shows the layout of the legacy/compatibility mode state information in memory and describes the fields in the memory image for the FXRSTOR and FXSAVE instructions. Table 3-56 shows the layout of the 64-bit mode state information when REX.W is set (FXSAVE64/FXRSTOR64). Table 3-57 shows the layout of the 64-bit mode state information when REX.W is clear (FXSAVE/FXRSTOR).

The state image referenced with an FXRSTOR instruction must have been saved using an FXSAVE instruction or be in the same format as required by Table 3-53, Table 3-56, or Table 3-57. Referencing a state image saved with an FSAVE, FNSAVE instruction or incompatible field layout will result in an incorrect state restoration.

The FXRSTOR instruction does not flush pending x87 FPU exceptions. To check and raise exceptions when loading x87 FPU state information with the FXRSTOR instruction, use an FWAIT instruction after the FXRSTOR instruction.

If the OESFXSR bit in control register CR4 is not set, the FXRSTOR instruction may not restore the states of the XMM and MXCSR registers. This behavior is implementation dependent.

If the MXCSR state contains an unmasked exception with a corresponding status flag also set, loading the register with the FXRSTOR instruction will not result in a SIMD floating-point error condition being generated. Only the next occurrence of this unmasked exception will result in the exception being generated.
Bits 16 through 32 of the MXCSR register are defined as reserved and should be set to 0. Attempting to write a 1 in any of these bits from the saved state image will result in a general protection exception (#GP) being generated.

Bytes 464:511 of an FXSAVE image are available for software use. FXRSTOR ignores the content of bytes 464:511 in an FXSAVE state image.

**Operation**

\[(x87 \text{ FPU, MMX, XMM7-XMM0, MXCSR}) \leftarrow \text{Load}(\text{SRC})\]

**x87 FPU and SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.

If a memory operand is not aligned on a 16-byte boundary, regardless of segment. (See alignment check exception [#AC] below.)

For an attempt to set reserved bits in MXCSR.

#SS(0) For an illegal address in the SS segment.

#PF(fault-code) For a page fault.

#NM If CR0.TS[bit 3] = 1.

If CR0.EM[bit 2] = 1.

#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.

If instruction is preceded by a LOCK prefix.

#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).

#UD If the LOCK prefix is used.
Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
   If any part of the operand lies outside the effective address space from 0 to FFFFH.
   For an attempt to set reserved bits in MXCSR.
#NM If CR0.TS[bit 3] = 1.
   If CR0.EM[bit 2] = 1.
#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
   If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.
#AC For unaligned memory reference.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
   If memory operand is not aligned on a 16-byte boundary, regardless of segment.
   For an attempt to set reserved bits in MXCSR.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
   If CR0.EM[bit 2] = 1.
#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
   If instruction is preceded by a LOCK prefix.
#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation.
FXRSTOR—Restore x87 FPU, MMX, XMM, and MXCSR State
FXSAVE—Save x87 FPU, MMX Technology, and SSE State

**Opcode** | **Instruction** | **Op/En** | **64-Bit Mode** | **Compat/Leg Mode** | **Description**
--- | --- | --- | --- | --- | ---
0F AE /0 | FXSAVE | M | Valid | Valid | Save the x87 FPU, MMX, XMM, and MXCSR register state to m512byte.

REX.W+ 0F AE /0 | FXSAVE64 | M | Valid | N.E. | Save the x87 FPU, MMX, XMM, and MXCSR register state to m512byte.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM/r/m (w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Saves the current state of the x87 FPU, MMX technology, XMM, and MXCSR registers to a 512-byte memory location specified in the destination operand. The content layout of the 512 byte region depends on whether the processor is operating in non-64-bit operating modes or 64-bit sub-mode of IA-32e mode.

Bytes 464:511 are available to software use. The processor does not write to bytes 464:511 of an FXSAVE area.

The operation of FXSAVE in non-64-bit modes is described first.

**Non-64-Bit Mode Operation**

Table 3-53 shows the layout of the state information in memory when the processor is operating in legacy modes.

**Table 3-53. Non-64-bit-Mode Layout of FXSAVE and FXRSTOR Memory Region**

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rsvrd</td>
<td>CS</td>
<td>FPU IP</td>
<td>FOP</td>
<td>Rsrvd</td>
<td>FTW</td>
<td>FSW</td>
<td>FCW</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MXCSR _MASK</td>
<td>MXCSR</td>
<td>Rsvrd</td>
<td>DS</td>
<td>FPU DP</td>
<td>16</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST0/MM0</td>
<td>32</td>
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<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST1/MM1</td>
<td>48</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST2/MM2</td>
<td>64</td>
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<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST3/MM3</td>
<td>80</td>
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</tr>
<tr>
<td>Reserved</td>
<td>ST4/MM4</td>
<td>96</td>
<td></td>
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</tbody>
</table>
The destination operand contains the first byte of the memory image, and it must be aligned on a 16-byte boundary. A misaligned destination operand will result in a general-protection (#GP) exception being generated (or in some cases, an alignment check exception [#AC]).
The FXSAVE instruction is used when an operating system needs to perform a context switch or when an exception handler needs to save and examine the current state of the x87 FPU, MMX technology, and/or XMM and MXCSR registers.

The fields in Table 3-53 are defined in Table 3-54.

### Table 3-54: Field Definitions

<table>
<thead>
<tr>
<th>Field</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>FCW</td>
<td>x87 FPU Control Word (16 bits). See Figure 8-6 in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for the layout of the x87 FPU control word.</td>
</tr>
<tr>
<td>FSW</td>
<td>x87 FPU Status Word (16 bits). See Figure 8-4 in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for the layout of the x87 FPU status word.</td>
</tr>
<tr>
<td>Abridged FTW</td>
<td>x87 FPU Tag Word (8 bits). The tag information saved here is abridged, as described in the following paragraphs.</td>
</tr>
<tr>
<td>FOP</td>
<td>x87 FPU Opcode (16 bits). The lower 11 bits of this field contain the opcode, upper 5 bits are reserved. See Figure 8-8 in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for the layout of the x87 FPU opcode field.</td>
</tr>
<tr>
<td>FPU IP</td>
<td>x87 FPU Instruction Pointer Offset (32 bits). The contents of this field differ depending on the current addressing mode (32-bit or 16-bit) of the processor when the FXSAVE instruction was executed: 32-bit mode — 32-bit IP offset. 16-bit mode — low 16 bits are IP offset; high 16 bits are reserved. See “x87 FPU Instruction and Operand (Data) Pointers” in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for a description of the x87 FPU instruction pointer.</td>
</tr>
<tr>
<td>CS</td>
<td>x87 FPU Instruction Pointer Selector (16 bits).</td>
</tr>
<tr>
<td>FPU DP</td>
<td>x87 FPU Instruction Operand (Data) Pointer Offset (32 bits). The contents of this field differ depending on the current addressing mode (32-bit or 16-bit) of the processor when the FXSAVE instruction was executed: 32-bit mode — 32-bit DP offset. 16-bit mode — low 16 bits are DP offset; high 16 bits are reserved. See “x87 FPU Instruction and Operand (Data) Pointers” in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1, for a description of the x87 FPU operand pointer.</td>
</tr>
<tr>
<td>DS</td>
<td>x87 FPU Instruction Operand (Data) Pointer Selector (16 bits).</td>
</tr>
</tbody>
</table>
**Table 3-54. Field Definitions (Contd.)**

<table>
<thead>
<tr>
<th>Field</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>MXCSR</td>
<td>MXCSR Register State (32 bits). See Figure 10-3 in the <em>Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1</em>, for the layout of the MXCSR register. If the OSFXSR bit in control register CR4 is not set, the FXSAVE instruction may not save this register. This behavior is implementation dependent.</td>
</tr>
<tr>
<td>MXCSR_MASK</td>
<td>MXCSR_MASK (32 bits). This mask can be used to adjust values written to the MXCSR register, ensuring that reserved bits are set to 0. Set the mask bits and flags in MXCSR to the mode of operation desired for SSE and SSE2 SIMD floating-point instructions. See “Guidelines for Writing to the MXCSR Register” in Chapter 11 of the <em>Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1</em>, for instructions on how to determine and use the MXCSR_MASK value.</td>
</tr>
<tr>
<td>ST0/MM0 through ST7/MM7</td>
<td>x87 FPU or MMX technology registers. These 80-bit fields contain the x87 FPU data registers or the MMX technology registers, depending on the state of the processor prior to the execution of the FXSAVE instruction. If the processor had been executing x87 FPU instruction prior to the FXSAVE instruction, the x87 FPU data registers are saved; if it had been executing MMX instructions (or SSE or SSE2 instructions that operated on the MMX technology registers), the MMX technology registers are saved. When the MMX technology registers are saved, the high 16 bits of the field are reserved.</td>
</tr>
<tr>
<td>XMM0 through XMM7</td>
<td>XMM registers (128 bits per field). If the OSFXSR bit in control register CR4 is not set, the FXSAVE instruction may not save these registers. This behavior is implementation dependent.</td>
</tr>
</tbody>
</table>

The FXSAVE instruction saves an abridged version of the x87 FPU tag word in the FTW field (unlike the FSAVE instruction, which saves the complete tag word). The tag information is saved in physical register order (R0 through R7), rather than in top-of-stack (TOS) order. With the FXSAVE instruction, however, only a single bit (1 for valid or 0 for empty) is saved for each tag. For example, assume that the tag word is currently set as follows:

```
R7  R6  R5  R4  R3  R2  R1  R0
11  xx  xx  xx  11  11  11  11
```

Here, 11B indicates empty stack elements and “xx” indicates valid (00B), zero (01B), or special (10B).

For this example, the FXSAVE instruction saves only the following 8 bits of information:

```
R7  R6  R5  R4  R3  R2  R1  R0
0  1  1  1  0  0  0  0
```
INSTRUCTION SET REFERENCE, A-L

Here, a 1 is saved for any valid, zero, or special tag, and a 0 is saved for any empty tag.

The operation of the FXSAVE instruction differs from that of the FSAVE instruction, the as follows:

- FXSAVE instruction does not check for pending unmasked floating-point exceptions. (The FXSAVE operation in this regard is similar to the operation of the FNSAVE instruction).

- After the FXSAVE instruction has saved the state of the x87 FPU, MMX technology, XMM, and MXCSR registers, the processor retains the contents of the registers. Because of this behavior, the FXSAVE instruction cannot be used by an application program to pass a “clean” x87 FPU state to a procedure, since it retains the current state. To clean the x87 FPU state, an application must explicitly execute an FINIT instruction after an FXSAVE instruction to reinitialize the x87 FPU state.

- The format of the memory image saved with the FXSAVE instruction is the same regardless of the current addressing mode (32-bit or 16-bit) and operating mode (protected, real address, or system management). This behavior differs from the FSAVE instructions, where the memory image format is different depending on the addressing mode and operating mode. Because of the different image formats, the memory image saved with the FXSAVE instruction cannot be restored correctly with the FRSTOR instruction, and likewise the state saved with the FSAVE instruction cannot be restored correctly with the FXRSTOR instruction.

The FSAVE format for FTW can be recreated from the FTW valid bits and the stored 80-bit FP data (assuming the stored data was not the contents of MMX technology registers) using Table 3-55.

Table 3-55. Recreating FSAVE Format

<table>
<thead>
<tr>
<th>Exponent all 1’s</th>
<th>Exponent all 0’s</th>
<th>Fraction all 0’s</th>
<th>J and M bits</th>
<th>FTW valid bit</th>
<th>x87 FTW</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1x</td>
<td>1</td>
<td>Valid 00</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>00</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>Valid 00</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0x</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1x</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>00</td>
<td>1</td>
<td>Zero 01</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1x</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1x</td>
<td>1</td>
<td>Special 10</td>
</tr>
</tbody>
</table>
The J-bit is defined to be the 1-bit binary integer to the left of the decimal place in the significand. The M-bit is defined to be the most significant bit of the fractional portion of the significand (i.e., the bit immediately to the right of the decimal place).

When the M-bit is the most significant bit of the fractional portion of the significand, it must be 0 if the fraction is all 0’s.

**IA-32e Mode Operation**

In compatibility sub-mode of IA-32e mode, legacy SSE registers, XMM0 through XMM7, are saved according to the legacy FXSAVE map. In 64-bit mode, all of the SSE registers, XMM0 through XMM15, are saved. Additionally, there are two different layouts of the FXSAVE map in 64-bit mode, corresponding to FXSAVE64 (which requires REX.W=1) and FXSAVE (REX.W=0). In the FXSAVE64 map (Table 3-56), the FPU IP and FPU DP pointers are 64-bit wide. In the FXSAVE map for 64-bit mode (Table 3-57), the FPU IP and FPU DP pointers are 32-bits.

### Table 3-55. Recreating FSAVE Format (Contd.)

<table>
<thead>
<tr>
<th>Exponent all 1’s</th>
<th>Exponent all 0’s</th>
<th>Fraction all 0’s</th>
<th>J and M bits</th>
<th>FTW valid bit</th>
<th>x87 FTW</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>00</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>Special 10</td>
</tr>
<tr>
<td>For all legal combinations above.</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Empty 11</td>
</tr>
</tbody>
</table>

The J-bit is defined to be the 1-bit binary integer to the left of the decimal place in the significand. The M-bit is defined to be the most significant bit of the fractional portion of the significand (i.e., the bit immediately to the right of the decimal place).

When the M-bit is the most significant bit of the fractional portion of the significand, it must be 0 if the fraction is all 0’s.

### Table 3-56. Layout of the 64-bit-mode FXSAVE64 Map (requires REX.W = 1)

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPU IP</td>
<td>FOP</td>
<td>Reserved</td>
<td>FTW</td>
<td>FSW</td>
<td>FCW</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MXCSR_MASK</th>
<th>MXCSR</th>
<th>FPU DP</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>ST0/MM0</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST1/MM1</td>
<td>48</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST2/MM2</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST3/MM3</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST4/MM4</td>
<td>96</td>
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</tr>
<tr>
<td>Reserved</td>
<td>ST5/MM5</td>
<td>112</td>
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</tr>
<tr>
<td>Reserved</td>
<td>ST6/MM6</td>
<td>128</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>ST7/MM7</td>
<td>144</td>
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<tr>
<td>XMM1</td>
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</tbody>
</table>
Table 3-56. Layout of the 64-bit-mode FXSAVE64 Map (requires REX.W = 1) (Contd.)

<table>
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<th>10</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
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<tr>
<td>XMM10</td>
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<tr>
<td>XMM11</td>
<td>336</td>
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Table 3-57. Layout of the 64-bit-mode FXSAVE Map (REX.W = 0)

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Table 3-57. Layout of the 64-bit-mode FXSAVE Map (REX.W = 0) (Contd.) (Contd.)

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Operation

IF 64-Bit Mode
THEN
  IF REX.W = 1
  THEN

FXSAVE—Save x87 FPU, MMX Technology, and SSE State
DEST ← Save64BitPromotedFxsave(x87 FPU, MMX, XMM7-XMM0, MXCSR);
ELSE
    DEST ← Save64BitDefaultFxsave(x87 FPU, MMX, XMM7-XMM0, MXCSR);
FI;
ELSE
    DEST ← SaveLegacyFxsave(x87 FPU, MMX, XMM7-XMM0, MXCSR);
FI;

**Protected Mode Exceptions**

- **#GP(0)** For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
  
  If a memory operand is not aligned on a 16-byte boundary, regardless of segment. (See the description of the alignment check exception [#AC] below.)
  
- **#SS(0)** For an illegal address in the SS segment.
  
- **#PF(fault-code)** For a page fault.
  
- **#NM** If CR0.TS[bit 3] = 1.
  
  If CR0.EM[bit 2] = 1.
  
- **#UD** If CPUID.01H:EDX.FXSR[bit 24] = 0.
  
- **#UD** If the LOCK prefix is used.
  
- **#AC** If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).

**Real-Address Mode Exceptions**

- **#GP** If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
  
  If any part of the operand lies outside the effective address space from 0 to FFFFH.
  
- **#NM** If CR0.TS[bit 3] = 1.
  
  If CR0.EM[bit 2] = 1.
#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
    If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

Same exceptions as in real address mode.

#PF(fault-code) For a page fault.
#AC For unaligned memory reference.
#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
    If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#PF(fault-code) For a page fault.
#NM If CR0.TS[bit 3] = 1.
    If CR0.EM[bit 2] = 1.
#UD If CPUID.01H:EDX.FXSR[bit 24] = 0.
    If the LOCK prefix is used.
#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).

**Implementation Note**

The order in which the processor signals general-protection (#GP) and page-fault (#PF) exceptions when they both occur on an instruction boundary is given in Table 5-2 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*. This order vary for FXSAVE for different processor implementations.
**FXTRACT—Extract Exponent and Significand**

<table>
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<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compait/ Leg Mode</th>
<th>Description</th>
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<tr>
<td>D9 F4</td>
<td>FXTRACT</td>
<td>Valid</td>
<td>Valid</td>
<td>Separate value in ST(0) into exponent and significand, store exponent in ST(0), and push the significand onto the register stack.</td>
</tr>
</tbody>
</table>

**Description**

Separates the source value in the ST(0) register into its exponent and significand, stores the exponent in ST(0), and pushes the significand onto the register stack. Following this operation, the new top-of-stack register ST(0) contains the value of the original significand expressed as a floating-point value. The sign and significand of this value are the same as those found in the source operand, and the exponent is 3FFFH (biased value for a true exponent of zero). The ST(1) register contains the value of the original operand's true (unbiased) exponent expressed as a floating-point value. (The operation performed by this instruction is a superset of the IEEE-recommended \( \log_b(x) \) function.)

This instruction and the F2XM1 instruction are useful for performing power and range scaling operations. The FXTRACT instruction is also useful for converting numbers in double extended-precision floating-point format to decimal representations (e.g., for printing or displaying).

If the floating-point zero-divide exception (#Z) is masked and the source operand is zero, an exponent value of \(-\infty\) is stored in register ST(1) and 0 with the sign of the source operand is stored in register ST(0).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\begin{align*}
\text{TEMP} & \leftarrow \text{Significand(ST(0))}; \\
\text{ST}(0) & \leftarrow \text{Exponent(ST(0))}; \\
\text{TOP} & \leftarrow \text{TOP} - 1; \\
\text{ST}(0) & \leftarrow \text{TEMP};
\end{align*}
\]

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred; set to 1 if stack overflow occurred.
- **C0, C2, C3** Undefined.

**Floating-Point Exceptions**

- **#IS** Stack underflow or overflow occurred.
#IA Source operand is an SNaN value or unsupported format.
#Z ST(0) operand is ±0.
#D Source operand is a denormal value.

Protected Mode Exceptions

#NM CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
#MF If there is a pending x87 FPU exception.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**FYL2X—Compute y * log₂x**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
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<td>FYL2X</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(1) with (ST(1) * log₂ST(0)) and pop the register stack.</td>
</tr>
</tbody>
</table>

**Description**

Computes (ST(1) * log₂ (ST(0))), stores the result in register ST(1), and pops the FPU register stack. The source operand in ST(0) must be a non-zero positive number.

The following table shows the results obtained when taking the log of various classes of numbers, assuming that neither overflow nor underflow occurs.

**Table 3-58. FYL2X Results**

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>−∞</th>
<th>−F</th>
<th>±0</th>
<th>+0&lt;+F&lt;+1</th>
<th>+1</th>
<th>+F&gt;+1</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
<td>*</td>
<td>+∞</td>
<td>+∞</td>
<td>*</td>
<td>−∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>*</td>
<td>*</td>
<td>**</td>
<td>+F</td>
<td>−0</td>
<td>−F</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>−0</td>
<td>−0</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>−0</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>*</td>
<td>*</td>
<td>**</td>
<td>−F</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
<td>*</td>
<td>−∞</td>
<td>−∞</td>
<td>*</td>
<td>+∞</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.
* Indicates floating-point invalid-operation (#IA) exception.
** Indicates floating-point zero-divide (#Z) exception.

If the divide-by-zero exception is masked and register ST(0) contains ±0, the instruction returns ± with a sign that is the opposite of the sign of the source operand in register ST(1).

The FYL2X instruction is designed with a built-in multiplication to optimize the calculation of logarithms with an arbitrary positive base (b):

\[
\log_b x \leftarrow (\log_2 b)^{-1} \times \log_2 x
\]

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
FYL2X—Compute \( y \cdot \log_2 x \)

**Operation**

\[
\text{ST}(1) \leftarrow \text{ST}(1) \cdot \log_2 \text{ST}(0);
\text{PopRegisterStack};
\]

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred.
  Set if result was rounded up; cleared otherwise.
- **C0, C2, C3** Undefined.

**Floating-Point Exceptions**

- **#IS** Stack underflow occurred.
- **#IA** Either operand is an SNaN or unsupported format.
  Source operand in register ST(0) is a negative finite value (not -0).
- **#Z** Source operand in register ST(0) is ±0.
- **#D** Source operand is a denormal value.
- **#U** Result is too small for destination format.
- **#O** Result is too large for destination format.
- **#P** Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#MF** If there is a pending x87 FPU exception.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
**FYL2XP1—Compute y * log₂(x + 1)**

### Opcode

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F9</td>
<td>FYL2XP1</td>
<td>Valid</td>
<td>Valid</td>
<td>Replace ST(1) with ST(1) * log₂(ST(0) + 1.0) and pop the register stack.</td>
</tr>
</tbody>
</table>

### Description

Computes (ST(1) * log₂(ST(0) + 1.0)), stores the result in register ST(1), and pops the FPU register stack. The source operand in ST(0) must be in the range:

\[-(1 - \sqrt{2}/2) to (1 - \sqrt{2}/2)\]

The source operand in ST(1) can range from \(-\infty\) to \(+\infty\). If the ST(0) operand is outside of its acceptable range, the result is undefined and software should not rely on an exception being generated. Under some circumstances exceptions may be generated when ST(0) is out of range, but this behavior is implementation specific and not guaranteed.

The following table shows the results obtained when taking the log epsilon of various classes of numbers, assuming that underflow does not occur.

#### Table 3-59. FYL2XP1 Results

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>ST(1)</th>
<th>(-1 \cdot (\sqrt{2}/2)) to (-0)</th>
<th>(-0)</th>
<th>(+0)</th>
<th>(+0) to (+1 \cdot (\sqrt{2}/2))</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>(-\infty)</td>
<td>(+\infty)</td>
<td>(*)</td>
<td>(*)</td>
<td>(-\infty)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>(-F)</td>
<td>(+F)</td>
<td>(+0)</td>
<td>(-0)</td>
<td>(-F)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>(-0)</td>
<td>(+0)</td>
<td>(+0)</td>
<td>(-0)</td>
<td>(-0)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>(+0)</td>
<td>(-0)</td>
<td>(-0)</td>
<td>(+0)</td>
<td>(+0)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>(+F)</td>
<td>(-F)</td>
<td>(-0)</td>
<td>(+0)</td>
<td>(+F)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>(+\infty)</td>
<td>(-\infty)</td>
<td>(*)</td>
<td>(*)</td>
<td>(+\infty)</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

F Means finite floating-point value.

* Indicates floating-point invalid-operation (#IA) exception.

This instruction provides optimal accuracy for values of epsilon [the value in register ST(0)] that are close to 0. For small epsilon (\(e\)) values, more significant digits can be retained by using the FYL2XP1 instruction than by using \((e+1)\) as an argument to the FYL2X instruction. The \((e+1)\) expression is commonly found in compound interest and annuity calculations. The result can be simply converted into a value in another logarithm base by including a scale factor in the ST(1) source operand. The following
equation is used to calculate the scale factor for a particular logarithm base, where \( n \) is the logarithm base desired for the result of the FYL2XP1 instruction:

\[
\text{scale factor} \leftarrow \log_n 2
\]

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[
\text{ST}(1) \leftarrow \text{ST}(1) \times \log_2(\text{ST}(0) + 1.0);
\]

PopRegisterStack;

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred.
- Set if result was rounded up; cleared otherwise.
- **C0, C2, C3** Undefined.

**Floating-Point Exceptions**

- **#IS** Stack underflow occurred.
- **#IA** Either operand is an SNaN value or unsupported format.
- **#D** Source operand is a denormal value.
- **#U** Result is too small for destination format.
- **#O** Result is too large for destination format.
- **#P** Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

- **#NM** CR0.EM[bit 2] or CR0.TS[bit 3] = 1.
- **#MF** If there is a pending x87 FPU exception.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
HADDPD—Packed Double-FP Horizontal Add

### Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 7C /r HADDPD xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE3</td>
<td>Horizontal add packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 7C /r VHADDPD xmm1,xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Horizontal add packed double-precision floating-point values from xmm2 and xmm3/mem.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 7C /r VHADDPD ymm1, ymm2, ymm3/m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Horizontal add packed double-precision floating-point values from ymm2 and ymm3/mem.</td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

 Adds the double-precision floating-point values in the high and low quadwords of the destination operand and stores the result in the low quadword of the destination operand.

 Adds the double-precision floating-point values in the high and low quadwords of the source operand and stores the result in the high quadword of the destination operand.

 In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

 See Figure 3-15 for HADDPD; see Figure 3-16 for VHADDPD.
HADDPD xmm1, xmm2/m128

Figure 3-15. HADDPD—Packed Double-FP Horizontal Add

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

Figure 3-16. VHADDPD operation
VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Operation

HADDPD (128-bit Legacy SSE version)
DEST[63:0] ← SRC1[127:64] + SRC1[63:0]
DEST[127:64] ← SRC2[127:64] + SRC2[63:0]
DEST[VLMAX-1:128] (Unmodified)

VHADDPD (VEX.128 encoded version)
DEST[63:0] ← SRC1[127:64] + SRC1[63:0]
DEST[127:64] ← SRC2[127:64] + SRC2[63:0]
DEST[VLMAX-1:128] ← 0

VHADDPD (VEX.256 encoded version)
DEST[63:0] ← SRC1[127:64] + SRC1[63:0]
DEST[127:64] ← SRC2[127:64] + SRC2[63:0]

Intel C/C++ Compiler Intrinsic Equivalent

VHADDPD: __m256d _mm256_hadd_pd (__m256d a, __m256d b);
HADDPD: __m128d _mm_hadd_pd (__m128d a, __m128d b);

Exceptions

When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

Numeric Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Other Exceptions
See Exceptions Type 2.
**HADDPS—Packed Single-FP Horizontal Add**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 7C /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE3</td>
<td>Horizontal add packed single-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>HADDPS xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.F2.0F:WIG 7C /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Horizontal add packed single-precision floating-point values from xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VHADDPS xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.F2.0F:WIG 7C /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Horizontal add packed single-precision floating-point values from ymm2 and ymm3/mem.</td>
</tr>
<tr>
<td>VHADDPS ymm1, ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Adds the single-precision floating-point values in the first and second dwords of the destination operand and stores the result in the first dword of the destination operand.

Adds single-precision floating-point values in the third and fourth dword of the destination operand and stores the result in the second dword of the destination operand.

Adds single-precision floating-point values in the first and second dword of the source operand and stores the result in the third dword of the destination operand.

Adds single-precision floating-point values in the third and fourth dword of the source operand and stores the result in the fourth dword of the destination operand.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
See Figure 3-17 for HADDPS; see Figure 3-18 for VHADDPS.

Figure 3-17. HADDPS—Packed Single-FP Horizontal Add

Figure 3-18. VHADDPS operation
128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**HADDPS (128-bit Legacy SSE version)**

DEST[31:0] ← SRC1[63:32] + SRC1[31:0]
DEST[95:64] ← SRC2[63:32] + SRC2[31:0]
DEST[VLMAX-1:128] (Unmodified)

**VHADDPS (VEX.128 encoded version)**

DEST[31:0] ← SRC1[63:32] + SRC1[31:0]
DEST[95:64] ← SRC2[63:32] + SRC2[31:0]
DEST[VLMAX-1:128] ← 0

**VHADDPS (VEX.256 encoded version)**

DEST[31:0] ← SRC1[63:32] + SRC1[31:0]
DEST[95:64] ← SRC2[63:32] + SRC2[31:0]

**Intel C/C++ Compiler Intrinsic Equivalent**

HADDPS: __m128 _mm_hadd_ps (__m128 a, __m128 b);

VHADDPS: __m256 _mm256_hadd_ps (__m256 a, __m256 b);
INSTRUCTION SET REFERENCE, A-L

Exceptions
When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

Numeric Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Other Exceptions
See Exceptions Type 2.
## HLT—Halt

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F4</td>
<td>HLT</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Halt</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Stops instruction execution and places the processor in a HALT state. An enabled interrupt (including NMI and SMI), a debug exception, the BINIT# signal, the INIT# signal, or the RESET# signal will resume execution. If an interrupt (including NMI) is used to resume execution after a HLT instruction, the saved instruction pointer (CS:EIP) points to the instruction following the HLT instruction.

When a HLT instruction is executed on an Intel 64 or IA-32 processor supporting Intel Hyper-Threading Technology, only the logical processor that executes the instruction is halted. The other logical processors in the physical processor remain active, unless they are each individually halted by executing a HLT instruction.

The HLT instruction is a privileged instruction. When the processor is running in protected or virtual-8086 mode, the privilege level of a program or procedure must be 0 to execute the HLT instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

### Operation

Enter Halt state;

### Flags Affected

None.

### Protected Mode Exceptions

- **#GP(0)** If the current privilege level is not 0.
- **#UD** If the LOCK prefix is used.

### Real-Address Mode Exceptions

None.
INSTRUCTION SET REFERENCE, A-L

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
HSUBPD—Packed Double-FP Horizontal Subtract

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 7D /r HSUBPD xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE3</td>
<td>Horizontal subtract packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 7D /r VHSUBPD xmm1,xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Horizontal subtract packed double-precision floating-point values from xmm2 and xmm3/mem.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 7D /r VHSUBPD ymm1, ymm2, ymm3/m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Horizontal subtract packed double-precision floating-point values from ymm2 and ymm3/mem.</td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

The HSUBPD instruction subtracts horizontally the packed DP FP numbers of both operands.

Subtracts the double-precision floating-point value in the high quadword of the destination operand from the low quadword of the destination operand and stores the result in the low quadword of the destination operand.

Subtracts the double-precision floating-point value in the high quadword of the source operand from the low quadword of the source operand and stores the result in the high quadword of the destination operand.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
See Figure 3-19 for HSUBPD; see Figure 3-20 for VHSUBPD.

**Figure 3-19. HSUBPD—Packed Double-FP Horizontal Subtract**

**Figure 3-20. VHSUBPD operation**

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.
VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**HSUBPD (128-bit Legacy SSE version)**
DEST[63:0] ← SRC1[63:0] - SRC1[127:64]
DEST[127:64] ← SRC2[63:0] - SRC2[127:64]
DEST[VLMAX-1:128] (Unmodified)

**VHSUBPD (VEX.128 encoded version)**
DEST[63:0] ← SRC1[63:0] - SRC1[127:64]
DEST[127:64] ← SRC2[63:0] - SRC2[127:64]
DEST[VLMAX-1:128] ← 0

**VHSUBPD (VEX.256 encoded version)**
DEST[63:0] ← SRC1[63:0] - SRC1[127:64]
DEST[127:64] ← SRC2[63:0] - SRC2[127:64]

**Intel C/C++ Compiler Intrinsic Equivalent**
HSUBPD: __m128d _mm_hsub_pd(__m128d a, __m128d b)
VHSUBPD: __m256d _mm256_hsub_pd (__m256d a, __m256d b);

**Exceptions**
When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

**Numeric Exceptions**
Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**
See Exceptions Type 2.
HSUBPS—Packed Single-FP Horizontal Subtract

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 7D /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE3</td>
<td>Horizontal subtract packed single-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>HSUBPS xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.F2.0F.WIG 7D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Horizontal subtract packed single-precision floating-point values from xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VHSUBPS xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.F2.0F.WIG 7D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Horizontal subtract packed single-precision floating-point values from ymm2 and ymm3/mem.</td>
</tr>
<tr>
<td>VHSUBPS ymm1, ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Subtracts the single-precision floating-point value in the second dword of the destination operand from the first dword of the destination operand and stores the result in the first dword of the destination operand.

Subtracts the single-precision floating-point value in the fourth dword of the destination operand from the third dword of the destination operand and stores the result in the second dword of the destination operand.

Subtracts the single-precision floating-point value in the second dword of the source operand from the first dword of the source operand and stores the result in the third dword of the destination operand.

Subtracts the single-precision floating-point value in the fourth dword of the source operand from the third dword of the source operand and stores the result in the fourth dword of the destination operand.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

See Figure 3-21 for HSUBPS; see Figure 3-22 for VHSUBPS.
Figure 3-21. HSUBPS—Packed Single-FP Horizontal Subtract

Figure 3-22. VHSUBPS operation
INSTRUCTION SET REFERENCE, A-L

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Operation

\textbf{HSUBPS (128-bit Legacy SSE version)}
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{SRC1}[31:0] - \text{SRC1}[63:32] \\
\text{DEST}[63:32] & \leftarrow \text{SRC1}[95:64] - \text{SRC1}[127:96] \\
\text{DEST}[95:64] & \leftarrow \text{SRC2}[31:0] - \text{SRC2}[63:32] \\
\text{DEST}[127:96] & \leftarrow \text{SRC2}[95:64] - \text{SRC2}[127:96] \\
\text{DEST}[VLMAX-1:128] & \leftarrow 0
\end{align*}

\textbf{VHSUBPS (VEX.128 encoded version)}
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{SRC1}[31:0] - \text{SRC1}[63:32] \\
\text{DEST}[63:32] & \leftarrow \text{SRC1}[95:64] - \text{SRC1}[127:96] \\
\text{DEST}[95:64] & \leftarrow \text{SRC2}[31:0] - \text{SRC2}[63:32] \\
\text{DEST}[127:96] & \leftarrow \text{SRC2}[95:64] - \text{SRC2}[127:96] \\
\text{DEST}[VLMAX-1:128] & \leftarrow 0
\end{align*}

\textbf{VHSUBPS (VEX.256 encoded version)}
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{SRC1}[31:0] - \text{SRC1}[63:32] \\
\text{DEST}[63:32] & \leftarrow \text{SRC1}[95:64] - \text{SRC1}[127:96] \\
\text{DEST}[95:64] & \leftarrow \text{SRC2}[31:0] - \text{SRC2}[63:32] \\
\text{DEST}[127:96] & \leftarrow \text{SRC2}[95:64] - \text{SRC2}[127:96] \\
\text{DEST}[159:128] & \leftarrow \text{SRC1}[159:128] - \text{SRC1}[191:160] \\
\text{DEST}[191:160] & \leftarrow \text{SRC1}[223:192] - \text{SRC1}[255:224] \\
\text{DEST}[223:192] & \leftarrow \text{SRC2}[159:128] - \text{SRC2}[191:160] \\
\text{DEST}[255:224] & \leftarrow \text{SRC2}[223:192] - \text{SRC2}[255:224]
\end{align*}

\textbf{Intel C/C++ Compiler Intrinsic Equivalent}

\begin{itemize}
\item HSUBPS: \texttt{__m128 \_mm\_hsub\_ps(__m128 a, __m128 b)};
\item VHSUBPS: \texttt{__m256 \_mm256\_hsub\_ps (__m256 a, __m256 b)};
\end{itemize}
Exceptions
When the source operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

Numeric Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Other Exceptions
See Exceptions Type 2.
IDIV—Signed Divide

**Opcode** | **Instruction** | **Op/En** | **64-Bit Mode** | **Compat/Leg Mode** | **Description**
--- | --- | --- | --- | --- | ---
F6 /7 | IDIV r/m8 | M | Valid | Valid | Signed divide AX by r/m8, with result stored in: AL ← Quotient, AH ← Remainder.
REX + F6 /7 | IDIV r/m8* | M | Valid | N.E. | Signed divide AX by r/m8, with result stored in AL ← Quotient, AH ← Remainder.
F7 /7 | IDIV r/m16 | M | Valid | Valid | Signed divide DX:AX by r/m16, with result stored in AX ← Quotient, DX ← Remainder.
F7 /7 | IDIV r/m32 | M | Valid | Valid | Signed divide EDX:EAX by r/m32, with result stored in EAX ← Quotient, EDX ← Remainder.
REX.W + F7 /7 | IDIV r/m64 | M | Valid | N.E. | Signed divide RDX:RAX by r/m64, with result stored in RAX ← Quotient, RDX ← Remainder.

**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

---

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModR/M:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Divides the (signed) value in the AX, DX:AX, or EDX:EAX (dividend) by the source operand (divisor) and stores the result in the AX (AH:AL), DX:AX, or EDX:EAX registers. The source operand can be a general-purpose register or a memory location. The action of this instruction depends on the operand size (dividend/divisor).

Non-integral results are truncated (chopped) towards 0. The remainder is always less than the divisor in magnitude. Overflow is indicated with the #DE (divide error) exception rather than with the CF flag.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. In 64-bit mode when REX.W is applied, the instruction
divides the signed value in RDX:RAX by the source operand. RAX contains a 64-bit quotient; RDX contains a 64-bit remainder.

See the summary chart at the beginning of this section for encoding data and limits. See Table 3-60.

### Table 3-60. IDIV Results

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Dividend</th>
<th>Divisor</th>
<th>Quotient</th>
<th>Remainder</th>
<th>Quotient Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word/byte</td>
<td>AX</td>
<td>r/m8</td>
<td>AL</td>
<td>AH</td>
<td>−128 to +127</td>
</tr>
<tr>
<td>Doubleword/word</td>
<td>DX:AX</td>
<td>r/m16</td>
<td>AX</td>
<td>DX</td>
<td>−32,768 to +32,767</td>
</tr>
<tr>
<td>Quadword/doubleword</td>
<td>EDX:EAX</td>
<td>r/m32</td>
<td>EAX</td>
<td>EDX</td>
<td>−2^{31} to 2^{32} − 1</td>
</tr>
<tr>
<td>Doublequadword/quadword</td>
<td>RDX:RAX</td>
<td>r/m64</td>
<td>RAX</td>
<td>RDX</td>
<td>−2^{63} to 2^{64} − 1</td>
</tr>
</tbody>
</table>

**Operation**

IF SRC = 0

THEN #DE; (* Divide error *)

FI;

IF OperandsSize = 8 (* Word/byte operation *)

THEN

    temp ← AX / SRC; (* Signed division *)

    IF (temp > 7FH) or (temp < 80H)

    (* If a positive result is greater than 7FH or a negative result is less than 80H *)

    THEN #DE; (* Divide error *)

    ELSE

        AL ← temp;
        AH ← AX SignedModulus SRC;

    FI;

ELSE IF OperandsSize = 16 (* Doubleword/word operation *)

THEN

    temp ← DX:AX / SRC; (* Signed division *)

    IF (temp > 7FFFH) or (temp < 8000H)

    (* If a positive result is greater than 7FFFH or a negative result is less than 8000H *)

    THEN #DE; (* Divide error *)

    ELSE

        AX ← temp;
        DX ← DX:AX SignedModulus SRC;

    FI;

FI;
ELSE IF "OperandSize = 32 (* Quadword/doubleword operation *)"
    temp ← EDX:EAX / SRC; (* Signed division *)
    IF (temp > 7FFFFFFFH) or (temp < 80000000H)
    (* If a positive result is greater than 7FFFFFFFH
    or a negative result is less than 80000000H *)
    THEN
        #DE; (* Divide error *)
    ELSE
        EAX ← temp;
        EDX ← EDX:EAX SignedModulus SRC;
    FI;
    FI;
ELSE IF "OperandSize = 64 (* Doublequadword/quadword operation *)"
    temp ← RDX:RAX / SRC; (* Signed division *)
    IF (temp > 7FFFFFFFFFFFFFFFH) or (temp < 8000000000000000H)
    (* If a positive result is greater than 7FFFFFFFFFFFFFFFH
    or a negative result is less than 8000000000000000H *)
    THEN
        #DE; (* Divide error *)
    ELSE
        RAX ← temp;
        RDX ← RDE:RAX SignedModulus SRC;
    FI;
    FI;

Flags Affected
The CF, OF, SF, ZF, AF, and PF flags are undefined.

Protected Mode Exceptions
#DE If the source operand (divisor) is 0.
    The signed result (quotient) is too large for the destination.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
Real-Address Mode Exceptions

#DE If the source operand (divisor) is 0.

The signed result (quotient) is too large for the destination.

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#DE If the source operand (divisor) is 0.

The signed result (quotient) is too large for the destination.

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#DE If the source operand (divisor) is 0

If the quotient is too large for the designated register.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
### IMUL—Signed Multiply

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /5</td>
<td>IMUL r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>AX ← AL * r/m byte.</td>
</tr>
<tr>
<td>F7 /5</td>
<td>IMUL r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>DX:AX ← AX * r/m word.</td>
</tr>
<tr>
<td>F7 /5</td>
<td>IMUL r/m32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>EDX:EAX ← EAX * r/m32.</td>
</tr>
<tr>
<td>REX.W + F7 /5</td>
<td>IMUL r/m64</td>
<td>M</td>
<td>N.E.</td>
<td>Valid</td>
<td>RDX:RAX ← RAX * r/m64.</td>
</tr>
<tr>
<td>0F AF /r</td>
<td>IMUL r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>word register ← word register * r/m16.</td>
</tr>
<tr>
<td>0F AF /r</td>
<td>IMUL r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>doubleword register ← doubleword register * r/m32.</td>
</tr>
<tr>
<td>REX.W + 0F AF /r</td>
<td>IMUL r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Quadword register ← Quadword register * r/m64.</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r16, r/m16, imm8</td>
<td>RMI</td>
<td>Valid</td>
<td></td>
<td>word register ← r/m16 * sign-extended immediate byte.</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r32, r/m32, imm8</td>
<td>RMI</td>
<td>Valid</td>
<td></td>
<td>doubleword register ← r/m32 * sign-extended immediate byte.</td>
</tr>
<tr>
<td>REX.W + 6B /r ib</td>
<td>IMUL r64, r/m64, imm8</td>
<td>RMI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Quadword register ← r/m64 * sign-extended immediate byte.</td>
</tr>
<tr>
<td>69 /r iw</td>
<td>IMUL r16, r/m16, imm16</td>
<td>RMI</td>
<td>Valid</td>
<td></td>
<td>word register ← r/m16 * immediate word.</td>
</tr>
<tr>
<td>69 /r id</td>
<td>IMUL r32, r/m32, imm32</td>
<td>RMI</td>
<td>Valid</td>
<td></td>
<td>doubleword register ← r/m32 * immediate doubleword.</td>
</tr>
<tr>
<td>REX.W + 69 /r id</td>
<td>IMUL r64, r/m64, imm32</td>
<td>RMI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Quadword register ← r/m64 * immediate doubleword.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
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<th>Operand 3</th>
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</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRMr/m (r, w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
Description
Performs a signed multiplication of two operands. This instruction has three forms, depending on the number of operands.

- **One-operand form** — This form is identical to that used by the MUL instruction. Here, the source operand (in a general-purpose register or memory location) is multiplied by the value in the AL, AX, EAX, or RAX register (depending on the operand size) and the product is stored in the AX, DX:AX, EDX:EAX, or RDX:RAX registers, respectively.

- **Two-operand form** — With this form the destination operand (the first operand) is multiplied by the source operand (second operand). The destination operand is a general-purpose register and the source operand is an immediate value, a general-purpose register, or a memory location. The product is then stored in the destination operand location.

- **Three-operand form** — This form requires a destination operand (the first operand) and two source operands (the second and the third operands). Here, the first source operand (which can be a general-purpose register or a memory location) is multiplied by the second source operand (an immediate value). The product is then stored in the destination operand (a general-purpose register).

When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The CF and OF flags are set when significant bit (including the sign bit) are carried into the upper half of the result. The CF and OF flags are cleared when the result (including the sign bit) fits exactly in the lower half of the result.

The three forms of the IMUL instruction are similar in that the length of the product is calculated to twice the length of the operands. With the one-operand form, the product is stored exactly in the destination. With the two- and three-operand forms, however, the result is truncated to the length of the destination before it is stored in the destination register. Because of this truncation, the CF or OF flag should be tested to ensure that no significant bits are lost.

The two- and three-operand forms may also be used with unsigned operands because the lower half of the product is the same regardless if the operands are signed or unsigned. The CF and OF flags, however, cannot be used to determine if the upper half of the result is non-zero.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. Use of REX.W modifies the three forms of the instruction as follows.
• One-operand form — The source operand (in a 64-bit general-purpose register or memory location) is multiplied by the value in the RAX register and the product is stored in the RDX:RAX registers.

• **Two-operand form** — The source operand is promoted to 64 bits if it is a register or a memory location. If the source operand is an immediate, it is sign extended to 64 bits. The destination operand is promoted to 64 bits.

• **Three-operand form** — The first source operand (either a register or a memory location) and destination operand are promoted to 64 bits.

**Operation**

\[
\text{IF } (\text{NumberOfOperands} = 1) \\
\quad \text{THEN IF } (\text{OperandSize} = 8) \\
\quad \quad \text{THEN} \\
\quad \quad \quad \text{AX} \leftarrow \text{AL} \times \text{SRC} \quad (\text{Signed multiplication}) \\
\quad \quad \quad \text{IF AL} = \text{AX} \\
\quad \quad \quad \quad \text{THEN CF} \leftarrow 0; \text{OF} \leftarrow 0; \\
\quad \quad \quad \quad \text{ELSE CF} \leftarrow 1; \text{OF} \leftarrow 1; \text{Fl}; \\
\quad \quad \quad \text{ELSE IF OperandSize} = 16 \\
\quad \quad \quad \quad \text{THEN} \\
\quad \quad \quad \quad \quad \text{DX:AX} \leftarrow \text{AX} \times \text{SRC} \quad (\text{Signed multiplication}) \\
\quad \quad \quad \quad \quad \text{IF sign\_extend\_to\_32 (AX)} = \text{DX:AX} \\
\quad \quad \quad \quad \quad \quad \text{THEN CF} \leftarrow 0; \text{OF} \leftarrow 0; \\
\quad \quad \quad \quad \quad \quad \text{ELSE CF} \leftarrow 1; \text{OF} \leftarrow 1; \text{Fl}; \\
\quad \quad \quad \text{ELSE IF OperandSize} = 32 \\
\quad \quad \quad \quad \text{THEN} \\
\quad \quad \quad \quad \quad \text{EDX:EAX} \leftarrow \text{EAX} \times \text{SRC} \quad (\text{Signed multiplication}) \\
\quad \quad \quad \quad \quad \text{IF EAX} = \text{EDX:EAX} \\
\quad \quad \quad \quad \quad \quad \text{THEN CF} \leftarrow 0; \text{OF} \leftarrow 0; \\
\quad \quad \quad \quad \quad \quad \text{ELSE CF} \leftarrow 1; \text{OF} \leftarrow 1; \text{Fl}; \\
\quad \quad \quad \text{ELSE (* OperandSize = 64 *)} \\
\quad \quad \quad \quad \text{RDX:RAX} \leftarrow \text{RAX} \times \text{SRC} \quad (\text{Signed multiplication}) \\
\quad \quad \quad \quad \text{IF RAX} = \text{RDX:RAX} \\
\quad \quad \quad \quad \quad \text{THEN CF} \leftarrow 0; \text{OF} \leftarrow 0; \\
\quad \quad \quad \quad \quad \text{ELSE CF} \leftarrow 1; \text{OF} \leftarrow 1; \text{Fl}; \\
\quad \quad \quad \text{Fl;} \\
\quad \quad \quad \text{ELSE IF (NumberOfOperands = 2)} \\
\quad \quad \quad \quad \text{THEN} \\
\quad \quad \quad \quad \quad \text{temp} \leftarrow \text{DEST} \times \text{SRC} \quad (\text{Signed multiplication}; \text{temp is double DEST size}) \\
\quad \quad \quad \quad \quad \text{DEST} \leftarrow \text{DEST} \times \text{SRC} \quad (\text{Signed multiplication}) \\
\quad \quad \quad \quad \quad \text{IF temp} \neq \text{DEST} \\
\quad \quad \quad \quad \quad \quad \text{THEN CF} \leftarrow 1; \text{OF} \leftarrow 1; \\
\quad \quad \quad \quad \quad \quad \text{ELSE CF} \leftarrow 0; \text{OF} \leftarrow 0; \text{Fl;} \
\text{Fl;}
\text{ELSE IF (NumberOfOperands = 2)} \\
\quad \text{THEN} \\
\text{temp} \leftarrow \text{DEST} \times \text{SRC} \quad (\text{Signed multiplication}; \text{temp is double DEST size}) \\
\text{DEST} \leftarrow \text{DEST} \times \text{SRC} \quad (\text{Signed multiplication}) \\
\text{IF temp} \neq \text{DEST} \\
\quad \text{THEN CF} \leftarrow 1; \text{OF} \leftarrow 1; \\
\quad \text{ELSE CF} \leftarrow 0; \text{OF} \leftarrow 0; \text{Fl;}
\]
ELSE (* NumberOfOperands = 3 *)
DEST ← SRC1 ∗ SRC2 (* Signed multiplication *)
temp ← SRC1 ∗ SRC2 (* Signed multiplication; temp is double SRC1 size *)
IF temp ≠ DEST
THEN CF ← 1; OF ← 1;
ELSE CF ← 0; OF ← 0; Fl;
Fl;
Fl;

Flags Affected
For the one operand form of the instruction, the CF and OF flags are set when significant bits are carried into the upper half of the result and cleared when the result fits exactly in the lower half of the result. For the two- and three-operand forms of the instruction, the CF and OF flags are set when the result must be truncated to fit in the destination operand size and cleared when the result fits exactly in the destination operand size. The SF, ZF, AF, and PF flags are undefined.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register is used to access memory and it contains a NULL NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
IN—Input from Port

Copies the value from the I/O port specified with the second operand (source operand) to the destination operand (first operand). The source operand can be a byte-immediate or the DX register; the destination operand can be register AL, AX, or EAX, depending on the size of the port being accessed (8, 16, or 32 bits, respectively). Using the DX register as a source operand allows I/O port addresses from 0 to 65,535 to be accessed; using a byte immediate allows I/O port addresses 0 to 255 to be accessed.

When accessing an 8-bit I/O port, the opcode determines the port size; when accessing a 16- and 32-bit I/O port, the operand-size attribute determines the port size. At the machine code level, I/O instructions are shorter when accessing 8-bit I/O ports. Here, the upper eight bits of the port address will be 0.

This instruction is only useful for accessing I/O ports located in the processor’s I/O address space. See Chapter 13, “Input/Output,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information on accessing I/O ports in the I/O address space.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

---

### IN—Input from Port

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E4 ib</td>
<td>IN AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Input byte from imm8 I/O port address into AL.</td>
</tr>
<tr>
<td>E5 ib</td>
<td>IN AX, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Input word from imm8 I/O port address into AX.</td>
</tr>
<tr>
<td>E5 ib</td>
<td>IN EAX, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Input dword from imm8 I/O port address into EAX.</td>
</tr>
<tr>
<td>EC</td>
<td>IN AL,DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input byte from I/O port in DX into AL.</td>
</tr>
<tr>
<td>ED</td>
<td>IN AX,DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input word from I/O port in DX into AX.</td>
</tr>
<tr>
<td>ED</td>
<td>IN EAX,DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input doubleword from I/O port in DX into EAX.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Copies the value from the I/O port specified with the second operand (source operand) to the destination operand (first operand). The source operand can be a byte-immediate or the DX register; the destination operand can be register AL, AX, or EAX, depending on the size of the port being accessed (8, 16, or 32 bits, respectively). Using the DX register as a source operand allows I/O port addresses from 0 to 65,535 to be accessed; using a byte immediate allows I/O port addresses 0 to 255 to be accessed.

When accessing an 8-bit I/O port, the opcode determines the port size; when accessing a 16- and 32-bit I/O port, the operand-size attribute determines the port size. At the machine code level, I/O instructions are shorter when accessing 8-bit I/O ports. Here, the upper eight bits of the port address will be 0.

This instruction is only useful for accessing I/O ports located in the processor’s I/O address space. See Chapter 13, “Input/Output,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information on accessing I/O ports in the I/O address space.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
INSTRUCTION SET REFERENCE, A-L

Operation

IF ((PE = 1) and ((CPL > IOPL) or (VM = 1)))
   THEN (* Protected mode with CPL > IOPL or virtual-8086 mode *)
      IF (Any I/O Permission Bit for I/O port being accessed = 1)
         THEN (* I/O operation is not allowed *)
            #GP(0);
      ELSE (* I/O operation is allowed *)
         DEST ← SRC; (* Read from selected I/O port *)
      FI;
   ELSE (Real Mode or Protected Mode with CPL ≤ IOPL *)
      DEST ← SRC; (* Read from selected I/O port *)
   FI;

Flags Affected
None.

Protected Mode Exceptions

#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.

#PF(fault-code) If a page fault occurs.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.

#UD If the LOCK prefix is used.
INC—Increment by 1

#### Opcode Table

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE /0</td>
<td>INC r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Increment r/m byte by 1.</td>
</tr>
<tr>
<td>REX + FE /0</td>
<td>INC r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Increment r/m byte by 1.</td>
</tr>
<tr>
<td>FF /0</td>
<td>INC r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Increment r/m word by 1.</td>
</tr>
<tr>
<td>FF /0</td>
<td>INC r/m32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Increment r/m doubleword by 1.</td>
</tr>
<tr>
<td>REX.W + FF /0</td>
<td>INC r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Increment r/m quadword by 1.</td>
</tr>
<tr>
<td>40+ rw**</td>
<td>INC r16</td>
<td>O</td>
<td>N.E.</td>
<td>Valid</td>
<td>Increment word register by 1.</td>
</tr>
<tr>
<td>40+ rd</td>
<td>INC r32</td>
<td>O</td>
<td>N.E.</td>
<td>Valid</td>
<td>Increment doubleword register by 1.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 cannot be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

** 40H through 47H are REX prefixes in 64-bit mode.

#### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRMr/m (r, w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0</td>
<td>opcode + rd (r, w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Description

Adds 1 to the destination operand, while preserving the state of the CF flag. The destination operand can be a register or a memory location. This instruction allows a loop counter to be updated without disturbing the CF flag. (Use a ADD instruction with an immediate operand of 1 to perform an increment operation that does updates the CF flag.)

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, INC r16 and INC r32 are not encodable (because opcodes 40H through 47H are REX prefixes). Otherwise, the instruction's 64-bit mode default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits.
INSTRUCTION SET REFERENCE, A-L

Operation

DEST ← DEST + 1;

AFlags Affected

The CF flag is not affected. The OF, SF, ZF, AF, and PF flags are set according to the result.

Protected Mode Exceptions

#GP(0) If the destination operand is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.
INS/INSB/INSW/INSD—Input from Port to String

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6C</td>
<td>INS m8, DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input byte from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.*</td>
</tr>
<tr>
<td>6D</td>
<td>INS m16, DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input word from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.¹</td>
</tr>
<tr>
<td>6D</td>
<td>INS m32, DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input doubleword from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.¹</td>
</tr>
<tr>
<td>6C</td>
<td>INSB</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input byte from I/O port specified in DX into memory location specified with ES:(E)DI or RDI.¹</td>
</tr>
<tr>
<td>6D</td>
<td>INSW</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input word from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.¹</td>
</tr>
<tr>
<td>6D</td>
<td>INSD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input doubleword from I/O port specified in DX into memory location specified in ES:(E)DI or RDI.¹</td>
</tr>
</tbody>
</table>

NOTES:
* In 64-bit mode, only 64-bit (RDI) and 32-bit (EDI) address sizes are supported. In non-64-bit mode, only 32-bit (EDI) and 16-bit (DI) address sizes are supported.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Copies the data from the I/O port specified with the source operand (second operand) to the destination operand (first operand). The source operand is an I/O port address (from 0 to 65,535) that is read from the DX register. The destination operand is a memory location, the address of which is read from either the ES:DI, ES:EDI or the RDI registers (depending on the address-size attribute of the instruc-
The ES segment cannot be overridden with a segment override prefix.) The size of the I/O port being accessed (that is, the size of the source and destination operands) is determined by the opcode for an 8-bit I/O port or by the operand-size attribute of the instruction for a 16- or 32-bit I/O port.

At the assembly-code level, two forms of this instruction are allowed: the “explicit-operands” form and the “no-operands” form. The explicit-operands form (specified with the INS mnemonic) allows the source and destination operands to be specified explicitly. Here, the source operand must be “DX,” and the destination operand should be a symbol that indicates the size of the I/O port and the destination address. This explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the destination operand symbol must specify the correct type (size) of the operand (byte, word, or doubleword), but it does not have to specify the correct location. The location is always specified by the ES:(E)DI registers, which must be loaded correctly before the INS instruction is executed.

The no-operands form provides "short forms" of the byte, word, and doubleword versions of the INS instructions. Here also DX is assumed by the processor to be the source operand and ES:(E)DI is assumed to be the destination operand. The size of the I/O port is specified with the choice of mnemonic: INSB (byte), INSW (word), or INSD (doubleword).

After the byte, word, or doubleword is transfer from the I/O port to the memory location, the DI/EDI/RDI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E)DI register is incremented; if the DF flag is 1, the (E)DI register is decremented.) The (E)DI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The INS, INSB, INSW, and INSD instructions can be preceded by the REP prefix for block input of ECX bytes, words, or doublewords. See “REP/REPE/REPZ /REPNE/REPNZ—Repeat String Operation Prefix” in Chapter 4 of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B, for a description of the REP prefix.

These instructions are only useful for accessing I/O ports located in the processor’s I/O address space. See Chapter 13, “Input/Output,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information on accessing I/O ports in the I/O address space.

In 64-bit mode, default address size is 64 bits, 32 bit address size is supported using the prefix 67H. The address of the memory destination is specified by RDI or EDI. 16-bit address size is not supported in 64-bit mode. The operand size is not promoted.

Operation

\[
\text{IF ((PE = 1) and ((CPL > IOPL) or (VM = 1)))} \\
\text{THEN (* Protected mode with CPL > IOPL or virtual-8086 mode *)}
\]
INS/INSB/INSW/INSD—Input from Port to String

IF (Any I/O Permission Bit for I/O port being accessed = 1)
THEN (* I/O operation is not allowed *)
  #GP(0);
ELSE (* I/O operation is allowed *)
  DEST ← SRC; (* Read from I/O port *)
FI;
ELSE (Real Mode or Protected Mode with CPL IOPL *)
  DEST ← SRC; (* Read from I/O port *)
FI;
FI;
Non-64-bit Mode:
IF (Byte transfer)
THEN IF DF = 0
  THEN (E)DI ← (E)DI + 1;
  ELSE (E)DI ← (E)DI - 1; FI;
ELSE IF (Word transfer)
  THEN IF DF = 0
    THEN (E)DI ← (E)DI + 2;
    ELSE (E)DI ← (E)DI - 2; FI;
ELSE (* Doubleword transfer *)
  THEN IF DF = 0
    THEN (E)DI ← (E)DI + 4;
    ELSE (E)DI ← (E)DI - 4; FI;
FI;
FI;
FI64-bit Mode:
IF (Byte transfer)
THEN IF DF = 0
  THEN (E|R)DI ← (E|R)DI + 1;
  ELSE (E|R)DI ← (E|R)DI - 1; FI;
ELSE IF (Word transfer)
  THEN IF DF = 0
    THEN (E)DI ← (E)DI + 2;
    ELSE (E)DI ← (E)DI - 2; FI;
ELSE (* Doubleword transfer *)
  THEN IF DF = 0
    THEN (E|R)DI ← (E|R)DI + 4;
    ELSE (E|R)DI ← (E|R)DI - 4; FI;
FI;
FI;
Flags Affected
None.

Protected Mode Exceptions
- **#GP(0)**: If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.
  - If the destination is located in a non-writable segment.
  - If an illegal memory operand effective address in the ES segments is given.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used.

Real-Address Mode Exceptions
- **#GP**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS**: If a memory operand effective address is outside the SS segment limit.
- **#UD**: If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
- **#GP(0)**: If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made.
- **#UD**: If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
- **#SS(0)**: If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)**: If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.
  - If the memory address is in a non-canonical form.
INSTRUCTION SET REFERENCE, A-L

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
INSERTPS — Insert Packed Single Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 21 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE_4_1</td>
<td>Insert a single precision floating-point value selected by imm8 from xmm2/m32 into xmm1 at the specified destination element specified by imm8 and zero out destination elements in xmm1 as indicated in imm8.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.WIG 21 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Insert a single precision floating point value selected by imm8 from xmm3/m32 and merge into xmm2 at the specified destination element specified by imm8 and zero out destination elements in xmm1 as indicated in imm8.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMr/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

(register source form)
Select a single precision floating-point element from second source as indicated by Count_S bits of the immediate operand and insert it into the first source at the location indicated by the Count_D bits of the immediate operand. Store in the destination and zero out destination elements based on the ZMask bits of the immediate operand.

(memory source form)
Load a floating-point element from a 32-bit memory location and insert it into the first source at the location indicated by the Count_D bits of the immediate operand. Store in the destination and zero out destination elements based on the ZMask bits of the immediate operand.
128-bit Legacy SSE version: The first source register is an XMM register. The second source operand is either an XMM register or a 32-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version. The destination and first source register is an XMM register. The second source operand is either an XMM register or a 32-bit memory location. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

If VINSERTPS is encoded with VEX.L=1, an attempt to execute the instruction encoded with VEX.L=1 will cause an #UD exception.

**Operation**

**INSERTPS (128-bit Legacy SSE version)**

IF (SRC = REG) THEN COUNT_S <- imm8[7:6]
ELSE COUNT_S <- 0

COUNT_D <- imm8[5:4]
ZMASK <- imm8[3:0]

CASE (COUNT_S) OF
  0: TMP <- SRC[31:0]
  1: TMP <- SRC[63:32]
  2: TMP <- SRC[95:64]
  3: TMP <- SRC[127:96]
ESAC;

CASE (COUNT_D) OF
  0: TMP2[31:0] <- TMP
  1: TMP2[63:32] <- TMP
      TMP2[31:0] <- DEST[31:0]
      TMP2[127:64] <- DEST[127:64]
  2: TMP2[95:64] <- TMP
      TMP2[63:0] <- DEST[63:0]
  3: TMP2[127:96] <- TMP
      TMP2[95:0] <- DEST[95:0]
ESAC;

IF (ZMASK[0] = 1) THEN DEST[31:0] <- 00000000H
ELSE DEST[31:0] <- TMP2[31:0]
INSERTPS — Insert Packed Single Precision Floating-Point Value

IF (ZMASK[2] = 1) THEN DEST[95:64] ← 00000000H
    ELSE DEST[95:64] ← TMP2[95:64]
    ELSE DEST[127:96] ← TMP2[127:96]
DEST[VLMAX-1:128] (Unmodified)

VINSERTPS (VEX.128 encoded version)
IF (SRC = REG) THEN COUNT_S ← imm8[7:6]
    ELSE COUNT_S ← 0
COUNT_D ← imm8[5:4]
ZMASK ← imm8[3:0]
CASE (COUNT_S) OF
    0: TMP ← SRC2[31:0]
    1: TMP ← SRC2[63:32]
    2: TMP ← SRC2[95:64]
    3: TMP ← SRC2[127:96]
ESAC;
CASE (COUNT_D) OF
    0: TMP2[31:0] ← TMP
    1: TMP2[63:32] ← TMP
       TMP2[31:0] ← SRC1[31:0]
       TMP2[127:64] ← SRC1[127:64]
    2: TMP2[95:64] ← TMP
       TMP2[63:0] ← SRC1[63:0]
       TMP2[127:96] ← SRC1[127:96]
    3: TMP2[127:96] ← TMP
       TMP2[95:0] ← SRC1[95:0]
ESAC;

IF (ZMASK[0] = 1) THEN DEST[31:0] ← 00000000H
    ELSE DEST[31:0] ← TMP2[31:0]
IF (ZMASK[2] = 1) THEN DEST[95:64] ← 00000000H
    ELSE DEST[95:64] ← TMP2[95:64]
    ELSE DEST[127:96] ← TMP2[127:96]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent

INSERTPS: __m128 _mm_insert_ps(__m128 dst, __m128 src, const int ndx);
SIMD Floating-Point Exceptions
None

Other Exceptions
See Exceptions Type 5.
INT n/INTO/INT 3—Call to Interrupt Procedure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC</td>
<td>INT 3</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Interrupt 3—trap to debugger.</td>
</tr>
<tr>
<td>CD ib</td>
<td>INT imm8</td>
<td>I</td>
<td>Valid</td>
<td></td>
<td>Interrupt vector number specified by immediate byte.</td>
</tr>
<tr>
<td>CE</td>
<td>INTO</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Interrupt 4—if overflow flag is 1.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>I</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

The INT n instruction generates a call to the interrupt or exception handler specified with the destination operand (see the section titled “Interrupts and Exceptions” in Chapter 6 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). The destination operand specifies an interrupt vector number from 0 to 255, encoded as an 8-bit unsigned intermediate value. Each interrupt vector number provides an index to a gate descriptor in the IDT. The first 32 interrupt vector numbers are reserved by Intel for system use. Some of these interrupts are used for internally generated exceptions.

The INT n instruction is the general mnemonic for executing a software-generated call to an interrupt handler. The INTO instruction is a special mnemonic for calling overflow exception (#OF), interrupt vector number 4. The overflow interrupt checks the OF flag in the EFLAGS register and calls the overflow interrupt handler if the OF flag is set to 1. (The INTO instruction cannot be used in 64-bit mode.)

The INT 3 instruction generates a special one byte opcode (CC) that is intended for calling the debug exception handler. (This one byte form is valuable because it can be used to replace the first byte of any instruction with a breakpoint, including other one byte instructions, without over-writing other code). To further support its function as a debug breakpoint, the interrupt generated with the CC opcode also differs from the regular software interrupts as follows:

- Interrupt redirection does not happen when in VME mode; the interrupt is handled by a protected-mode handler.
- The virtual-8086 mode IOPL checks do not occur. The interrupt is taken without faulting at any IOPL level.
Note that the "normal" 2-byte opcode for INT 3 (CD03) does not have these special features. Intel and Microsoft assemblers will not generate the CD03 opcode from any mnemonic, but this opcode can be created by direct numeric code definition or by self-modifying code.

The action of the INT \( n \) instruction (including the INTO and INT 3 instructions) is similar to that of a far call made with the CALL instruction. The primary difference is that with the INT \( n \) instruction, the EFLAGS register is pushed onto the stack before the return address. (The return address is a far address consisting of the current values of the CS and EIP registers.) Returns from interrupt procedures are handled with the IRET instruction, which pops the EFLAGS information and return address from the stack.

The interrupt vector number specifies an interrupt descriptor in the interrupt descriptor table (IDT); that is, it provides index into the IDT. The selected interrupt descriptor in turn contains a pointer to an interrupt or exception handler procedure. In protected mode, the IDT contains an array of 8-byte descriptors, each of which is an interrupt gate, trap gate, or task gate. In real-address mode, the IDT is an array of 4-byte far pointers (2-byte code segment selector and a 2-byte instruction pointer), each of which point directly to a procedure in the selected segment. (Note that in real-address mode, the IDT is called the interrupt vector table, and its pointers are called interrupt vectors.)

The following decision table indicates which action in the lower portion of the table is taken given the conditions in the upper portion of the table. Each Y in the lower section of the decision table represents a procedure defined in the "Operation" section for this instruction (except #GP).

<table>
<thead>
<tr>
<th>PE</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>IOPL</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>&lt;3</td>
<td>=3</td>
</tr>
<tr>
<td>CPL/CPL RELATIONSHIP</td>
<td>DPL&lt; CPL</td>
<td>DPL&lt; CPL or C</td>
<td>DPL&lt; CPL &amp; NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTERRUPT TYPE</td>
<td>-</td>
<td>S/W</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GATE TYPE</td>
<td>-</td>
<td>-</td>
<td>Task</td>
<td>Trap or Interrupt</td>
<td>Trap or Interrupt</td>
<td>Trap or Interrupt</td>
<td>Trap or Interrupt</td>
</tr>
<tr>
<td>REAL-ADDRESS-MODE</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PROTECTED-MODE</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>TRAP-OR-INTERRUPT-GATE</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTER-PRIVILEGE-LEVEL-INTERRUPT</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTRA-PRIVILEGE-LEVEL-INTERRUPT</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
When the processor is executing in virtual-8086 mode, the IOPL determines the action of the INT n instruction. If the IOPL is less than 3, the processor generates a #GP(selector) exception; if the IOPL is 3, the processor executes a protected mode interrupt to privilege level 0. The interrupt gate's DPL must be set to 3 and the target CPL of the interrupt handler procedure must be 0 to execute the protected mode interrupt to privilege level 0.

The interrupt descriptor table register (IDTR) specifies the base linear address and limit of the IDT. The initial base address value of the IDTR after the processor is powered up or reset is 0.

Operation

The following operational description applies not only to the INT n and INTO instructions, but also to external interrupts, nonmaskable interrupts (NMIs), and exceptions. Some of these events push onto the stack an error code.

The operational description specifies numerous checks whose failure may result in delivery of a nested exception. In these cases, the original event is not delivered.

The operational description specifies the error code delivered by any nested exception. In some cases, the error code is specified with a pseudofunction error_code(num,idt,ext), where idt and ext are bit values. The pseudofunction produces an error code as follows: (1) if idt is 0, the error code is (num & FCH) | ext; (2) if idt is 1, the error code is (num « 3) | 2 | ext.

In many cases, the pseudofunction error_code is invoked with a pseudovariable EXT. The value of EXT depends on the nature of the event whose delivery encountered a nested exception: if that event is a software interrupt, EXT is 0; otherwise, EXT is 1.

IF PE = 0
THEN
   GOTO REAL-ADDRESS-MODE;
ELSE (* PE = 1 *)
   IF (VM = 1 and IOPL < 3 AND INT n)
      THEN
         #GP(0); (* Bit 0 of error code is 0 because INT n *)

Table 3-61. Decision Table (Contd.)

<table>
<thead>
<tr>
<th>INTERRUPT-FROM-VIRTUAL-8086-MODE</th>
<th>TASK-GATE</th>
<th>#GP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
</tbody>
</table>

NOTES:
- Don't Care.
- Y Yes, action taken.
- Blank Action not taken.

Table 3-61. Decision Table (Contd.)

- Do not care.
- Y Yes, action taken.
- Blank Action not taken.
ELSE (* Protected mode, IA-32e mode, or virtual-8086 mode interrupt *)
    IF (IA32_EFER.LMA = 0)
        THEN (* Protected mode, or virtual-8086 mode interrupt *)
            GOTO PROTECTED-MODE;
    ELSE (* IA-32e mode interrupt *)
        GOTO IA-32e-MODE;
    FI;
FI;
FI;
REAL-ADDRESS-MODE:
    IF ((vector_number « 2) + 3) is not within IDT limit
        THEN #GP; FI;
    IF stack not large enough for a 6-byte return information
        THEN #SS; FI;
    Push (EFLAGS[15:0]);
    IF ← 0; (* Clear interrupt flag *)
    TF ← 0; (* Clear trap flag *)
    AC ← 0; (* Clear AC flag *)
    Push(CS);
    Push(IP);
    (* No error codes are pushed in real-address mode*)
    CS ← IDT(Descriptor (vector_number « 2), selector));
    EIP ← IDT(Descriptor (vector_number « 2), offset)); (* 16 bit offset AND 0000FFFFH *)
END;
PROTECTED-MODE:
    IF ((vector_number « 3) + 7) is not within IDT limits
    or selected IDT descriptor is not an interrupt-, trap-, or task-gate type
        THEN #GP(error_code(vector_number,1,EXT)); FI;
    (* idt operand to error_code set because vector is used *)
    IF software interrupt (* Generated by INT n, INT3, or INTO *)
        THEN
            IF gate DPL < CPL (* PE = 1, DPL < CPL, software interrupt *)
                THEN #GP(error_code(vector_number,1,0)); FI;
                (* idt operand to error_code set because vector is used *)
                (* ext operand to error_code is 0 because INT n, INT3, or INTO*)
            FI;
            IF gate not present
                THEN #NP(error_code(vector_number,1,EXT)); FI;
                (* idt operand to error_code set because vector is used *)
            IF task gate (* Specified in the selected interrupt table descriptor *)
                THEN GOTO TASK-GATE;
                ELSE GOTO TRAP-OR-INTERRUPT-GATE; (* PE = 1, trap/interrupt gate *)
            FI;
INT n/INTO/INT 3—Call to Interrupt Procedure

END;

IA-32e-MODE:

IF INTO and CS.L = 1 (64-bit mode)
THEN #UD;
FI;

IF ((vector_number « 4) + 15) is not in IDT limits
or selected IDT descriptor is not an interrupt-, or trap-gate type
THEN #GP(error_code(vector_number,1,EXT));
(* idt operand to error_code set because vector is used *)
FI;

IF software interrupt (* Generated by INT n, INT 3, or INTO *)
THEN
  IF gate DPL < CPL (* PE = 1, DPL < CPL, software interrupt *)
  THEN #GP(error_code(vector_number,1,0));
  (* ext operand to error_code set because vector is used *)
  (* idt operand to error_code set because vector is used *)
  FI;
FI;

IF gate not present
THEN #NP(error_code(vector_number,1,EXT));
(* idt operand to error_code is 0 because INT n, INT3, or INTO*)
FI;

GOTO TRAP-OR-INTERRUPT-GATE; (* Trap/interrupt gate *)

END;

TASK-GATE: (* PE = 1, task gate *)

Read TSS selector in task gate (IDT descriptor);
IF local/global bit is set to local or index not within GDT limits
THEN #GP(error_code(TSS selector,0,EXT)); FI;
(* idt operand to error_code set because selector is used *)
Access TSS descriptor in GDT;
IF TSS descriptor specifies that the TSS is busy (low-order 5 bits set to 00001)
THEN #GP(TSS selector,0,EXT)); FI;
(* idt operand to error_code set because selector is used *)
IF TSS not present
THEN #NP(TSS selector,0,EXT)); FI;
(* idt operand to error_code is 0 because selector is used *)
SWITCH-TASKS (with nesting) to TSS;
IF interrupt caused by fault with error code
THEN
  IF stack limit does not allow push of error code
  THEN #SS(EXT); FI;
  Push(error code);
FI;
IF EIP not within code segment limit
THEN #GP(EXT); FI;
END;
TRAP-OR-INTERRUPT-GATE:
Read new code-segment selector for trap or interrupt gate (IDT descriptor);
IF new code-segment selector is NULL
THEN #GP(EXT); FI; (* Error code contains NULL selector *)
IF new code-segment selector is not within its descriptor table limits
THEN #GP(error_code(new code-segment selector,0,EXT)); FI;
(* idt operand to error_code is 0 because selector is used *)
Read descriptor referenced by new code-segment selector;
IF descriptor does not indicate a code segment or new code-segment DPL > CPL
THEN #GP(error_code(new code-segment selector,0,EXT)); FI;
(* idt operand to error_code is 0 because selector is used *)
IF new code-segment descriptor is not present,
THEN #NP(error_code(new code-segment selector,0,EXT)); FI;
(* idt operand to error_code is 0 because selector is used *)
IF new code segment is non-conforming with DPL < CPL
THEN
IF VM = 0
THEN
GOTO INTER-PRIVILEGE-LEVEL-INTERRUPT;
(* PE = 1, VM = 0, interrupt or trap gate, nonconforming code segment,
DPL < CPL *)
ELSE (* VM = 1 *)
IF new code-segment DPL ≠ 0
THEN #GP(error_code(new code-segment selector,0,EXT));
(* idt operand to error_code is 0 because selector is used *)
GOTO INTERRUPT-FROM-VIRTUAL-8086-MODE; FI;
(* PE = 1, interrupt or trap gate, DPL < CPL, VM = 1 *)
FI;
ELSE (* PE = 1, interrupt or trap gate, DPL ≥ CPL *)
IF VM = 1
THEN #GP(error_code(new code-segment selector,0,EXT));
(* idt operand to error_code is 0 because selector is used *)
IF new code segment is conforming or new code-segment DPL = CPL
THEN
GOTO INTRA-PRIVILEGE-LEVEL-INTERRUPT;
ELSE (* PE = 1, interrupt or trap gate, nonconforming code segment, DPL > CPL *)
#GP(error_code(new code-segment selector,0,EXT));
(* idt operand to error_code is 0 because selector is used *)
FI;
FI;
END;
INTER-PRIVILEGE-LEVEL-INTERRUPT:
(* PE = 1, interrupt or trap gate, non-conforming code segment, DPL < CPL *)
IF (IA32_EFER.LMA = 0) (* Not IA-32e mode *)
THEN
(* Identify stack-segment selector for new privilege level in current TSS *)
IF current TSS is 32-bit
THEN
  TSSstackAddress ← (new code-segment DPL « 3) + 4;
  IF (TSSstackAddress + 5) > current TSS limit
  THEN #TS(error_code(current TSS selector,0,EXT)); Fl;
  (* idt operand to error_code is 0 because selector is used *)
  NewSS ← 2 bytes loaded from (TSS base + TSSstackAddress + 4);
  NewESP ← 4 bytes loaded from (TSS base + TSSstackAddress);
ELSE (* current TSS is 16-bit *)
  TSSstackAddress ← (new code-segment DPL « 2) + 2
  IF (TSSstackAddress + 3) > current TSS limit
  THEN #TS(error_code(current TSS selector,0,EXT)); Fl;
  (* idt operand to error_code is 0 because selector is used *)
  NewSS ← 2 bytes loaded from (TSS base + TSSstackAddress + 2);
  NewESP ← 2 bytes loaded from (TSS base + TSSstackAddress);
FI;
IF NewSS is NULL
THEN #TS(EXT); Fl;
IF NewSS index is not within its descriptor-table limits
or NewSS RPL ≠ new code-segment DPL
THEN #TS(error_code(NewSS,0,EXT)); Fl;
(* idt operand to error_code is 0 because selector is used *)
Read new stack-segment descriptor for NewSS in GDT or LDT;
IF new stack-segment DPL ≠ new code-segment DPL
or new stack-segment Type does not indicate writable data segment
THEN #TS(error_code(NewSS,0,EXT)); Fl;
(* idt operand to error_code is 0 because selector is used *)
IF NewSS is not present
THEN #SS(error_code(NewSS,0,EXT)); Fl;
(* idt operand to error_code is 0 because selector is used *)
ELSE (* IA-32e mode *)
IF IDT-gate IST = 0
THEN TSSstackAddress ← (new code-segment DPL « 3) + 4;
ELSE TSSstackAddress ← (IDT gate IST « 3) + 28;
FI;
IF (TSSstackAddress + 7) > current TSS limit
THEN #TS(error_code(current TSS selector,0,EXT)); Fl;
NewRSP ← 8 bytes loaded from (current TSS base + TSSStackAddress);
NewSS ← new code-segment DPL; (* NULL selector with RPL = new CPL *)
FI;

IF IDT gate is 32-bit
    THEN
        IF new stack does not have room for 24 bytes (error code pushed)
            or 20 bytes (no error code pushed)
            THEN #SS(error_code(NewSS,0,EXT)); FI;
        (* idt operand to error_code is 0 because selector is used *)
    FI
ELSE (64-bit IDT gate*)
    IF StackAddress is non-canonical
        THEN #SS(EXT); FI; (* Error code contains NULL selector *)
    FI;
FI;

IF (IA32_EFER.LMA = 0) (* Not IA-32e mode *)
    THEN
        IF instruction pointer from IDT gate is not within new code-segment limits
            THEN #GP(EXT); FI; (* Error code contains NULL selector *)
        ESP ← NewESP;
        SS ← NewSS; (* Segment descriptor information also loaded *)
    ELSE (* IA-32e mode *)
        IF instruction pointer from IDT gate contains a non-canonical address
            THEN #GP(EXT); FI; (* Error code contains NULL selector *)
        RSP ← NewRSP & FFFFFFFF0H;
        SS ← NewSS;
    FI;
FI;

IF IDT gate is 32-bit
    THEN
        CS:EIP ← Gate(CS:EIP); (* Segment descriptor information also loaded *)
    ELSE
        IF IDT gate 16-bit
            THEN
                CS:IP ← Gate(CS:IP);
                (* Segment descriptor information also loaded *)
            ELSE
ELSE (* 64-bit IDT gate *)
    CS:RIP ← Gate(CS:RIP);
    (* Segment descriptor information also loaded *)
    FI;
    FI;
IF IDT gate is 32-bit
    THEN
    Push(far pointer to old stack);
    (* Old SS and ESP, 3 words padded to 4 *)
    Push(EFLAGS);
    Push(far pointer to return instruction);
    (* Old CS and EIP, 3 words padded to 4 *)
    Push(ErrorCode); (* If needed, 4 bytes *)
    ELSE
    IF IDT gate 16-bit
    THEN
    Push(far pointer to old stack);
    (* Old SS and SP, 2 words *)
    Push(EFLAGS(15-0));
    Push(far pointer to return instruction);
    (* Old CS and IP, 2 words *)
    Push(ErrorCode); (* If needed, 2 bytes *)
    ELSE (* 64-bit IDT gate *)
    Push(far pointer to old stack);
    (* Old SS and SP, each an 8-byte push *)
    Push(RFLAGS); (* 8-byte push *)
    Push(far pointer to return instruction);
    (* Old CS and RIP, each an 8-byte push *)
    Push(ErrorCode); (* If needed, 8-bytes *)
    FI;
    FI;
CPL ← new code-segment DPL;
CS(RPL) ← CPL;
IF IDT gate is interrupt gate
    THEN IF ← 0 (* Interrupt flag set to 0, interrupts disabled *); FI;
    TF ← 0;
    VM ← 0;
    RF ← 0;
    NT ← 0;
END;
INTERRUPT-FROM-VIRTUAL-8086-MODE:
    (* Identify stack-segment selector for privilege level 0 in current TSS *)
    IF current TSS is 32-bit
THEN
    IF TSS limit < 9
        THEN #TS(error_code(current TSS selector,0,EXT)); Fl;
            (* idt operand to error_code is 0 because selector is used *)
    NewSS ← 2 bytes loaded from (current TSS base + 8);
    NewESP ← 4 bytes loaded from (current TSS base + 4);
ELSE (* current TSS is 16-bit *)
    IF TSS limit < 5
        THEN #TS(error_code(current TSS selector,0,EXT)); Fl;
            (* idt operand to error_code is 0 because selector is used *)
    NewSS ← 2 bytes loaded from (current TSS base + 4);
    NewESP ← 2 bytes loaded from (current TSS base + 2);
FI;
IF NewSS is NULL
    THEN #TS(EXT); Fl; (* Error code contains NULL selector *)
IF NewSS index is not within its descriptor table limits
    or NewSS RPL ≠ 0
    THEN #TS(error_code(NewSS,0,EXT)); Fl;
        (* idt operand to error_code is 0 because selector is used *)
Read new stack-segment descriptor for NewSS in GDT or LDT;
IF new stack-segment DPL ≠ 0 or stack segment does not indicate writable data segment
    THEN #TS(error_code(NewSS,0,EXT)); Fl;
        (* idt operand to error_code is 0 because selector is used *)
IF new stack segment not present
    THEN #SS(error_code(NewSS,0,EXT)); Fl;
        (* idt operand to error_code is 0 because selector is used *)
IF IDT gate is 32-bit
    THEN
        IF new stack does not have room for 40 bytes (error code pushed)
            or 36 bytes (no error code pushed)
            THEN #SS(error_code(NewSS,0,EXT)); Fl;
                (* idt operand to error_code is 0 because selector is used *)
    ELSE (* IDT gate is 16-bit)
        IF new stack does not have room for 20 bytes (error code pushed)
            or 18 bytes (no error code pushed)
            THEN #SS(error_code(NewSS,0,EXT)); Fl;
                (* idt operand to error_code is 0 because selector is used *)
FI;
IF instruction pointer from IDT gate is not within new code-segment limits
    THEN #GP(EXT); Fl; (* Error code contains NULL selector *)
tempEFLAGS ← EFLAGS;
VM ← 0;
TF ← 0;
INT n/INTO/INT 3—Call to Interrupt Procedure

RF ← 0;
NT ← 0;
IF service through interrupt gate
    THEN IF = 0; FI;
TempSS ← SS;
TempESP ← ESP;
SS ← NewSS;
ESP ← NewESP;
(* Following pushes are 16 bits for 16-bit IDT gates and 32 bits for 32-bit IDT gates; Segment selector pushes in 32-bit mode are padded to two words *)
Push(GS);
Push(FS);
Push(DS);
Push(ES);
Push(TempSS);
Push(TempESP);
Push(TempEFlags);
Push(CS);
Push(EIP);
GS ← 0; (* Segment registers made NULL, invalid for use in protected mode *)
FS ← 0;
DS ← 0;
ES ← 0;
CS:IP ← Gate(CS); (* Segment descriptor information also loaded *)
IF OperandSize = 32
    THEN
        EIP ← Gate(instruction pointer);
    ELSE (* OperandSize is 16 *)
        EIP ← Gate(instruction pointer) AND 0000FFFFH;
    FI;
(* Start execution of new routine in Protected Mode *)
END;
INTRA-PRIVILEGE-LEVEL-INTERRUPT:
(* PE = 1, DPL = CPL or conforming segment *)
IF IA32_EFER.LMA = 1 (* IA-32e mode *)
    IF IDT-descriptor IST ≠ 0
        THEN
            TSSstackAddress ← (IDT-descriptor IST × 3) + 28;
            IF (TSSstackAddress + 7) > TSS limit
                THEN #TS(error_code(current TSS selector,0,EXT)); FI;
                (* idt operand to error_code is 0 because selector is used *)
            NewRSP ← 8 bytes loaded from (current TSS base + TSSstackAddress);
        FI;
    FI;
IF 32-bit gate (* implies IA32_EFER.LMA = 0 *)
   THEN
       IF current stack does not have room for 16 bytes (error code pushed)
        or 12 bytes (no error code pushed)
           THEN #SS(EXT); Fl; (* Error code contains NULL selector *)
       ELSE IF 16-bit gate (* implies IA32_EFER.LMA = 0 *)
           IF current stack does not have room for 8 bytes (error code pushed)
            or 6 bytes (no error code pushed)
               THEN #SS(EXT); Fl; (* Error code contains NULL selector *)
           ELSE (* IA32_EFER.LMA = 1, 64-bit gate*)
               IF NewRSP contains a non-canonical address
                  THEN #SS(EXT); (* Error code contains NULL selector *)
               FI;
       FI;
   FI;
IF (IA32_EFER.LMA = 0) (* Not IA-32e mode *)
   THEN
       IF instruction pointer from IDT gate is not within new code-segment limit
          THEN #GP(EXT); Fl; (* Error code contains NULL selector *)
       ELSE
           IF instruction pointer from IDT gate contains a non-canonical address
              THEN #GP(EXT); Fl; (* Error code contains NULL selector *)
           RSP ← NewRSP & FFFFFFFFFFFFFFF0H;
       FI;
   FI;
IF IDT gate is 32-bit (* implies IA32_EFER.LMA = 0 *)
   THEN
       Push (EFLAGS);
       Push (far pointer to return instruction); (* 3 words padded to 4 *)
       CS:EIP ← Gate(CS:EIP); (* Segment descriptor information also loaded *)
       Push (ErrorCode); (* If any *)
   ELSE
       IF IDT gate is 16-bit (* implies IA32_EFER.LMA = 0 *)
          THEN
              Push (FLAGS);
              Push (far pointer to return location); (* 2 words *)
              CS:IP ← Gate(CS:IP);
              (* Segment descriptor information also loaded *)
              Push (ErrorCode); (* If any *)
       ELSE (* IA32_EFER.LMA = 1, 64-bit gate*)
           Push(far pointer to old stack);
           (* Old SS and SP, each an 8-byte push *)
           Push(RFLAGS); (* 8-byte push *)
           Push(far pointer to return instruction);
           (* Old CS and RIP, each an 8-byte push *)
Push(ErrorCode); (* If needed, 8 bytes *)
CS: RIP ← GATE(CS:RIP);
(* Segment descriptor information also loaded *)
Fi;
Fi;
CS(RPL) ← CPL;
IF IDT gate is interrupt gate
    THEN IF ← 0; Fi; (* Interrupt flag set to 0; interrupts disabled *)
    TF ← 0;
    NT ← 0;
    VM ← 0;
    RF ← 0;
END;

Flags Affected
The EFLAGS register is pushed onto the stack. The IF, TF, NT, AC, RF, and VM flags may be cleared, depending on the mode of operation of the processor when the INT instruction is executed (see the “Operation” section). If the interrupt uses a task gate, any flags may be set or cleared, controlled by the EFLAGS image in the new task’s TSS.

Protected Mode Exceptions
#GP(error_code) If the instruction pointer in the IDT or in the interrupt-, trap-, or task gate is beyond the code segment limits.
If the segment selector in the interrupt-, trap-, or task gate is NULL.
If an interrupt-, trap-, or task gate, code segment, or TSS segment selector index is outside its descriptor table limits.
If the interrupt vector number is outside the IDT limits.
If an IDT descriptor is not an interrupt-, trap-, or task-descriptor.
If an interrupt is generated by the INT n, INT 3, or INTO instruction and the DPL of an interrupt-, trap-, or task-descriptor is less than the CPL.
If the segment selector in an interrupt- or trap-gate does not point to a segment descriptor for a code segment.
If the segment selector for a TSS has its local/global bit set for local.
If a TSS segment descriptor specifies that the TSS is busy or not available.

#SS(error_code) If pushing the return address, flags, or error code onto the stack exceeds the bounds of the stack segment and no stack switch occurs.
If the SS register is being loaded and the segment pointed to is marked not present.
If pushing the return address, flags, error code, or stack segment pointer exceeds the bounds of the new stack segment when a stack switch occurs.

#NP(error_code) If code segment, interrupt-, trap-, or task gate, or TSS is not present.
#TS(error_code) If the RPL of the stack segment selector in the TSS is not equal to the DPL of the code segment being accessed by the interrupt or trap gate.
If the stack segment for the TSS is not a writable data segment.
If segment-selector index for stack segment is outside descriptor table limits.

#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.
#AC(EXT) If alignment checking is enabled, the gate DPL is 3, and a stack push is unaligned.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the interrupt vector number is outside the IDT limits.

#SS If stack limit violation on push.
If pushing the return address, flags, or error code onto the stack exceeds the bounds of the stack segment.

Virtual-8086 Mode Exceptions

#GP(error_code) (For INT n, INTO, or BOUND instruction) If the IOPL is less than 3 or the DPL of the interrupt-, trap-, or task-gate descriptor is not equal to 3.
If the instruction pointer in the IDT or in the interrupt-, trap-, or task gate is beyond the code segment limits.
If a interrupt-, trap-, or task gate, code segment, or TSS segment selector index is outside its descriptor table limits.
If the interrupt vector number is outside the IDT limits.
If an IDT descriptor is not an interrupt-, trap-, or task-descriptor.
If an interrupt is generated by the INT $n$ instruction and the DPL of an interrupt-, trap-, or task-descriptor is less than the CPL.
If the segment selector in an interrupt- or trap-gate does not point to a segment descriptor for a code segment.
If the segment selector for a TSS has its local/global bit set for local.

### #SS(error_code)
If the SS register is being loaded and the segment pointed to is marked not present.
If pushing the return address, flags, error code, stack segment pointer, or data segments exceeds the bounds of the stack segment.

### #NP(error_code)
If code segment, interrupt-, trap-, or task gate, or TSS is not present.

### #TS(error_code)
If the RPL of the stack segment selector in the TSS is not equal to the DPL of the code segment being accessed by the interrupt or trap gate.
If DPL of the stack segment descriptor for the TSS’s stack segment is not equal to the DPL of the code segment descriptor for the interrupt or trap gate.
If the stack segment selector in the TSS is NULL.
If the stack segment for the TSS is not a writable data segment.
If segment-selector index for stack segment is outside descriptor table limits.

### #PF(fault-code)
If a page fault occurs.

### #BP
If the INT 3 instruction is executed.

### #OF
If the INTO instruction is executed and the OF flag is set.

### #UD
If the LOCK prefix is used.

### #AC(EXT)
If alignment checking is enabled, the gate DPL is 3, and a stack push is unaligned.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

### #GP(error_code)
If the instruction pointer in the 64-bit interrupt gate or 64-bit trap gate is non-canonical.
If the segment selector in the 64-bit interrupt or trap gate is NULL.
If the interrupt vector number is outside the IDT limits.
If the interrupt vector number points to a gate which is in non-canonical space.
If the interrupt vector number points to a descriptor which is not a 64-bit interrupt gate or 64-bit trap gate.
If the descriptor pointed to by the gate selector is outside the descriptor table limit.
If the descriptor pointed to by the gate selector is in non-canonical space.
If the descriptor pointed to by the gate selector is not a code segment.
If the descriptor pointed to by the gate selector doesn’t have the L-bit set, or has both the L-bit and D-bit set.
If the descriptor pointed to by the gate selector has DPL > CPL.

#SS(error_code) If a push of the old EFLAGS, CS selector, EIP, or error code is in non-canonical space with no stack switch.
If a push of the old SS selector, ESP, EFLAGS, CS selector, EIP, or error code is in non-canonical space on a stack switch (either CPL change or no-CPL with IST).

#NP(error_code) If the 64-bit interrupt-gate, 64-bit trap-gate, or code segment is not present.

#TS(error_code) If an attempt to load RSP from the TSS causes an access to non-canonical space.
If the RSP from the TSS is outside descriptor table limits.

#PF(fault-code) If a page fault occurs.

#UD If the LOCK prefix is used.

#AC(EXT) If alignment checking is enabled, the gate DPL is 3, and a stack push is unaligned.
INVD—Invalidate Internal Caches

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 08</td>
<td>INVD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Flush internal caches; initiate flushing of external caches.</td>
</tr>
</tbody>
</table>

NOTES:
* See the IA-32 Architecture Compatibility section below.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Invalidates (flushes) the processor’s internal caches and issues a special-function bus cycle that directs external caches to also flush themselves. Data held in internal caches is not written back to main memory.

After executing this instruction, the processor does not wait for the external caches to complete their flushing operation before proceeding with instruction execution. It is the responsibility of hardware to respond to the cache flush signal.

The INVD instruction is a privileged instruction. When the processor is running in protected mode, the CPL of a program or procedure must be 0 to execute this instruction.

Use this instruction with care. Data cached internally and not written back to main memory will be lost. Unless there is a specific requirement or benefit to flushing caches without writing back modified cache lines (for example, testing or fault recovery where cache coherency with main memory is not a concern), software should use the WBINVD instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

IA-32 Architecture Compatibility

The INVD instruction is implementation dependent; it may be implemented differently on different families of Intel 64 or IA-32 processors. This instruction is not supported on IA-32 processors earlier than the Intel486 processor.

Operation

Flush(InternalCaches);
SignalFlush(ExternalCaches);
Continue (* Continue execution * )
Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the current privilege level is not 0.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) The INVD instruction cannot be executed in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
INSTRUCTION SET REFERENCE, A-L

INVLPGL—Invalidate TLB Entry

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01/7</td>
<td>INVLPGL m</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Invalidate TLB Entry for page that contains m.</td>
</tr>
</tbody>
</table>

NOTES:
* See the IA-32 Architecture Compatibility section below.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Invalidate (flushes) the translation lookaside buffer (TLB) entry specified with the source operand. The source operand is a memory address. The processor determines the page that contains that address and flushes the TLB entry for that page.

The INVLPGL instruction is a privileged instruction. When the processor is running in protected mode, the CPL of a program or procedure must be 0 to execute this instruction.

The INVLPGL instruction normally flushes the TLB entry only for the specified page; however, in some cases, it flushes the entire TLB. See “MOV—Move to/from Control Registers” in this chapter for further information on operations that flush the TLB.

This instruction’s operation is the same in all non-64-bit modes. It also operates the same in 64-bit mode, except if the memory address is in non-canonical form. In this case, INVLPGL is the same as a NOP.

IA-32 Architecture Compatibility

The INVLPGL instruction is implementation dependent, and its function may be implemented differently on different families of Intel 64 or IA-32 processors. This instruction is not supported on IA-32 processors earlier than the Intel486 processor.

Operation

Flush(RelevantTLBEntries);
Continue; (* Continue execution *)

Flags Affected

None.
**Protected Mode Exceptions**

- **#GP(0)**: If the current privilege level is not 0.
- **#UD**: Operand is a register.
  - If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#UD**: Operand is a register.
  - If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

- **#GP(0)**: The INVLPG instruction cannot be executed at the virtual-8086 mode.

**64-Bit Mode Exceptions**

- **#GP(0)**: If the current privilege level is not 0.
- **#UD**: Operand is a register.
  - If the LOCK prefix is used.
INVPCID—Invalidate Process-Context Identifier

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 82 /r INVPCID r32, m128</td>
<td>RM</td>
<td>NE/V</td>
<td>INVPCID</td>
<td>Invalidates entries in the TLBs and paging-structure caches based on invalidation type in r32 and descriptor in m128.</td>
</tr>
<tr>
<td>66 0F 38 82 /r INVPCID r64, m128</td>
<td>RM</td>
<td>V/NE</td>
<td>INVPCID</td>
<td>Invalidates entries in the TLBs and paging-structure caches based on invalidation type in r64 and descriptor in m128.</td>
</tr>
</tbody>
</table>

Description

Invokes mapping in the translation lookaside buffers (TLBs) and paging-structure caches based on process-context identifier (PCID). (See Section 4.10, "Caching Translation Information," in Intel 64 and IA-32 Architecture Software Developer’s Manual, Volume 3A.) Invalidation is based on the INVPCID type specified in the register operand and the INVPCID descriptor specified in the memory operand.

Outside 64-bit mode, the register operand is always 32 bits, regardless of the value of CS.D. In 64-bit mode the register operand has 64 bits.

There are four INVPCID types currently defined:

- **Individual-address invalidation:** If the INVPCID type is 0, the logical processor invalidates mappings—except global translations—for the linear address and PCID specified in the INVPCID descriptor. In some cases, the instruction may invalidate global translations or mappings for other linear addresses (or other PCIDs) as well.

- **Single-context invalidation:** If the INVPCID type is 1, the logical processor invalidates all mappings—associated with the PCID specified in the INVPCID descriptor. In some cases, the instruction may invalidate global translations or mappings for other PCIDs as well.

- **All-context invalidation, including global translations:** If the INVPCID type is 2, the logical processor invalidates all mappings—including global translations—associated with any PCID.
• All-context invalidation: If the INVPCID type is 3, the logical processor invalidates all mappings—except global translations—associated with any PCID. In some case, the instruction may invalidate global translations as well.

The INVPCID descriptor comprises 128 bits and consists of a PCID and a linear address as shown in Figure 3-23. For INVPCID type 0, the processor uses the full 64 bits of the linear address even outside 64-bit mode; the linear address is not used for other INVPCID types.

\[
\begin{array}{cccc}
127 & 64 & 63 & 12 \quad 11 \quad 0 \\
\hline
\text{Linear Address} & \text{Reserved (must be zero)} & \text{PCID}
\end{array}
\]

Figure 3-23. INVPCID Descriptor

If CR4.PCIDE = 0, a logical processor does not cache information for any PCID other than 000H. In this case, executions with INVPCID types 0 and 1 are allowed only if the PCID specified in the INVPCID descriptor is 000H; executions with INVPCID types 2 and 3 invalidate mappings only for PCID 000H. Note that CR4.PCIDE must be 0 outside 64-bit mode (see Chapter 4.10.1, “Process-Context Identifiers (PCIDs),” of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A).

**Operation**

INVPCID_TYPE ← value of register operand;          // must be in the range of 0–3
INVPCID_DESC ← value of memory operand;
CASE INVPCID_TYPE OF
  0:          // individual-address invalidation
    PCID ← INVPCID_DESC[11:0];
    L_ADDR ← INVPCID_DESC[127:64];
    Invalidate mappings for L_ADDR associated with PCID except global translations;
    BREAK;
  1:          // single PCID invalidation
    PCID ← INVPCID_DESC[11:0];
    Invalidate all mappings associated with PCID except global translations;
    BREAK;
  2:          // all PCID invalidation including global translations
    Invalidate all mappings for all PCIDs, including global translations;
    BREAK;
  3:          // all PCID invalidation retaining global translations
    Invalidate all mappings for all PCIDs except global translations;
BREAK;
ESAC;

**Intel C/C++ Compiler Intrinsic Equivalent**

INVPCID:  void __invpcid(unsigned __int32 type, void * descriptor);

**SIMD Floating-Point Exceptions**

None

**Protected Mode Exceptions**

- **#GP(0)**: If the current privilege level is not 0.
- If the memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register contains an unusable segment.
- If the source operand is located in an execute-only code segment.
- If an invalid type is specified in the register operand, i.e., INVPCID_TYPE > 3.
- If bits 63:12 of INVPCID_DESC are not all zero.
- If INVPCID_TYPE is either 0 or 1 and INVPCID_DESC[11:0] is not zero.
- If INVPCID_TYPE is 0 and the linear address in INVPCID_DESC[127:64] is not canonical.
- **#PF(fault-code)**: If a page fault occurs in accessing the memory operand.
- **#SS(0)**: If the memory operand effective address is outside the SS segment limit.
- If the SS register contains an unusable segment.
- **#UD**: If CPUID.(EAX=07H, ECX=0H):EBX.INVPCID (bit 10) = 0.
- If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP**: If an invalid type is specified in the register operand, i.e., INVPCID_TYPE > 3.
- If bits 63:12 of INVPCID_DESC are not all zero.
- If INVPCID_TYPE is either 0 or 1 and INVPCID_DESC[11:0] is not zero.
- If INVPCID_TYPE is 0 and the linear address in INVPCID_DESC[127:64] is not canonical.
- **#UD**: If CPUID.(EAX=07H, ECX=0H):EBX.INVPCID (bit 10) = 0.
INSTRUCTION SET REFERENCE, A-L

If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) The INVPCID instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the current privilege level is not 0.
    If the memory operand is in the CS, DS, ES, FS, or GS segments and the memory address is in a non-canonical form.
    If an invalid type is specified in the register operand, i.e., INVPCID_TYPE > 3.
    If bits 63:12 of INVPCID_DESC are not all zero.
    If CR4.PCIDE=0, INVPCID_TYPE is either 0 or 1, and INVPCID_DESC[11:0] is not zero.
    If INVPCID_TYPE is 0 and the linear address in INVPCID_DESC[127:64] is not canonical.
#PF(fault-code) If a page fault occurs in accessing the memory operand.
#SS(0) If the memory destination operand is in the SS segment and the memory address is in a non-canonical form.
#UD If the LOCK prefix is used.
    If CPUID.(EAX=07H, ECX=0H):EBX.INVPCID (bit 10) = 0.
IRET/IRETD—Interrupt Return

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CF</td>
<td>IRET</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Interrupt return (16-bit operand size).</td>
</tr>
<tr>
<td>CF</td>
<td>IRETD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Interrupt return (32-bit operand size).</td>
</tr>
<tr>
<td>REX.W + CF</td>
<td>IRETQ</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Interrupt return (64-bit operand size).</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Returns program control from an exception or interrupt handler to a program or procedure that was interrupted by an exception, an external interrupt, or a software-generated interrupt. These instructions are also used to perform a return from a nested task. (A nested task is created when a CALL instruction is used to initiate a task switch or when an interrupt or exception causes a task switch to an interrupt or exception handler.) See the section titled "Task Linking" in Chapter 7 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*.

IRET and IRETD are mnemonics for the same opcode. The IRETD mnemonic (interrupt return double) is intended for use when returning from an interrupt when using the 32-bit operand size; however, most assemblers use the IRET mnemonic interchangeably for both operand sizes.

In Real-Address Mode, the IRET instruction performs a far return to the interrupted program or procedure. During this operation, the processor pops the return instruction pointer, return code segment selector, and EFLAGS image from the stack to the EIP, CS, and EFLAGS registers, respectively, and then resumes execution of the interrupted program or procedure.

In Protected Mode, the action of the IRET instruction depends on the settings of the NT (nested task) and VM flags in the EFLAGS register and the VM flag in the EFLAGS image stored on the current stack. Depending on the setting of these flags, the processor performs the following types of interrupt returns:

- Return from virtual-8086 mode.
- Return to virtual-8086 mode.
- Intra-privilege level return.
- Inter-privilege level return.
- Return from nested task (task switch).
If the NT flag (EFLAGS register) is cleared, the IRET instruction performs a far return from the interrupt procedure, without a task switch. The code segment being returned to must be equally or less privileged than the interrupt handler routine (as indicated by the RPL field of the code segment selector popped from the stack).

As with a real-address mode interrupt return, the IRET instruction pops the return instruction pointer, return code segment selector, and EFLAGS image from the stack to the EIP, CS, and EFLAGS registers, respectively, and then resumes execution of the interrupted program or procedure. If the return is to another privilege level, the IRET instruction also pops the stack pointer and SS from the stack, before resuming program execution. If the return is to virtual-8086 mode, the processor also pops the data segment registers from the stack.

If the NT flag is set, the IRET instruction performs a task switch (return) from a nested task (a task called with a CALL instruction, an interrupt, or an exception) back to the calling or interrupted task. The updated state of the task executing the IRET instruction is saved in its TSS. If the task is re-entered later, the code that follows the IRET instruction is executed.

If the NT flag is set and the processor is in IA-32e mode, the IRET instruction causes a general protection exception.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.W prefix promotes operation to 64 bits (IRETQ). See the summary chart at the beginning of this section for encoding data and limits.

See “Changes to Instruction Behavior in VMX Non-Root Operation” in Chapter 25 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, for more information about the behavior of this instruction in VMX non-root operation.

**Operation**

IF PE = 0
THEN
    GOTO REAL-ADDRESS-MODE;
ELSE
    IF (IA32_EFER.LMA = 0)
        THEN (* Protected mode *)
            GOTO PROTECTED-MODE;
        ELSE (* IA-32e mode *)
            GOTO IA-32e-MODE;
    FI;
FI;
REAL-ADDRESS-MODE;
IF OperandsSize = 32
THEN
    IF top 12 bytes of stack not within stack limits
        THEN #SS; FI;
IRET/IRETD—Interrupt Return

tempEIP ← 4 bytes at end of stack
IF tempEIP[31:16] is not zero THEN #GP(0); FI;
EIP ← Pop();
CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded *)
tempEFLAGS ← Pop();
EFLAGS ← (tempEFLAGS AND 257FD5H) OR (EFLAGS AND 1A0000H);
ELSE (* OperandSize = 16 *)
IF top 6 bytes of stack are not within stack limits
THEN #SS; FI;
EIP ← Pop(); (* 16-bit pop; clear upper 16 bits *)
CS ← Pop(); (* 16-bit pop *)
EFLAGS[15:0] ← Pop();
END;

PROTECTED-MODE:
IF VM = 1 (* Virtual-8086 mode: PE = 1, VM = 1 *)
THEN
GOTO RETURN-FROM-VIRTUAL-8086-MODE; (* PE = 1, VM = 1 *)
FI;
IF NT = 1
THEN
GOTO TASK-RETURN; (* PE = 1, VM = 0, NT = 1 *)
FI;
IF OperandSize = 32
THEN
IF top 12 bytes of stack not within stack limits
THEN #SS(0); FI;
tempEIP ← Pop();
tempCS ← Pop();
tempEFLAGS ← Pop();
ELSE (* OperandSize = 16 *)
IF top 6 bytes of stack are not within stack limits
THEN #SS(0); FI;
tempEIP ← Pop();
tempCS ← Pop();
tempEFLAGS ← Pop();
tempEIP ← tempEIP AND FFFFH;
tempEFLAGS ← tempEFLAGS AND FFFFH;
FI;
IF tempEFLAGS(VM) = 1 and CPL = 0
THEN
GOTO RETURN-TO-VIRTUAL-8086-MODE;
ELSE
INSTRUCTION SET REFERENCE, A-L

GOTO PROTECTED-MODE-RETURN;
FI;
IA-32e-MODE:
IF NT = 1
THEN #GP(0);
ELSE IF OperandSize = 32
THEN
IF top 12 bytes of stack not within stack limits
THEN #SS(0); FI;
tempEIP ← Pop();
tempCS ← Pop();
tempEFLAGS ← Pop();
ELSE IF OperandSize = 16
THEN
IF top 6 bytes of stack are not within stack limits
THEN #SS(0); FI;
tempEIP ← Pop();
tempCS ← Pop();
tempEFLAGS ← Pop();
tempEIP ← tempEIP AND FFFFH;
tempEFLAGS ← tempEFLAGS AND FFFFH;
FI;
ELSE (* OperandSize = 64 *)
THEN
tempRIP ← Pop();
tempCS ← Pop();
tempEFLAGS ← Pop();
tempRSP ← Pop();
tempSS ← Pop();
FI;
GOTO IA-32e-MODE-RETURN;

RETURN-FROM-VIRTUAL-8086-MODE:
(* Processor is in virtual-8086 mode when IRET is executed and stays in virtual-8086 mode *)
IF IOPL = 3 (* Virtual mode: PE = 1, VM = 1, IOPL = 3 *)
THEN IF OperandSize = 32
THEN
IF top 12 bytes of stack not within stack limits
THEN #SS(0); FI;
IF instruction pointer not within code segment limits
THEN #GP(0); FI;
EIP ← Pop();
CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded *)
EFLAGS ← Pop();
IRET/IRETD—Interrupt Return

(* VM, IOPL,VIP and VIF EFLAG bits not modified by pop *)
ELSE (* Operandsize = 16 *)
IF top 6 bytes of stack are not within stack limits
    THEN #SS(0); FI;
IF instruction pointer not within code segment limits
    THEN #GP(0); FI;
    EIP ← Pop();
    EIP ← EIP AND 0000FFFFH;
    CS ← Pop(); (* 16-bit pop *)
    EFLAGS[15:0] ← Pop(); (* IOPL in EFLAGS not modified by pop *)
    FI;
ELSE
    #GP(0); (* Trap to virtual-8086 monitor: PE = 1, VM = 1, IOPL < 3 *)
    FI;
END;

RETURN-TO-VIRTUAL-8086-MODE:
(* Interrupted procedure was in virtual-8086 mode: PE = 1, CPL=0, VM = 1 in flag image *)
IF top 24 bytes of stack are not within stack segment limits
    THEN #SS(0); FI;
IF instruction pointer not within code segment limits
    THEN #GP(0); FI;
    CS ← tempCS;
    EIP ← tempEIP & FFFFH;
    EFLAGS ← tempEFLAGS;
    TempESP ← Pop();
    TempSS ← Pop();
    ES ← Pop(); (* Pop 2 words; throw away high-order word *)
    DS ← Pop(); (* Pop 2 words; throw away high-order word *)
    FS ← Pop(); (* Pop 2 words; throw away high-order word *)
    GS ← Pop(); (* Pop 2 words; throw away high-order word *)
    SS:ESP ← TempSS:TempESP;
    CPL ← 3;
    (* Resume execution in Virtual-8086 mode *)
END;

TASK-RETURN: (* PE = 1, VM = 0, NT = 1 *)
Read segment selector in link field of current TSS;
IF local/global bit is set to local
or index not within GDT limits
    THEN #TS (TSS selector); FI;
Access TSS for task specified in link field of current TSS;
IF TSS descriptor type is not TSS or if the TSS is marked not busy
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THEN #TS (TSS selector); Fl;
IF TSS not present
THEN #NP(TSS selector); Fl;
SWITCH-TASKS (without nesting) to TSS specified in link field of current TSS;
Mark the task just abandoned as NOT BUSY;
IF EIP is not within code segment limit
THEN #GP(0); Fl;
END;

PROTECTED-MODE-RETURN: (* PE = 1 *)
IF return code segment selector is NULL
THEN GP(0); Fl;
IF return code segment selector addresses descriptor beyond descriptor table limit
THEN GP(selector); Fl;
Read segment descriptor pointed to by the return code segment selector;
IF return code segment descriptor is not a code segment
THEN #GP(selector); Fl;
IF return code segment selector RPL < CPL
THEN #GP(selector); Fl;
IF return code segment descriptor is conforming
and return code segment DPL > return code segment selector RPL
THEN #GP(selector); Fl;
IF return code segment descriptor is not present
THEN #NP(selector); Fl;
IF return code segment selector RPL > CPL
THEN GOTO RETURN-OUTER-PRIVILEGE-LEVEL;
ELSE GOTO RETURN-TO-SAME-PRIVILEGE-LEVEL; Fl;
END;

RETURN-TO-SAME-PRIVILEGE-LEVEL: (* PE = 1, RPL = CPL *)
IF new mode ≠ 64-Bit Mode
THEN
    IF tempEIP is not within code segment limits
        THEN #GP(0); Fl;
        EIP ← tempEIP;
    ELSE (* new mode = 64-bit mode *)
        IF tempRIP is non-canonical
            THEN #GP(0); Fl;
            RIP ← tempRIP;
    Fl;
CS ← tempCS; (* Segment descriptor information also loaded *)
EFLAGS (CF, PF, AF, ZF, SF, TF, DF, OF, NT) ← tempEFLAGS;
IF OperandSize = 32 or OperandSize = 64
THEN EFLAGS(RF, AC, ID) ← tempEFLAGS; FI;
IF CPL ≤ IOPL
THEN EFLAGS(IF) ← tempEFLAGS; FI;
IF CPL = 0
THEN (* VM = 0 in flags image *)
EFLAGS(IOPL) ← tempEFLAGS;
IF OperandSize = 32 or OperandSize = 64
THEN EFLAGS(VIF, VIP) ← tempEFLAGS; FI;
FI;
END;
RETURN-TO-OUTER-PRIVILEGE-LEVEL:
IF OperandSize = 32
THEN
  IF top 8 bytes on stack are not within limits
  THEN #SS(0); FI;
  ELSE (* OperandSize = 16 *)
  IF top 4 bytes on stack are not within limits
  THEN #SS(0); FI;
FI;
Read return segment selector;
IF stack segment selector is NULL
THEN #GP(0); FI;
IF return stack segment selector index is not within its descriptor table limits
THEN #GP(SSselector); FI;
Read segment descriptor pointed to by return segment selector;
IF stack segment selector RPL ≠ RPL of the return code segment selector
or the stack segment descriptor does not indicate a writable data segment;
or the stack segment DPL ≠ RPL of the return code segment selector
THEN #GP(SS selector); FI;
IF stack segment is not present
THEN #SS(SS selector); FI;
IF new mode ≠ 64-Bit Mode
THEN
  IF tempEIP is not within code segment limits
  THEN #GP(0); FI;
  EIP ← tempEIP;
  ELSE (* new mode = 64-bit mode *)
  IF tempRIP is non-canonical
  THEN #GP(0); FI;
  RIP ← tempRIP;
FI;
CS ← tempCS;
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EFLAGS (CF, PF, AF, ZF, SF, TF, DF, OF, NT) ← tempEFLAGS;
IF OperandSize = 32
    THEN EFLAGS(RF, AC, ID) ← tempEFLAGS; Fl;
IF CPL ≤ IOPL
    THEN EFLAGS(IF) ← tempEFLAGS; Fl;
IF CPL = 0
    THEN
        EFLAGS(IOPL) ← tempEFLAGS;
        IF OperandSize = 32
            THEN EFLAGS(VM, VIF, VIP) ← tempEFLAGS; Fl;
        IF OperandSize = 64
            THEN EFLAGS(VIF, VIP) ← tempEFLAGS; Fl;
    Fl;
CPL ← RPL of the return code segment selector;
FOR each of segment register (ES, FS, GS, and DS)
    DO
        IF segment register points to data or non-conforming code segment
            and CPL > segment descriptor DPL (* Stored in hidden part of segment register *)
            THEN (* Segment register invalid *)
                SegmentSelector ← 0; (* NULL segment selector *)
        FI;
    OD;
END;

IA-32e-MODE-RETURN: (* IA32_EFER.LMA = 1, PE = 1 *)
    IF ( (return code segment selector is NULL) or (return RIP is non-canonical) or
        (SS selector is NULL going back to compatibility mode) or
        (SS selector is NULL going back to CPL3 64-bit mode) or
        (RPL <> CPL going back to non-CPL3 64-bit mode for a NULL SS selector) )
        THEN GP(0); Fl;
    IF return code segment selector addresses descriptor beyond descriptor table limit
        THEN GP(selector); Fl;
    Read segment descriptor pointed to by the return code segment selector;
    IF return code segment descriptor is not a code segment
        THEN #GP(selector); Fl;
    IF return code segment selector RPL < CPL
        THEN #GP(selector); Fl;
    IF return code segment descriptor is conforming
        and return code segment DPL > return code segment selector RPL
        THEN #GP(selector); Fl;
    IF return code segment descriptor is not present
        THEN #NP(selector); Fl;
    IF return code segment selector RPL > CPL
THEN GOTO RETURN-OUTER-PRIVILEGE-LEVEL;
ELSE GOTO RETURN-TO-SAME-PRIVILEGE-LEVEL; FI;
END;

Flags Affected
All the flags and fields in the EFLAGS register are potentially modified, depending on the mode of operation of the processor. If performing a return from a nested task to a previous task, the EFLAGS register will be modified according to the EFLAGS image stored in the previous task’s TSS.

Protected Mode Exceptions
#GP(0) If the return code or stack segment selector is NULL.
If the return instruction pointer is not within the return code segment limit.
#GP(selector) If a segment selector index is outside its descriptor table limits.
If the return code segment selector RPL is greater than the CPL.
If the DPL of a conforming-code segment is greater than the return code segment selector RPL.
If the DPL for a nonconforming-code segment is not equal to the RPL of the code segment selector.
If the stack segment descriptor DPL is not equal to the RPL of the return code segment selector.
If the stack segment is not a writable data segment.
If the stack segment selector RPL is not equal to the RPL of the return code segment selector.
If the segment descriptor for a code segment does not indicate it is a code segment.
If the segment selector for a TSS has its local/global bit set for local.
If a TSS segment descriptor specifies that the TSS is not busy.
If a TSS segment descriptor specifies that the TSS is not available.
#SS(0) If the top bytes of stack are not within stack limits.
#NP(selector) If the return code or stack segment is not present.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference occurs when the CPL is 3 and alignment checking is enabled.
#UD If the LOCK prefix is used.
Real-Address Mode Exceptions
#GP If the return instruction pointer is not within the return code segment limit.
#SS If the top bytes of stack are not within stack limits.

Virtual-8086 Mode Exceptions
#GP(0) If the return instruction pointer is not within the return code segment limit.
   IF IOPL not equal to 3.
#PF(fault-code) If a page fault occurs.
#SS(0) If the top bytes of stack are not within stack limits.
#AC(0) If an unaligned memory reference occurs and alignment checking is enabled.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
#GP(0) If EFLAGS.NT[bit 14] = 1.
Other exceptions same as in Protected Mode.

64-Bit Mode Exceptions
#GP(0) If EFLAGS.NT[bit 14] = 1.
   If the return code segment selector is NULL.
   If the stack segment selector is NULL going back to compatibility mode.
   If the stack segment selector is NULL going back to CPL3 64-bit mode.
   If a NULL stack segment selector RPL is not equal to CPL going back to non-CPL3 64-bit mode.
   If the return instruction pointer is not within the return code segment limit.
   If the return instruction pointer is non-canonical.
#GP(Selector) If a segment selector index is outside its descriptor table limits.
   If a segment descriptor memory address is non-canonical.
   If the segment descriptor for a code segment does not indicate it is a code segment.
   If the proposed new code segment descriptor has both the D-bit and L-bit set.
   If the DPL for a nonconforming-code segment is not equal to the RPL of the code segment selector.
   If CPL is greater than the RPL of the code segment selector.
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If the DPL of a conforming-code segment is greater than the return code segment selector RPL.
If the stack segment is not a writable data segment.
If the stack segment descriptor DPL is not equal to the RPL of the return code segment selector.
If the stack segment selector RPL is not equal to the RPL of the return code segment selector.

#SS(0)  If an attempt to pop a value off the stack violates the SS limit.
If an attempt to pop a value off the stack causes a non-canonical address to be referenced.

#NP(selector)  If the return code or stack segment is not present.

#PF(fault-code)  If a page fault occurs.
#AC(0)  If an unaligned memory reference occurs when the CPL is 3 and alignment checking is enabled.

#UD  If the LOCK prefix is used.
### Jcc—Jump if Condition Is Met

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>77 cb</td>
<td>JA rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>73 cb</td>
<td>JAE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if above or equal (CF=0).</td>
</tr>
<tr>
<td>72 cb</td>
<td>JB rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if below (CF=1).</td>
</tr>
<tr>
<td>76 cb</td>
<td>JBE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>72 cb</td>
<td>JC rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if carry (CF=1).</td>
</tr>
<tr>
<td>E3 cb</td>
<td>JCXZ rel8</td>
<td>D</td>
<td>N.E.</td>
<td>Valid</td>
<td>Jump short if CX register is 0.</td>
</tr>
<tr>
<td>E3 cb</td>
<td>JECXZ rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if ECX register is 0.</td>
</tr>
<tr>
<td>E3 cb</td>
<td>JRCXZ rel8</td>
<td>D</td>
<td>N.E.</td>
<td>Valid</td>
<td>Jump short if RCX register is 0.</td>
</tr>
<tr>
<td>74 cb</td>
<td>JE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if equal (ZF=1).</td>
</tr>
<tr>
<td>7F cb</td>
<td>JG rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>7D cb</td>
<td>JGE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if greater or equal (SF=OF).</td>
</tr>
<tr>
<td>7C cb</td>
<td>JL rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if less (SF≠ OF).</td>
</tr>
<tr>
<td>7E cb</td>
<td>JLE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if less or equal (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>76 cb</td>
<td>JNA rel8</td>
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<td>Valid</td>
<td>Jump short if not above (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>72 cb</td>
<td>JNAE rel8</td>
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<td>Valid</td>
<td>Valid</td>
<td>Jump short if not above or equal (CF=1).</td>
</tr>
<tr>
<td>73 cb</td>
<td>JNB rel8</td>
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<td>Valid</td>
<td>Valid</td>
<td>Jump short if not below (CF=0).</td>
</tr>
<tr>
<td>77 cb</td>
<td>JNBE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not below or equal (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>73 cb</td>
<td>JNC rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not carry (CF=0).</td>
</tr>
<tr>
<td>75 cb</td>
<td>JNE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not equal (ZF=0).</td>
</tr>
<tr>
<td>7E cb</td>
<td>JNG rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not greater (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
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<td>64-Bit Mode</td>
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<td>------------------</td>
<td>---------------------------------------------------------------</td>
</tr>
<tr>
<td>7C cb</td>
<td>JNGE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not greater or equal (SF≠ OF).</td>
</tr>
<tr>
<td>7D cb</td>
<td>JNL rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not less (SF=OF).</td>
</tr>
<tr>
<td>7F cb</td>
<td>JNLE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not less or equal (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>71 cb</td>
<td>JNO rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not overflow (OF=0).</td>
</tr>
<tr>
<td>7B cb</td>
<td>JNP rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not parity (PF=0).</td>
</tr>
<tr>
<td>79 cb</td>
<td>JNS rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not sign (SF=0).</td>
</tr>
<tr>
<td>75 cb</td>
<td>JNZ rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if not zero (ZF=0).</td>
</tr>
<tr>
<td>70 cb</td>
<td>JO rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if overflow (OF=1).</td>
</tr>
<tr>
<td>7A cb</td>
<td>JP rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if parity (PF=1).</td>
</tr>
<tr>
<td>7A cb</td>
<td>JPE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if parity even (PF=1).</td>
</tr>
<tr>
<td>7B cb</td>
<td>JPO rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if parity odd (PF=0).</td>
</tr>
<tr>
<td>78 cb</td>
<td>JS rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if sign (SF=1).</td>
</tr>
<tr>
<td>74 cb</td>
<td>JZ rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short if zero (ZF ← 1).</td>
</tr>
<tr>
<td>0F 87 cw</td>
<td>JA rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if above (CF=0 and ZF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 87 cd</td>
<td>JA rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>0F 83 cw</td>
<td>JAΕ rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if above or equal (CF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 83 cd</td>
<td>JAΕ rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if above or equal (CF=0).</td>
</tr>
<tr>
<td>0F 82 cw</td>
<td>JB rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if below (CF=1).</td>
</tr>
<tr>
<td>0F 82 cd</td>
<td>JB rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if below (CF=1).</td>
</tr>
</tbody>
</table>

**Jcc—Jump if Condition Is Met**
## INSTRUCTION SET REFERENCE, A-L

<table>
<thead>
<tr>
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<th>64-Bit Mode</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0F 86  cw</td>
<td>JBE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if below or equal (CF=1 or ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 86  cd</td>
<td>JBE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>0F 82  cw</td>
<td>JC rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if carry (CF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 82  cd</td>
<td>JC rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if carry (CF=1).</td>
</tr>
<tr>
<td>0F 84  cw</td>
<td>JE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if equal (ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 84  cd</td>
<td>JE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if equal (ZF=1).</td>
</tr>
<tr>
<td>0F 84  cw</td>
<td>JZ rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if 0 (ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 84  cd</td>
<td>JZ rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if 0 (ZF=1).</td>
</tr>
<tr>
<td>0F 8F  cw</td>
<td>JG rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if greater (ZF=0 and SF=OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8F  cd</td>
<td>JG rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>0F 8D  cw</td>
<td>JGE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if greater or equal (SF=OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8D  cd</td>
<td>JGE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if greater or equal (SF=OF).</td>
</tr>
<tr>
<td>0F 8C  cw</td>
<td>JL rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if less (SF≠ OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8C  cd</td>
<td>JL rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if less (SF≠ OF).</td>
</tr>
<tr>
<td>0F 8E  cw</td>
<td>JLE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if less or equal (ZF=1 or SF≠ OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8E  cd</td>
<td>JLE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if less or equal (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>Op/En</td>
<td>64-Bit Mode</td>
<td>Compat/Leg Mode</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>-------</td>
<td>-------------</td>
<td>-----------------</td>
<td>-------------</td>
</tr>
<tr>
<td>OF 86 cw</td>
<td>JNA rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not above (CF=1 or ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>OF 86 cd</td>
<td>JNA rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not above (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>OF 82 cw</td>
<td>JNAE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not above or equal (CF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>OF 82 cd</td>
<td>JNAE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not above or equal (CF=1).</td>
</tr>
<tr>
<td>OF 83 cw</td>
<td>JNB rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not below (CF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>OF 83 cd</td>
<td>JNB rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not below (CF=0).</td>
</tr>
<tr>
<td>OF 87 cw</td>
<td>JNBE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not below or equal (CF=0 and ZF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>OF 87 cd</td>
<td>JNBE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not below or equal (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>OF 83 cw</td>
<td>JNC rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not carry (CF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>OF 83 cd</td>
<td>JNC rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not carry (CF=0).</td>
</tr>
<tr>
<td>OF 85 cw</td>
<td>JNE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not equal (ZF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>OF 85 cd</td>
<td>JNE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not equal (ZF=0).</td>
</tr>
<tr>
<td>OF 8E cw</td>
<td>JNG rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not greater (ZF=1 or SF≠ OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>OF 8E cd</td>
<td>JNG rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not greater (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>OF 8C cw</td>
<td>JNGE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not greater or equal (SF≠ OF). Not supported in 64-bit mode.</td>
</tr>
</tbody>
</table>

Jcc—Jump if Condition Is Met
<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 8C cd</td>
<td>JNGE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not greater or equal (SF≠ OF).</td>
</tr>
<tr>
<td>0F 8D cw</td>
<td>JNL rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not less (SF=OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8D cd</td>
<td>JNL rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not less (SF=OF).</td>
</tr>
<tr>
<td>0F 8F cw</td>
<td>JNLE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not less or equal (ZF=0 and SF=OF). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8F cd</td>
<td>JNLE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not less or equal (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>0F 81 cw</td>
<td>JNO rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not overflow (OF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 81 cd</td>
<td>JNO rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not overflow (OF=0).</td>
</tr>
<tr>
<td>0F 8B cw</td>
<td>JNP rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not parity (PF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8B cd</td>
<td>JNP rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not parity (PF=0).</td>
</tr>
<tr>
<td>0F 89 cw</td>
<td>JNS rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not sign (SF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 89 cd</td>
<td>JNS rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not sign (SF=0).</td>
</tr>
<tr>
<td>0F 85 cw</td>
<td>JNZ rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if not zero (ZF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 85 cd</td>
<td>JNZ rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if not zero (ZF=0).</td>
</tr>
<tr>
<td>0F 80 cw</td>
<td>JO rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if overflow (OF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 80 cd</td>
<td>JO rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if overflow (OF=1).</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-L

Jcc—Jump if Condition Is Met

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>Offset</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Checks the state of one or more of the status flags in the EFLAGS register (CF, OF, PF, SF, and ZF) and, if the flags are in the specified state (condition), performs a jump to the target instruction specified by the destination operand. A condition code (cc) is associated with each instruction to indicate the condition being tested for. If the condition is not satisfied, the jump is not performed and execution continues with the instruction following the Jcc instruction.

The target instruction is specified with a relative offset (a signed offset relative to the current value of the instruction pointer in the EIP register). A relative offset (rel8, rel16, or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed, 8-bit or 32-bit immediate value, which is added to the instruction pointer. Instruction coding is most efficient for offsets of –128 to 127.

---

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 8A cw</td>
<td>JP rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if parity (PF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8A cd</td>
<td>JP rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if parity (PF=1).</td>
</tr>
<tr>
<td>0F 8A cw</td>
<td>JPE rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if parity even (PF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8A cd</td>
<td>JPE rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if parity even (PF=1).</td>
</tr>
<tr>
<td>0F 8B cw</td>
<td>JPO rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if parity odd (PF=0). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 8B cd</td>
<td>JPO rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if parity odd (PF=0).</td>
</tr>
<tr>
<td>0F 88 cw</td>
<td>JS rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if sign (SF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 88 cd</td>
<td>JS rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if sign (SF=1).</td>
</tr>
<tr>
<td>0F 84 cw</td>
<td>JZ rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near if 0 (ZF=1). Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>0F 84 cd</td>
<td>JZ rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near if 0 (ZF=1).</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, A-L

+127. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared, resulting in a maximum instruction pointer size of 16 bits.

The conditions for each Jcc mnemonic are given in the "Description" column of the table on the preceding page. The terms "less" and "greater" are used for comparisons of signed integers and the terms "above" and "below" are used for unsigned integers.

Because a particular state of the status flags can sometimes be interpreted in two ways, two mnemonics are defined for some opcodes. For example, the JA (jump if above) instruction and the JNBE (jump if not below or equal) instruction are alternate mnemonics for the opcode 77H.

The Jcc instruction does not support far jumps (jumps to other code segments). When the target for the conditional jump is in a different segment, use the opposite condition from the condition being tested for the Jcc instruction, and then access the target with an unconditional far jump (JMP instruction) to the other segment. For example, the following conditional far jump is illegal:

```
JZ FARLABEL;
```
To accomplish this far jump, use the following two instructions:
```
JNZ BEYOND;
JMP FARLABEL;
BEYOND:
```

The JRCXZ, JECXZ and JCXZ instructions differ from other Jcc instructions because they do not check status flags. Instead, they check RCX, ECX or CX for 0. The register checked is determined by the address-size attribute. These instructions are useful when used at the beginning of a loop that terminates with a conditional loop instruction (such as LOOPNE). They can be used to prevent an instruction sequence from entering a loop when RCX, ECX or CX is 0. This would cause the loop to execute $2^{64}$, $2^{32}$ or 64K times (not zero times).

All conditional jumps are converted to code fetches of one or two cache lines, regardless of jump address or cacheability.

In 64-bit mode, operand size is fixed at 64 bits. JMP Short is RIP = RIP + 8-bit offset sign extended to 64 bits. JMP Near is RIP = RIP + 32-bit offset sign extended to 64-bits.

**Operation**

```c
IF condition
    THEN
tempEIP ← EIP + SignExtend(DEST);
    IF OperandSize = 16
        THEN tempEIP ← tempEIP AND 0000FFFFH;
    FI;
    IF tempEIP is not within code segment limit
        THEN #GP(0);
```

Jcc—Jump if Condition Is Met
ELSE EIP ← tempEIP
FI;
FI;

Protected Mode Exceptions
#GP(0) If the offset being jumped to is beyond the limits of the CS segment.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If the offset being jumped to is beyond the limits of the CS segment or is outside of the effective address space from 0 to FFFFH. This condition can occur if a 32-bit address size override prefix is used.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
#UD If the LOCK prefix is used.
### JMP—Jump

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EB cb</td>
<td>JMP rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump short, RIP = RIP + 8-bit displacement sign extended to 64-bits</td>
</tr>
<tr>
<td>E9 cw</td>
<td>JMP rel16</td>
<td>D</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near, relative, displacement relative to next instruction. Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>E9 cd</td>
<td>JMP rel32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump near, relative, RIP = RIP + 32-bit displacement sign extended to 64-bits</td>
</tr>
<tr>
<td>FF /4</td>
<td>JMP r/m16</td>
<td>M</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near, absolute indirect, address = zero-extended r/m16. Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>FF /4</td>
<td>JMP r/m32</td>
<td>M</td>
<td>N.S.</td>
<td>Valid</td>
<td>Jump near, absolute indirect, address given in r/m32. Not supported in 64-bit mode.</td>
</tr>
<tr>
<td>FF /4</td>
<td>JMP r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Jump near, absolute indirect, RIP = 64-Bit offset from register or memory</td>
</tr>
<tr>
<td>EA cd</td>
<td>JMP ptr16:16</td>
<td>D</td>
<td>Inv.</td>
<td>Valid</td>
<td>Jump far, absolute, address given in operand</td>
</tr>
<tr>
<td>EA cp</td>
<td>JMP ptr16:32</td>
<td>D</td>
<td>Inv.</td>
<td>Valid</td>
<td>Jump far, absolute, address given in operand</td>
</tr>
<tr>
<td>FF /5</td>
<td>JMP m16:16</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump far, absolute indirect, address given in m16:16</td>
</tr>
<tr>
<td>FF /5</td>
<td>JMP m16:32</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Jump far, absolute indirect, address given in m16:32</td>
</tr>
<tr>
<td>REX.w + FF /5</td>
<td>JMP m16:64</td>
<td>D</td>
<td>Valid</td>
<td>N.E.</td>
<td>Jump far, absolute indirect, address given in m16:64</td>
</tr>
</tbody>
</table>

#### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 2</th>
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</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>Offset</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
Description

Transfers program control to a different point in the instruction stream without recording return information. The destination (target) operand specifies the address of the instruction being jumped to. This operand can be an immediate value, a general-purpose register, or a memory location.

This instruction can be used to execute four different types of jumps:

• Near jump—A jump to an instruction within the current code segment (the segment currently pointed to by the CS register), sometimes referred to as an intrasegment jump.
• Short jump—A near jump where the jump range is limited to –128 to +127 from the current EIP value.
• Far jump—A jump to an instruction located in a different segment than the current code segment but at the same privilege level, sometimes referred to as an intersegment jump.
• Task switch—A jump to an instruction located in a different task.

A task switch can only be executed in protected mode (see Chapter 7, in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A, for information on performing task switches with the JMP instruction).

Near and Short Jumps. When executing a near jump, the processor jumps to the address (within the current code segment) that is specified with the target operand. The target operand specifies either an absolute offset (that is an offset from the base of the code segment) or a relative offset (a signed displacement relative to the current value of the instruction pointer in the EIP register). A near jump to a relative offset of 8-bits (rel8) is referred to as a short jump. The CS register is not changed on near and short jumps.

An absolute offset is specified indirectly in a general-purpose register or a memory location (r/m16 or r/m32). The operand-size attribute determines the size of the target operand (16 or 32 bits). Absolute offsets are loaded directly into the EIP register. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared, resulting in a maximum instruction pointer size of 16 bits.

A relative offset (rel8, rel16, or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed 8-, 16-, or 32-bit immediate value. This value is added to the value in the EIP register. (Here, the EIP register contains the address of the instruction following the JMP instruction). When using relative offsets, the opcode (for short vs. near jumps) and the operand-size attribute (for near relative jumps) determines the size of the target operand (8, 16, or 32 bits).

Far Jumps in Real-Address or Virtual-8086 Mode. When executing a far jump in real-address or virtual-8086 mode, the processor jumps to the code segment and offset specified with the target operand. Here the target operand specifies an absolute far address either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). With the pointer method, the segment and address of the called procedure is encoded in the instruction, using a 4-byte (16-bit
operand size) or 6-byte (32-bit operand size) far address immediate. With the indirect method, the target operand specifies a memory location that contains a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address. The far address is loaded directly into the CS and EIP registers. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared.

Far Jumps in Protected Mode. When the processor is operating in protected mode, the JMP instruction can be used to perform the following three types of far jumps:

- A far jump to a conforming or non-conforming code segment.
- A far jump through a call gate.
- A task switch.

(The JMP instruction cannot be used to perform inter-privilege-level far jumps.)

In protected mode, the processor always uses the segment selector part of the far address to access the corresponding descriptor in the GDT or LDT. The descriptor type (code segment, call gate, task gate, or TSS) and access rights determine the type of jump to be performed.

If the selected descriptor is for a code segment, a far jump to a code segment at the same privilege level is performed. (If the selected code segment is at a different privilege level and the code segment is non-conforming, a general-protection exception is generated.) A far jump to the same privilege level in protected mode is very similar to one carried out in real-address or virtual-8086 mode. The target operand specifies an absolute far address either directly with a pointer ($ptr_{16:16}$ or $ptr_{16:32}$) or indirectly with a memory location ($m_{16:16}$ or $m_{16:32}$). The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The new code segment selector and its descriptor are loaded into CS register, and the offset from the instruction is loaded into the EIP register. Note that a call gate (described in the next paragraph) can also be used to perform far call to a code segment at the same privilege level. Using this mechanism provides an extra level of indirection and is the preferred method of making jumps between 16-bit and 32-bit code segments.

When executing a far jump through a call gate, the segment selector specified by the target operand identifies the call gate. (The offset part of the target operand is ignored.) The processor then jumps to the code segment specified in the call gate descriptor and begins executing the instruction at the offset specified in the call gate. No stack switch occurs. Here again, the target operand can specify the far address of the call gate either directly with a pointer ($ptr_{16:16}$ or $ptr_{16:32}$) or indirectly with a memory location ($m_{16:16}$ or $m_{16:32}$).

Executing a task switch with the JMP instruction is somewhat similar to executing a jump through a call gate. Here the target operand specifies the segment selector of the task gate for the task being switched to (and the offset part of the target operand is ignored). The task gate in turn points to the TSS for the task, which contains the segment selectors for the task’s code and stack segments. The TSS also contains the EIP value for the next instruction that was to be executed before the task was suspended. This instruction pointer value is loaded into the EIP register so that the task begins executing again at this next instruction.
The JMP instruction can also specify the segment selector of the TSS directly, which eliminates the indirection of the task gate. See Chapter 7 in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for detailed information on the mechanics of a task switch.

Note that when you execute at task switch with a JMP instruction, the nested task flag (NT) is not set in the EFLAGS register and the new TSS’s previous task link field is not loaded with the old task’s TSS selector. A return to the previous task can thus not be carried out by executing the IRET instruction. Switching tasks with the JMP instruction differs in this regard from the CALL instruction which does set the NT flag and save the previous task link information, allowing a return to the calling task with an IRET instruction.

**In 64-Bit Mode** — The instruction’s operation size is fixed at 64 bits. If a selector points to a gate, then RIP equals the 64-bit displacement taken from gate; else RIP equals the zero-extended offset from the far pointer referenced in the instruction. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF near jump
  IF 64-bit Mode
    THEN
      IF near relative jump
        THEN
          tempRIP ← RIP + DEST; (* RIP is instruction following JMP instruction*)
        ELSE (* Near absolute jump *)
          tempRIP ← DEST;
        FI;
      ELSE
        IF near relative jump
          THEN
            tempEIP ← EIP + DEST; (* EIP is instruction following JMP instruction*)
          ELSE (* Near absolute jump *)
            tempEIP ← DEST;
          FI;
        FI;
    FI;
  IF (IA32_EFER.LMA = 0 or target mode = Compatibility mode)
and tempEIP outside code segment limit
    THEN #GP(0); FI
  IF 64-bit mode and tempRIP is not canonical
    THEN #GP(0);
  FI;
  IF OperandSize = 32
    THEN
      EIP ← tempEIP;
JMP—Jump
ELSE
    IF OperandSize = 16
        THEN (* OperandSize = 16 *)
            EIP ← tempEIP AND 0000FFFFH;
        ELSE (* OperandSize = 64 *)
            RIP ← tempRIP;
        FI;
    FI;
FI;
IF far jump and (PE = 0 or (PE = 1 AND VM = 1)) (* Real-address or virtual-8086 mode *)
THEN
    tempEIP ← DEST(Offset); (* DEST is ptr16:32 or [m16:32] *)
    IF tempEIP is beyond code segment limit
        THEN #GP(0); FI;
    CS ← DEST(segment selector); (* DEST is ptr16:32 or [m16:32] *)
    IF OperandSize = 32
        THEN
            EIP ← tempEIP; (* DEST is ptr16:32 or [m16:32] *)
        ELSE (* OperandSize = 16 *)
            EIP ← tempEIP AND 0000FFFFH; (* Clear upper 16 bits *)
        FI;
    FI;
IF far jump and (PE = 1 and VM = 0)
(* IA-32e mode or protected mode, not virtual-8086 mode *)
THEN
    IF effective address in the CS, DS, ES, FS, GS, or SS segment is illegal
        or segment selector in target operand NULL
        THEN #GP(0); FI;
    IF segment selector index not within descriptor table limits
        THEN #GP(new selector); FI;
    Read type and access rights of segment descriptor;
    IF (EFER.LMA = 0)
        THEN
            IF segment type is not a conforming or nonconforming code
                segment, call gate, task gate, or TSS
                THEN #GP(segment selector); FI;
            ELSE
                IF segment type is not a conforming or nonconforming code segment
                    call gate
                    THEN #GP(segment selector); FI;
            FI;
        Depending on type and access rights:
            GO TO CONFORMING-CODE-SEGMENT;
            GO TO NONCONFORMING-CODE-SEGMENT;
GO TO CALL-GATE;
GO TO TASK-GATE;
GO TO TASK-STATE-SEGMENT;
ELSE
    #GP(segment selector);
FI;

CONFORMING-CODE-SEGMENT:
    IF L-Bit = 1 and D-BIT = 1 and IA32_EFER.LMA = 1
        THEN GP(new code segment selector); FI;
    IF DPL > CPL
        THEN #GP(segment selector); FI;
    IF segment not present
        THEN #NP(segment selector); FI;
    tempEIP ← DEST(Offset);
    IF OperandSize = 16
        THEN tempEIP ← tempEIP AND 0000FFFFH;
    FI;
    IF (IA32_EFER.LMA = 0 or target mode = Compatibility mode) and
    tempEIP outside code segment limit
        THEN #GP(0); FI
    IF tempEIP is non-canonical
        THEN #GP(0); FI;
    CS ← DEST[segment selector]; (* Segment descriptor information also loaded *)
    CS(RPL) ← CPL
    EIP ← tempEIP;
END;

NONCONFORMING-CODE-SEGMENT:
    IF L-Bit = 1 and D-BIT = 1 and IA32_EFER.LMA = 1
        THEN GP(new code segment selector); FI;
    IF (RPL > CPL) OR (DPL ≠ CPL)
        THEN #GP(code segment selector); FI;
    IF segment not present
        THEN #NP(segment selector); FI;
    tempEIP ← DEST(Offset);
    IF OperandSize = 16
        THEN tempEIP ← tempEIP AND 0000FFFFH; FI;
    IF (IA32_EFER.LMA = 0 OR target mode = Compatibility mode)
    and tempEIP outside code segment limit
        THEN #GP(0); FI
    IF tempEIP is non-canonical THEN #GP(0); FI;
    CS ← DEST[segment selector]; (* Segment descriptor information also loaded *)
    CS(RPL) ← CPL;
    EIP ← tempEIP;
END;
INSTRUCTION SET REFERENCE, A-L

CALL-GATE:
   IF call gate DPL < CPL
   or call gate DPL < call gate segment-selector RPL
      THEN #GP(call gate selector); Fi;
   IF call gate not present
      THEN #NP(call gate selector); Fi;
   IF call gate code-segment selector is NULL
      THEN #GP(0); Fi;
   IF call gate code-segment selector index outside descriptor table limits
      THEN #GP(code segment selector); Fi;
   Read code segment descriptor;
   IF code-segment segment descriptor does not indicate a code segment
   or code-segment segment descriptor is conforming and DPL > CPL
   or code-segment segment descriptor is non-conforming and DPL ≠ CPL
      THEN #GP(code segment selector); Fi;
   IF IA32_EFER.LMA = 1 and (code-segment descriptor is not a 64-bit code segment
   or code-segment segment descriptor has both L-Bit and D-bit set)
      THEN #GP(code segment selector); Fi;
   IF code segment is not present
      THEN #NP(code-segment selector); Fi;
   IF instruction pointer is not within code-segment limit
      THEN #GP(0); Fi;
   tempEIP ← DEST(Offset);
   IF GateSize = 16
      THEN tempEIP ← tempEIP AND 0000FFFFH; Fi;
   IF (IA32_EFER.LMA = 0 OR target mode = Compatibility mode) AND tempEIP
      outside code segment limit
      THEN #GP(0); Fi
   CS ← DEST[SegmentSelector]; (* Segment descriptor information also loaded *)
   CS(RPL) ← CPL;
   EIP ← tempEIP;
END;

TASK-GATE:
   IF task gate DPL < CPL
   or task gate DPL < task gate segment-selector RPL
      THEN #GP(task gate selector); Fi;
   IF task gate not present
      THEN #NP(gate selector); Fi;
   Read the TSS segment selector in the task-gate descriptor;
   IF TSS segment selector local/global bit is set to local
   or index not within GDT limits
   or TSS descriptor specifies that the TSS is busy
      THEN #GP(TSS selector); Fi;
IF TSS not present
    THEN #NP(TSS selector); Fl;
SWITCH-TASKS to TSS;
IF EIP not within code segment limit
    THEN #GP(0); Fl;
END;

TASK-STATE-SEGMENT:
IF TSS DPL < CPL
    or TSS DPL < TSS segment-selector RPL
    or TSS descriptor indicates TSS not available
    THEN #GP(TSS selector); Fl;
IF TSS is not present
    THEN #NP(TSS selector); Fl;
SWITCH-TASKS to TSS;
IF EIP not within code segment limit
    THEN #GP(0); Fl;
END;

Flags Affected
All flags are affected if a task switch occurs; no flags are affected if a task switch does not occur.

Protected Mode Exceptions
#GP(0)   If offset in target operand, call gate, or TSS is beyond the code segment limits.
         If the segment selector in the destination operand, call gate, task gate, or TSS is NULL.
         If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
         If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#GP(selector) If the segment selector index is outside descriptor table limits.
         If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, call gate, task gate, or task state segment.
         If the DPL for a nonconforming-code segment is not equal to the CPL
         (When not using a call gate.) If the RPL for the segment’s segment selector is greater than the CPL.
         If the DPL for a conforming-code segment is greater than the CPL.
If the DPL from a call-gate, task-gate, or TSS segment descriptor is less than the CPL or than the RPL of the call-gate, task-gate, or TSS’s segment selector.
If the segment descriptor for selector in a call gate does not indicate it is a code segment.
If the segment descriptor for the segment selector in a task gate does not indicate an available TSS.
If the segment selector for a TSS has its local/global bit set for local.
If a TSS segment descriptor specifies that the TSS is busy or not available.

#SS(0) If a memory operand effective address is outside the SS segment limit.
#NP (selector) If the code segment being accessed is not present.
If call gate, task gate, or TSS not present.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3. (Only occurs when fetching target from memory.)
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If the target operand is beyond the code segment limits.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made. (Only occurs when fetching target from memory.)
#UD If the LOCK prefix is used.
Compatibility Mode Exceptions
Same as 64-bit mode exceptions.

64-Bit Mode Exceptions

#GP(0) If a memory address is non-canonical.
If target offset in destination operand is non-canonical.
If target offset in destination operand is beyond the new code segment limit.
If the segment selector in the destination operand is NULL.
If the code segment selector in the 64-bit gate is NULL.

#GP(selector) If the code segment or 64-bit call gate is outside descriptor table limits.
If the code segment or 64-bit call gate overlaps non-canonical space.
If the segment descriptor from a 64-bit call gate is in non-canonical space.
If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, 64-bit call gate.
If the segment descriptor pointed to by the segment selector in the destination operand is a code segment, and has both the D-bit and the L-bit set.
If the DPL for a nonconforming-code segment is not equal to the CPL, or the RPL for the segment’s segment selector is greater than the CPL.
If the DPL for a conforming-code segment is greater than the CPL.
If the DPL from a 64-bit call-gate is less than the CPL or than the RPL of the 64-bit call-gate.
If the upper type field of a 64-bit call gate is not 0x0.
If the segment selector from a 64-bit call gate is beyond the descriptor table limits.
If the code segment descriptor pointed to by the selector in the 64-bit gate doesn’t have the L-bit set and the D-bit clear.
If the segment descriptor for a segment selector from the 64-bit call gate does not indicate it is a code segment.
If the code segment is non-confirming and CPL ≠ DPL.
If the code segment is confirming and CPL < DPL.

#NP(selector) If a code segment or 64-bit call gate is not present.

#UD (64-bit mode only) If a far jump is direct to an absolute address in memory.
INSTRUCTION SET REFERENCE, A-L

If the LOCK prefix is used.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
LAHF—Load Status Flags into AH Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
</table>

NOTES:
*Valid in specific steppings. See Description section.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

This instruction executes as described above in compatibility mode and legacy mode. It is valid in 64-bit mode only if CPUID.80000001H:ECX.LAHF-SAHF[bit 0] = 1.

Operation

IF 64-Bit Mode
THEN
IF CPUID.80000001H:ECX.LAHF-SAHF[bit 0] = 1;
THEN AH ← RFLAGS(SF:ZF:0:AF:0:PF:1:CF);
ELSE #UD;
FI;
ELSE
AH ← EFLAGS(SF:ZF:0:AF:0:PF:1:CF);
FI;

Flags Affected

None. The state of the flags in the EFLAGS register is not affected.

Protected Mode Exceptions

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.


INSTRUCTION SET REFERENCE, A-L

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#UD  If CPUID.80000001H:ECX.LAHF-SAHF[bit 0] = 0.
     If the LOCK prefix is used.
LAR—Load Access Rights Byte

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m(r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Loads the access rights from the segment descriptor specified by the second operand (source operand) into the first operand (destination operand) and sets the ZF flag in the flag register. The source operand (which can be a register or a memory location) contains the segment selector for the segment descriptor being accessed. If the source operand is a memory address, only 16 bits of data are accessed. The destination operand is a general-purpose register.

The processor performs access checks as part of the loading process. Once loaded in the destination register, software can perform additional checks on the access rights information.

When the operand size is 32 bits, the access rights for a segment descriptor include the type and DPL fields and the S, P, AVL, D/B, and G flags, all of which are located in the second doubleword (bytes 4 through 7) of the segment descriptor. The doubleword is masked by 00FxFF00H before it is loaded into the destination operand. When the operand size is 16 bits, the access rights include the type and DPL fields. Here, the two lower-order bytes of the doubleword are masked by FF00H before being loaded into the destination operand.

This instruction performs the following checks before it loads the access rights in the destination register:

- Checks that the segment selector is not NULL.
- Checks that the segment selector points to a descriptor that is within the limits of the GDT or LDT being accessed.

### Notes:

1. For all loads (regardless of source or destination sizing) only bits 16-0 are used. Other bits are ignored.
Checks that the descriptor type is valid for this instruction. All code and data segment descriptors are valid for (can be accessed with) the LAR instruction. The valid system segment and gate descriptor types are given in Table 3-62.

If the segment is not a conforming code segment, it checks that the specified segment descriptor is visible at the CPL (that is, if the CPL and the RPL of the segment selector are less than or equal to the DPL of the segment selector).

If the segment descriptor cannot be accessed or is an invalid type for the instruction, the ZF flag is cleared and no access rights are loaded in the destination operand.

The LAR instruction can only be executed in protected mode and IA-32e mode.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.W prefix permits access to 64-bit registers as destination.

When the destination operand size is 64 bits, the access rights are loaded from the second doubleword (bytes 4 through 7) of the segment descriptor. The doubleword is masked by 00FXFF00H and zero extended to 64 bits before it is loaded into the destination operand.

<table>
<thead>
<tr>
<th>Type</th>
<th>Protected Mode</th>
<th>IA-32e Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Name</td>
<td>Valid</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>Available 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>LDT</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>Busy 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>16-bit call gate</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>16-bit/32-bit task gate</td>
<td>Yes</td>
</tr>
<tr>
<td>6</td>
<td>16-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>7</td>
<td>16-bit trap gate</td>
<td>No</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>9</td>
<td>Available 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>A</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>B</td>
<td>Busy 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>C</td>
<td>32-bit call gate</td>
<td>Yes</td>
</tr>
<tr>
<td>D</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>E</td>
<td>32-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>F</td>
<td>32-bit trap gate</td>
<td>No</td>
</tr>
</tbody>
</table>
Operation

IF Offset(SRC) > descriptor table limit
  THEN
    ZF = 0;
  ELSE
    IF SegmentDescriptor(Type) ≠ conforming code segment
       and (CPL > DPL) or (RPL > DPL)
       or segment type is not valid for instruction
       THEN
         ZF ← 0
       ELSE
         TEMP ← Read segment descriptor ;
         IF OperandSize = 64
            THEN
              DEST ← (ACCESSRIGHTWORD(TEMP) AND 00000000_00FxFF00H);
            ELSE (* OperandSize = 32*)
              DEST ← (ACCESSRIGHTWORD(TEMP) AND 00FxFF00H);
            ELSE (* OperandSize = 16 *)
              DEST ← (ACCESSRIGHTWORD(TEMP) AND FF00H);
            FI;
          FI;
        FI;
  FI;

Flags Affected
The ZF flag is set to 1 if the access rights are loaded successfully; otherwise, it is set to 0.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and the memory operand effective address is unaligned while the current privilege level is 3.

#UD If the LOCK prefix is used.

LAR—Load Access Rights Byte
Real-Address Mode Exceptions
#UD The LAR instruction is not recognized in real-address mode.

Virtual-8086 Mode Exceptions
#UD The LAR instruction cannot be executed in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If the memory operand effective address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory operand effective address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and the memory operand effective address is unaligned while the current privilege level is 3.
#UD If the LOCK prefix is used.
LDDQU—Load Unaligned Integer 128 Bits

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F F0 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE3</td>
<td>Load unaligned data from mem and return double quadword in xmm1.</td>
</tr>
<tr>
<td>LDDQU xmm1, mem</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.F2.0F:WIG F0 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Load unaligned packed integer values from mem to xmm1.</td>
</tr>
<tr>
<td>VLDDQU xmm1, m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.F2.0F:WIG F0 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Load unaligned packed integer values from mem to ymm1.</td>
</tr>
<tr>
<td>VLDDQU ymm1, m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

InstructionOperand Encoding

<table>
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<tbody>
<tr>
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<td>ModRMreg (w)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

The instruction is functionally similar to (V)MOVDQU ymm/xmm, m256/m128 for loading from memory. That is: 32/16 bytes of data starting at an address specified by the source memory operand (second operand) are fetched from memory and placed in a destination register (first operand). The source operand need not be aligned on a 32/16-byte boundary. Up to 64/32 bytes may be loaded from memory; this is implementation dependent.

This instruction may improve performance relative to (V)MOVDQU if the source operand crosses a cache line boundary. In situations that require the data loaded by (V)LDDQU to be modified and stored to the same location, use (V)MOVDQU or (V)MOVDQA instead of (V)LDDQU. To move a double quadword to or from memory locations that are known to be aligned on 16-byte boundaries, use the (V)MOVDQA instruction.

Implementation Notes

- If the source is aligned to a 32/16-byte boundary, based on the implementation, the 32/16 bytes may be loaded more than once. For that reason, the usage of (V)LDDQU should be avoided when using uncached or write-combining (WC) memory regions. For uncached or WC memory regions, keep using (V)MOVDQU.
- This instruction is a replacement for (V)MOVDQU (load) in situations where cache line splits significantly affect performance. It should not be used in situations where store-load forwarding is performance critical. If performance of store-load forwarding is critical to the application, use (V)MOVDQA store-load pairs when...
data is 256/128-bit aligned or (V)MOVDQU store-load pairs when data is 256/128-bit unaligned.

- If the memory address is not aligned on 32/16-byte boundary, some implementations may load up to 64/32 bytes and return 32/16 bytes in the destination. Some processor implementations may issue multiple loads to access the appropriate 32/16 bytes. Developers of multi-threaded or multi-processor software should be aware that on these processors the loads will be performed in a non-atomic way.

- If alignment checking is enabled (CR0.AM = 1, RFLAGS.AC = 1, and CPL = 3), an alignment-check exception (#AC) may or may not be generated (depending on processor implementation) when the memory address is not aligned on an 8-byte boundary.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

**LDDQU (128-bit Legacy SSE version)**

DEST[127:0] ← SRC[127:0]

DEST[VLMAX-1:128] (Unmodified)

**VLDDQU (VEX.128 encoded version)**

DEST[127:0] ← SRC[127:0]

DEST[VLMAX-1:128] ← 0

**VLDDQU (VEX.256 encoded version)**

DEST[255:0] ← SRC[255:0]

**Intel C/C++ Compiler Intrinsic Equivalent**

LDDQU:  __m128i _mm_lddqu_si128 (__m128i * p);

LDDQU:  __m256i _mm256_lddqu_si256 (__m256i * p);

**Numeric Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4;

Note treatment of #AC varies.
**LDMXCSR—Load MXCSR Register**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,AE,/2</td>
<td>M</td>
<td>V/V</td>
<td>SSE</td>
<td>Load MXCSR register from m32.</td>
</tr>
<tr>
<td>LDMXCSR m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LZ.0F:WIG AE /2</td>
<td>M</td>
<td>V/V</td>
<td>AVX</td>
<td>Load MXCSR register from m32.</td>
</tr>
<tr>
<td>VLDMXCSR m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Loads the source operand into the MXCSR control/status register. The source operand is a 32-bit memory location. See "MXCSR Control and Status Register" in Chapter 10, of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for a description of the MXCSR register and its contents.

The LDMXCSR instruction is typically used in conjunction with the (V)STMXCSR instruction, which stores the contents of the MXCSR register in memory.

The default MXCSR value at reset is 1F80H.

If a (V)LDMXCSR instruction clears a SIMD floating-point exception mask bit and sets the corresponding exception flag bit, a SIMD floating-point exception will not be immediately generated. The exception will be generated only upon the execution of the next instruction that meets both conditions below:

- the instruction must operate on an XMM or YMM register operand,
- the instruction causes that particular SIMD floating-point exception to be reported.

This instruction's operation is the same in non-64-bit modes and 64-bit mode. If VLDMXCSR is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

**Operation**

\[
\text{MXCSR} \leftarrow \text{m32};
\]
C/C++ Compiler Intrinsic Equivalent

_{mm_setcsr}(unsigned int i)

Numeric Exceptions

None.

Other Exceptions

See Exceptions Type 5; additionally

#GP For an attempt to set reserved bits in MXCSR.

#UD If VEX.vvvv ! = 1111B.
### LDS/LES/LFS/LGS/LSS—Load Far Pointer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C5 /r</td>
<td>LDS r16,m16:16</td>
<td>RM</td>
<td>Invalid</td>
<td>Valid</td>
<td>Load DS:r16 with far pointer from memory.</td>
</tr>
<tr>
<td>C5 /r</td>
<td>LDS r32,m16:32</td>
<td>RM</td>
<td>Invalid</td>
<td>Valid</td>
<td>Load DS:r32 with far pointer from memory.</td>
</tr>
<tr>
<td>0F B2 /r</td>
<td>LSS r16,m16:16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load SS:r16 with far pointer from memory.</td>
</tr>
<tr>
<td>0F B2 /r</td>
<td>LSS r32,m16:32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load SS:r32 with far pointer from memory.</td>
</tr>
<tr>
<td>REX + 0F B2 /r</td>
<td>LSS r64,m16:64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load SS:r64 with far pointer from memory.</td>
</tr>
<tr>
<td>C4 /r</td>
<td>LES r16,m16:16</td>
<td>RM</td>
<td>Invalid</td>
<td>Valid</td>
<td>Load ES:r16 with far pointer from memory.</td>
</tr>
<tr>
<td>C4 /r</td>
<td>LES r32,m16:32</td>
<td>RM</td>
<td>Invalid</td>
<td>Valid</td>
<td>Load ES:r32 with far pointer from memory.</td>
</tr>
<tr>
<td>0F B4 /r</td>
<td>LFS r16,m16:16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FS:r16 with far pointer from memory.</td>
</tr>
<tr>
<td>0F B4 /r</td>
<td>LFS r32,m16:32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load FS:r32 with far pointer from memory.</td>
</tr>
<tr>
<td>REX + 0F B4 /r</td>
<td>LFS r64,m16:64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load FS:r64 with far pointer from memory.</td>
</tr>
<tr>
<td>0F B5 /r</td>
<td>LGS r16,m16:16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load GS:r16 with far pointer from memory.</td>
</tr>
<tr>
<td>0F B5 /r</td>
<td>LGS r32,m16:32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load GS:r32 with far pointer from memory.</td>
</tr>
<tr>
<td>REX + 0F B5 /r</td>
<td>LGS r64,m16:64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load GS:r64 with far pointer from memory.</td>
</tr>
</tbody>
</table>

#### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Description

Loads a far pointer (segment selector and offset) from the second operand (source operand) into a segment register and the first operand (destination operand). The source operand specifies a 48-bit or a 32-bit pointer in memory depending on the current setting of the operand-size attribute (32 bits or 16 bits, respectively). The
INSTRUCTION SET REFERENCE, A-L

Instruction opcode and the destination operand specify a segment register/general-purpose register pair. The 16-bit segment selector from the source operand is loaded into the segment register specified with the opcode (DS, SS, ES, FS, or GS). The 32-bit or 16-bit offset is loaded into the register specified with the destination operand.

If one of these instructions is executed in protected mode, additional information from the segment descriptor pointed to by the segment selector in the source operand is loaded in the hidden part of the selected segment register.

Also in protected mode, a NULL selector (values 0000 through 0003) can be loaded into DS, ES, FS, or GS registers without causing a protection exception. (Any subsequent reference to a segment whose corresponding segment register is loaded with a NULL selector, causes a general-protection exception (#GP) and no memory reference to the segment occurs.)

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.W promotes operation to specify a source operand referencing an 80-bit pointer (16-bit selector, 64-bit offset) in memory. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). See the summary chart at the beginning of this section for encoding data and limits.

Operation

64-BIT MODE

IF SS is loaded

THEN

IF SegmentSelector = NULL and ((RPL = 3) or
 (RPL ≠ 3 and RPL ≠ CPL))
 THEN #GP(0);
ELSE IF descriptor is in non-canonical space
 THEN #GP(0); Fl;
ELSE IF Segment selector index is not within descriptor table limits
 or segment selector RPL ≠ CPL
 or access rights indicate nonwritable data segment
 or DPL ≠ CPL
 THEN #GP(selector); Fl;
ELSE IF Segment marked not present
 THEN #SS(selector); Fl;
 Fl;
 SS ← SegmentSelector(SRC);
 SS ← SegmentDescriptor([SRC]);
ELSE IF attempt to load DS, or ES
 THEN #UD;
ELSE IF FS, or GS is loaded with non-NULL segment selector
 THEN IF Segment selector index is not within descriptor table limits
 or access rights indicate segment neither data nor readable code segment

LDS/LES/LFS/LGS/LSS—Load Far Pointer
or segment is data or nonconforming-code segment
and (RPL > DPL or CPL > DPL)
THEN #GP(selector); FI;
ELSE IF Segment marked not present
THEN #NP(selector); FI;
FI;
SegmentRegister ← SegmentSelector(SRC);
SegmentRegister ← SegmentDescriptor([SRC]);
FI;
ELSE IF FS, or GS is loaded with a NULL selector:
THEN
SegmentRegister ← NULLSelector;
SegmentRegister(DescriptorValidBit) ← 0; F1; (* Hidden flag:
not accessible by software *)
FI;
DEST ← Offset(SRC);

PRETECTED MODE OR COMPATIBILITY MODE;
IF SS is loaded
THEN
IF SegmentSelector = NULL
THEN #GP(0);
ELSE IF Segment selector index is not within descriptor table limits
or segment selector RPL ≠ CPL
or access rights indicate nonwritable data segment
or DPL ≠ CPL
THEN #GP(selector); FI;
ELSE IF Segment marked not present
THEN #SS(selector); FI;
FI;
SS ← SegmentSelector(SRC);
SS ← SegmentDescriptor([SRC]);
ELSE IF DS, ES, FS, or GS is loaded with non-NULL segment selector
THEN IF Segment selector index is not within descriptor table limits
or access rights indicate segment neither data nor readable code segment
or segment is data or nonconforming-code segment
and (RPL > DPL or CPL > DPL)
THEN #GP(selector); FI;
ELSE IF Segment marked not present
THEN #NP(selector); FI;
FI;
SegmentRegister ← SegmentSelector(SRC) AND RPL;
SegmentRegister ← SegmentDescriptor([SRC]);
FI;

LDS/LES/LFS/LGS/LSS—Load Far Pointer
ELSE IF DS, ES, FS, or GS is loaded with a NULL selector:
    THEN
        SegmentRegister ← NULLSelector;
        SegmentRegister(DescriptorValidBit) ← 0; Fl; (* Hidden flag; not accessible by software *)
    Fl;
    DEST ← Offset(SRC);

Real-Address or Virtual-8086 Mode
    SegmentRegister ← SegmentSelector(SRC); Fl;
    DEST ← Offset(SRC);

Flags Affected
None.

Protected Mode Exceptions
#UD If source operand is not a memory location.
    If the LOCK prefix is used.
#GP(0) If a NULL selector is loaded into the SS register.
    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#GP(selector) If the SS register is being loaded and any of the following is true: the segment selector index is not within the descriptor table limits, the segment selector RPL is not equal to CPL, the segment is a non-writable data segment, or DPL is not equal to CPL.
    If the DS, ES, FS, or GS register is being loaded with a non-NULL segment selector and any of the following is true: the segment selector index is not within descriptor table limits, the segment is neither a data nor a readable code segment, or the segment is a data or nonconforming-code segment and both RPL and CPL are greater than DPL.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#SS(selector) If the SS register is being loaded and the segment is marked not present.
#NP(selector) If DS, ES, FS, or GS register is being loaded with a non-NULL segment selector and the segment is marked not present.
#PF(fault-code) If a page fault occurs.
LDS/LES/LFS/LGS/LSS—Load Far Pointer

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#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If source operand is not a memory location.
       If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#UD If source operand is not a memory location.
       If the LOCK prefix is used.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
       If a NULL selector is attempted to be loaded into the SS register in compatibility mode.
       If a NULL selector is attempted to be loaded into the SS register in CPL3 and 64-bit mode.
       If a NULL selector is attempted to be loaded into the SS register in non-CPL3 and 64-bit mode where its RPL is not equal to CPL.
#GP(Selector) If the FS, or GS register is being loaded with a non-NULL segment selector and any of the following is true: the segment selector index is not within descriptor table limits, the memory address of the descriptor is non-canonical, the segment is neither a data nor a readable code segment, or the segment is a data or nonconforming-code segment and both RPL and CPL are greater than DPL.
If the SS register is being loaded and any of the following is true: the segment selector index is not within the descriptor table limits, the memory address of the descriptor is non-canonical, the segment selector RPL is not equal to CPL, the segment is a nonwritable data segment, or DPL is not equal to CPL.

#SS(0) If a memory operand effective address is non-canonical
#SS(Selector) If the SS register is being loaded and the segment is marked not present.
#NP(selector) If FS, or GS register is being loaded with a non-NULL segment selector and the segment is marked not present.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If source operand is not a memory location.
If the LOCK prefix is used.
**LEA—Load Effective Address**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8D /r</td>
<td>LEA r16,m</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Store effective address for m in register r16.</td>
</tr>
<tr>
<td>8D /r</td>
<td>LEA r32,m</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Store effective address for m in register r32.</td>
</tr>
<tr>
<td>REX.W + 8D /r</td>
<td>LEA r64,m</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store effective address for m in register r64.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Computes the effective address of the second operand (the source operand) and stores it in the first operand (destination operand). The source operand is a memory address (offset part) specified with one of the processors addressing modes; the destination operand is a general-purpose register. The address-size and operand-size attributes affect the action performed by this instruction, as shown in the following table. The operand-size attribute of the instruction is determined by the chosen register; the address-size attribute is determined by the attribute of the code segment.

**Table 3-63. Non-64-bit Mode LEA Operation with Address and Operand Size Attributes**

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Address Size</th>
<th>Action Performed</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>16</td>
<td>16-bit effective address is calculated and stored in requested 16-bit register destination.</td>
</tr>
<tr>
<td>16</td>
<td>32</td>
<td>32-bit effective address is calculated. The lower 16 bits of the address are stored in the requested 16-bit register destination.</td>
</tr>
<tr>
<td>32</td>
<td>16</td>
<td>16-bit effective address is calculated. The 16-bit address is zero-extended and stored in the requested 32-bit register destination.</td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>32-bit effective address is calculated and stored in the requested 32-bit register destination.</td>
</tr>
</tbody>
</table>

Different assemblers may use different algorithms based on the size attribute and symbolic reference of the source operand.
In 64-bit mode, the instruction’s destination operand is governed by operand size attribute, the default operand size is 32 bits. Address calculation is governed by address size attribute, the default address size is 64-bits. In 64-bit mode, address size of 16 bits is not encodable. See Table 3-64.

Table 3-64. 64-bit Mode LEA Operation with Address and Operand Size Attributes

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Address Size</th>
<th>Action Performed</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>32</td>
<td>32-bit effective address is calculated (using 67H prefix). The lower 16 bits of the address are stored in the requested 16-bit register destination (using 66H prefix).</td>
</tr>
<tr>
<td>16</td>
<td>64</td>
<td>64-bit effective address is calculated (default address size). The lower 16 bits of the address are stored in the requested 16-bit register destination (using 66H prefix).</td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>32-bit effective address is calculated (using 67H prefix) and stored in the requested 32-bit register destination.</td>
</tr>
<tr>
<td>32</td>
<td>64</td>
<td>64-bit effective address is calculated (default address size) and the lower 32 bits of the address are stored in the requested 32-bit register destination.</td>
</tr>
<tr>
<td>64</td>
<td>32</td>
<td>32-bit effective address is calculated (using 67H prefix), zero-extended to 64-bits, and stored in the requested 64-bit register destination (using REX.W).</td>
</tr>
<tr>
<td>64</td>
<td>64</td>
<td>64-bit effective address is calculated (default address size) and all 64-bits of the address are stored in the requested 64-bit register destination (using REX.W).</td>
</tr>
</tbody>
</table>

Operation

\[
\text{IF } \text{OperandSize} = 16 \text{ and } \text{AddressSize} = 16 \\
\text{THEN} \\
\text{DEST} \leftarrow \text{EffectiveAddress(SRC)}; (* 16-bit address *) \\
\text{ELSE IF } \text{OperandSize} = 16 \text{ and } \text{AddressSize} = 32 \\
\text{THEN} \\
\text{temp} \leftarrow \text{EffectiveAddress(SRC)}; (* 32-bit address *) \\
\text{DEST} \leftarrow \text{temp}[0:15]; (* 16-bit address *) \\
\text{FI;} \\
\text{ELSE IF } \text{OperandSize} = 32 \text{ and } \text{AddressSize} = 16 \\
\text{THEN} \\
\text{temp} \leftarrow \text{EffectiveAddress(SRC)}; (* 16-bit address *) \\
\text{DEST} \leftarrow \text{ZeroExtend(temp); (* 32-bit address *)} \\
\text{FI;} \\
\text{ELSE IF } \text{OperandSize} = 32 \text{ and } \text{AddressSize} = 32 \\
\text{THEN} \\
\text{DEST} \leftarrow \text{EffectiveAddress(SRC); (* 32-bit address *)} \\
\]
ELSE IF OperandSize = 16 and AddressSize = 64
THEN
    temp ← EffectiveAddress(SRC); (* 64-bit address *)
    DEST ← temp[0:15]; (* 16-bit address *)
ELSE IF OperandSize = 32 and AddressSize = 64
THEN
    temp ← EffectiveAddress(SRC); (* 64-bit address *)
    DEST ← temp[0:31]; (* 16-bit address *)
ELSE IF OperandSize = 64 and AddressSize = 64
THEN
    DEST ← EffectiveAddress(SRC); (* 64-bit address *)
FI;

Flags Affected
None.

Protected Mode Exceptions
#UD If source operand is not a memory location.
     If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
LEAVE—High Level Procedure Exit

**Description**

Releases the stack frame set up by an earlier ENTER instruction. The LEAVE instruction copies the frame pointer (in the EBP register) into the stack pointer register (ESP), which releases the stack space allocated to the stack frame. The old frame pointer (the frame pointer for the calling procedure that was saved by the ENTER instruction) is then popped from the stack into the EBP register, restoring the calling procedure’s stack frame.

A RET instruction is commonly executed following a LEAVE instruction to return program control to the calling procedure.

See “Procedure Calls for Block-Structured Languages” in Chapter 7 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for detailed information on the use of the ENTER and LEAVE instructions.

In 64-bit mode, the instruction’s default operation size is 64 bits; 32-bit operation cannot be encoded. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF StackAddressSize = 32
    THEN
        ESP ← EBP;
        ELSE IF StackAddressSize = 64
            THEN RSP ← RBP; FI;
        ELSE IF StackAddressSize = 16
            THEN SP ← BP; FI;
    FI;
IF OperandSize = 32

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C9</td>
<td>LEAVE</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Set SP to BP, then pop BP.</td>
</tr>
<tr>
<td>C9</td>
<td>LEAVE</td>
<td>NP</td>
<td>N.E.</td>
<td>Valid</td>
<td>Set ESP to EBP, then pop EBP.</td>
</tr>
<tr>
<td>C9</td>
<td>LEAVE</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set RSP to RBP, then pop RBP.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding
THEN EBP ← Pop();
ELSE IF OperandSize = 64
    THEN RBP ← Pop(); FI;
ELSE IF OperandSize = 16
    THEN BP ← Pop(); FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#SS(0) If the EBP register points to a location that is not within the limits of the current stack segment.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If the EBP register points to a location outside of the effective address space from 0 to FFFFH.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If the EBP register points to a location outside of the effective address space from 0 to FFFFH.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If the stack address is in a non-canonical form.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**LFENCE—Load Fence**

**Opcode** | Instruction | Op/En | 64-Bit Mode | Compat/ Leg Mode | Description
--- | --- | --- | --- | --- | ---
0F AE /5 | LFENCE | NP | Valid | Valid | Serializes load operations.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a serializing operation on all load-from-memory instructions that were issued prior the LFENCE instruction. Specifically, LFENCE does not execute until all prior instructions have completed locally, and no later instruction begins execution until LFENCE completes. In particular, an instruction that loads from memory and that precedes an LFENCE receives data from memory prior to completion of the LFENCE. (An LFENCE that follows an instruction that stores to memory might complete before the data being stored have become globally visible.) Instructions following an LFENCE may be fetched from memory before the LFENCE, but they will not execute until the LFENCE completes.

Weakly ordered memory types can be used to achieve higher processor performance through such techniques as out-of-order issue and speculative reads. The degree to which a consumer of data recognizes or knows that the data is weakly ordered varies among applications and may be unknown to the producer of this data. The LFENCE instruction provides a performance-efficient way of ensuring load ordering between routines that produce weakly-ordered results and routines that consume that data.

Processors are free to fetch and cache data speculatively from regions of system memory that use the WB, WC, and WT memory types. This speculative fetching can occur at any time and is not tied to instruction execution. Thus, it is not ordered with respect to executions of the LFENCE instruction; data can be brought into the caches speculatively just before, during, or after the execution of an LFENCE instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

Wait_On_Following_Instructions_Until(preceding_instructions_complete);

**Intel C/C++ Compiler Intrinsic Equivalent**

void _mm_lfence(void)

**Exceptions (All Modes of Operation)**

#UD If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
LGDT/LIDT—Load Global/Interrupt Descriptor Table Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 /2</td>
<td>LGDT m16&amp;32</td>
<td>M</td>
<td>N.E.</td>
<td>Valid</td>
<td>Load m into GDTR.</td>
</tr>
<tr>
<td>0F 01 /3</td>
<td>LIDT m16&amp;32</td>
<td>M</td>
<td>N.E.</td>
<td>Valid</td>
<td>Load m into IDTR.</td>
</tr>
<tr>
<td>0F 01 /2</td>
<td>LGDT m16&amp;64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load m into GDTR.</td>
</tr>
<tr>
<td>0F 01 /3</td>
<td>LIDT m16&amp;64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load m into IDTR.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Loads the values in the source operand into the global descriptor table register (GDTR) or the interrupt descriptor table register (IDTR). The source operand specifies a 6-byte memory location that contains the base address (a linear address) and the limit (size of table in bytes) of the global descriptor table (GDT) or the interrupt descriptor table (IDT). If operand-size attribute is 32 bits, a 16-bit limit (lower 2 bytes of the 6-byte data operand) and a 32-bit base address (upper 4 bytes of the data operand) are loaded into the register. If the operand-size attribute is 16 bits, a 16-bit limit (lower 2 bytes) and a 24-bit base address (third, fourth, and fifth byte) are loaded. Here, the high-order byte of the operand is not used and the high-order byte of the base address in the GDTR or IDTR is filled with zeros.

The LGDT and LIDT instructions are used only in operating-system software; they are not used in application programs. They are the only instructions that directly load a linear address (that is, not a segment-relative address) and a limit in protected mode. They are commonly executed in real-address mode to allow processor initialization prior to switching to protected mode.

In 64-bit mode, the instruction's operand size is fixed at 8+2 bytes (an 8-byte base and a 2-byte limit). See the summary chart at the beginning of this section for encoding data and limits.

See "SGDT—Store Global Descriptor Table Register" in Chapter 4, Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B, for information on storing the contents of the GDTR and IDTR.

Operation

IF Instruction is LIDT
THEN
  IF OperandSize = 16
  THEN
IDTR(Limit) ← SRC[0:15];
IDTR(Base) ← SRC[16:47] AND 00FFFFFFH;
ELSE IF 32-bit Operand Size
    THEN
        IDTR(Limit) ← SRC[0:15];
        IDTR(Base) ← SRC[16:47];
        FI;
ELSE IF 64-bit Operand Size (* In 64-Bit Mode *)
    THEN
        IDTR(Limit) ← SRC[0:15];
        IDTR(Base) ← SRC[16:79];
        FI;
FI;
ELSE (* Instruction is LGDT *)
    IF OperandSize = 16
        THEN
            GDTR(Limit) ← SRC[0:15];
            GDTR(Base) ← SRC[16:47] AND 00FFFFFFH;
        ELSE IF 32-bit Operand Size
            THEN
                GDTR(Limit) ← SRC[0:15];
                GDTR(Base) ← SRC[16:47];
                FI;
        ELSE IF 64-bit Operand Size (* In 64-Bit Mode *)
            THEN
                GDTR(Limit) ← SRC[0:15];
                GDTR(Base) ← SRC[16:79];
                FI;
        FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#UD If source operand is not a memory location.
    If the LOCK prefix is used.
#GP(0) If the current privilege level is not 0.
    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
INSTRUCTION SET REFERENCE, A-L

#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.

Real-Address Mode Exceptions
#UD If source operand is not a memory location.
If the LOCK prefix is used.
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual-8086 Mode Exceptions
#UD If source operand is not a memory location.
If the LOCK prefix is used.
#GP(0) The LGDT and LIDT instructions are not recognized in virtual-8086 mode.
#GP If the current privilege level is not 0.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the current privilege level is not 0.
If the memory address is in a non-canonical form.
#UD If source operand is not a memory location.
If the LOCK prefix is used.
#PF(fault-code) If a page fault occurs.
LLDT—Load Local Descriptor Table Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /2</td>
<td>LLDT r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Load segment selector r/m16 into LDTR.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Loads the source operand into the segment selector field of the local descriptor table register (LDTR). The source operand (a general-purpose register or a memory location) contains a segment selector that points to a local descriptor table (LDT). After the segment selector is loaded in the LDTR, the processor uses the segment selector to locate the segment descriptor for the LDT in the global descriptor table (GDT). It then loads the segment limit and base address for the LDT from the segment descriptor into the LDTR. The segment registers DS, ES, SS, FS, GS, and CS are not affected by this instruction, nor is the LDTR field in the task state segment (TSS) for the current task.

If bits 2-15 of the source operand are 0, LDTR is marked invalid and the LLDT instruction completes silently. However, all subsequent references to descriptors in the LDT (except by the LAR, VERR, VERW or LSL instructions) cause a general protection exception (#GP).

The operand-size attribute has no effect on this instruction.

The LLDT instruction is provided for use in operating-system software; it should not be used in application programs. This instruction can only be executed in protected mode or 64-bit mode.

In 64-bit mode, the operand size is fixed at 16 bits.

**Operation**

IF SRC(Offset) > descriptor table limit
   THEN #GP(segment selector); Fl;

IF segment selector is valid
   Read segment descriptor;
   IF SegmentDescriptor(Type) ≠ LDT
      THEN #GP(segment selector); Fl;
IF segment descriptor is not present
    THEN #NP(segment selector); Fl;

        LDTR(SegmentSelector) ← SRC;
        LDTR(SegmentDescriptor) ← GDTSegmentDescriptor;
ELSE LDTR ← INVALID
    Fl;

**Flags Affected**

None.

**Protected Mode Exceptions**

#GP(0)  If the current privilege level is not 0.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register contains a NULL segment selector.

#GP(selector)  If the selector operand does not point into the Global Descriptor Table or if the entry in the GDT is not a Local Descriptor Table.
        Segment selector is beyond GDT limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NP(selector)  If the LDT descriptor is not present.

#PF(fault-code)  If a page fault occurs.

#UD  If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#UD  The LLDT instruction is not recognized in real-address mode.

**Virtual-8086 Mode Exceptions**

#UD  The LLDT instruction is not recognized in virtual-8086 mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.

#GP(0)  If the current privilege level is not 0.
        If the memory address is in a non-canonical form.
LLDT—Load Local Descriptor Table Register

INSTRUCTION SET REFERENCE, A-L

#GP(selector)  If the selector operand does not point into the Global Descriptor Table or if the entry in the GDT is not a Local Descriptor Table.
Segment selector is beyond GDT limit.

#NP(selector)  If the LDT descriptor is not present.

#PF(fault-code)  If a page fault occurs.

#UD  If the LOCK prefix is used.
LMSW—Load Machine Status Word

Description
Loads the source operand into the machine status word, bits 0 through 15 of register CR0. The source operand can be a 16-bit general-purpose register or a memory location. Only the low-order 4 bits of the source operand (which contains the PE, MP, EM, and TS flags) are loaded into CR0. The PG, CD, NW, AM, WP, NE, and ET flags of CR0 are not affected. The operand-size attribute has no effect on this instruction.

If the PE flag of the source operand (bit 0) is set to 1, the instruction causes the processor to switch to protected mode. While in protected mode, the LMSW instruction cannot be used to clear the PE flag and force a switch back to real-address mode.

The LMSW instruction is provided for use in operating-system software; it should not be used in application programs. In protected or virtual-8086 mode, it can only be executed at CPL 0.

This instruction is provided for compatibility with the Intel 286 processor; programs and procedures intended to run on the Pentium 4, Intel Xeon, P6 family, Pentium, Intel486, and Intel386 processors should use the MOV (control registers) instruction to load the whole CR0 register. The MOV CR0 instruction can be used to set and clear the PE flag in CR0, allowing a procedure or program to switch between protected and real-address modes.

This instruction is a serializing instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode. Note that the operand size is fixed at 16 bits.

See "Changes to Instruction Behavior in VMX Non-Root Operation" in Chapter 25 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, for more information about the behavior of this instruction in VMX non-root operation.

Operation

\[ CR0[0:3] \leftarrow SRC[0:3]; \]
Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the current privilege level is not 0.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the current privilege level is not 0.
If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.
LOCK—Assert LOCK# Signal Prefix

Causes the processor’s LOCK# signal to be asserted during execution of the accompanying instruction (turns the instruction into an atomic instruction). In a multiprocessor environment, the LOCK# signal ensures that the processor has exclusive use of any shared memory while the signal is asserted.

Note that, in later Intel 64 and IA-32 processors (including the Pentium 4, Intel Xeon, and P6 family processors), locking may occur without the LOCK# signal being asserted. See the “IA-32 Architecture Compatibility” section below.

The LOCK prefix can be prepended only to the following instructions and only to those forms of the instructions where the destination operand is a memory operand: ADD, ADC, AND, BTC, BTR, BTS, CMPXCHG, CMPXCH8B, DEC, INC, NEG, NOT, OR, SBB, SUB, XOR, XADD, and XCHG. If the LOCK prefix is used with one of these instructions and the source operand is a memory operand, an undefined opcode exception (#UD) may be generated. An undefined opcode exception will also be generated if the LOCK prefix is used with any instruction not in the above list. The XCHG instruction always asserts the LOCK# signal regardless of the presence or absence of the LOCK prefix.

The LOCK prefix is typically used with the BTS instruction to perform a read-modify-write operation on a memory location in shared memory environment.

The integrity of the LOCK prefix is not affected by the alignment of the memory field. Memory locking is observed for arbitrarily misaligned fields.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

Beginning with the P6 family processors, when the LOCK prefix is prefixed to an instruction and the memory area being accessed is cached internally in the processor, the LOCK# signal is generally not asserted. Instead, only the processor’s cache is locked. Here, the processor’s cache coherency mechanism ensures that the
operation is carried out atomically with regards to memory. See “Effects of a Locked Operation on Internal Processor Caches” in Chapter 8 of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, the for more information on locking of caches.

**Operation**

AssertLOCK#(DurationOfAccompanyingInstruction);

**Flags Affected**

None.

**Protected Mode Exceptions**

#UD If the LOCK prefix is used with an instruction not listed: ADD, ADC, AND, BTC, BTR, BTS, CMPXCHG, CMPXCH8B, CMPXCHG16B, DEC, INC, NEG, NOT, OR, SBB, SUB, XOR, XADD, XCHG.

Other exceptions can be generated by the instruction when the LOCK prefix is applied.

**Real-Address Mode Exceptions**

Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

Same exceptions as in protected mode.
LODS/LODSB/LODSW/LODSD/LODSQ—Load String

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>LODS m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load byte at address DS:(E)SI into AL. For 64-bit mode load byte at address (R)SI into AL.</td>
</tr>
<tr>
<td>AD</td>
<td>LODS m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load word at address DS:(E)SI into AX. For 64-bit mode load word at address (R)SI into AX.</td>
</tr>
<tr>
<td>AD</td>
<td>LODS m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load dword at address DS:(E)SI into EAX. For 64-bit mode load dword at address (R)SI into EAX.</td>
</tr>
<tr>
<td>REX.W + AD</td>
<td>LODS m64</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load qword at address (R)SI into RAX.</td>
</tr>
<tr>
<td>AC</td>
<td>LODSB</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load byte at address DS:(E)SI into AL. For 64-bit mode load byte at address (R)SI into AL.</td>
</tr>
<tr>
<td>AD</td>
<td>LODSW</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load word at address DS:(E)SI into AX. For 64-bit mode load word at address (R)SI into AX.</td>
</tr>
<tr>
<td>AD</td>
<td>LODSD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Load dword at address DS:(E)SI into EAX. For 64-bit mode load dword at address (R)SI into EAX.</td>
</tr>
<tr>
<td>REX.W + AD</td>
<td>LODSQ</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load qword at address (R)SI into RAX.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Loads a byte, word, or doubleword from the source operand into the AL, AX, or EAX register, respectively. The source operand is a memory location, the address of which...
is read from the DS:ESI or the DS:SI registers (depending on the address-size attribute of the instruction, 32 or 16, respectively). The DS segment may be overridden with a segment override prefix.

At the assembly-code level, two forms of this instruction are allowed: the “explicit-operands” form and the “no-operands” form. The explicit-operands form (specified with the LODS mnemonic) allows the source operand to be specified explicitly. Here, the source operand should be a symbol that indicates the size and location of the source value. The destination operand is then automatically selected to match the size of the source operand (the AL register for byte operands, AX for word operands, and EAX for doubleword operands). This explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the source operand symbol must specify the correct type (size) of the operand (byte, word, or doubleword), but it does not have to specify the correct location. The location is always specified by the DS:(E)SI registers, which must be loaded correctly before the load string instruction is executed.

The no-operands form provides ”short forms” of the byte, word, and doubleword versions of the LODS instructions. Here also DS:(E)SI is assumed to be the source operand and the AL, AX, or EAX register is assumed to be the destination operand. The size of the source and destination operands is selected with the mnemonic: LODSB (byte loaded into register AL), LODSW (word loaded into AX), or LODSD (doubleword loaded into EAX).

After the byte, word, or doubleword is transferred from the memory location into the AL, AX, or EAX register, the (E)SI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E)SI register is incremented; if the DF flag is 1, the ESI register is decremented.) The (E)SI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

In 64-bit mode, use of the REX.W prefix promotes operation to 64 bits. LODS/LODSQ load the quadword at address (R)SI into RAX. The (R)SI register is then incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register.

The LODS, LODSB, LODSW, and LODSD instructions can be preceded by the REP prefix for block loads of ECX bytes, words, or doublewords. More often, however, these instructions are used within a LOOP construct because further processing of the data moved into the register is usually necessary before the next transfer can be made. See "REP/REPE/REPZ /REPNE/REPNZ—Repeat String Operation Prefix" in Chapter 4 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B, for a description of the REP prefix.

**Operation**

\[
\begin{align*}
\text{IF } & AL \leftarrow \text{SRC}; \quad \text{(* Byte load *)} \\
& \quad \text{THEN } AL \leftarrow \text{SRC}; \quad \text{(* Byte load *)} \\
& \quad \quad \quad \text{IF } DF = 0 \quad \text{THEN } (E)SI \leftarrow (E)SI + 1;
\end{align*}
\]
ELSE (E)SI ← (E)SI – 1;
FI;
ELSE IF AX ← SRC; (* Word load *)
THEN IF DF = 0
    THEN (E)SI ← (E)SI + 2;
    ELSE (E)SI ← (E)SI – 2;
    FI;
ELSE IF EAX ← SRC; (* Doubleword load *)
THEN IF DF = 0
    THEN (E)SI ← (E)SI + 4;
    ELSE (E)SI ← (E)SI – 4;
    FI;
ELSE IF RAX ← SRC; (* Quadword load *)
THEN IF DF = 0
    THEN (R)SI ← (R)SI + 8;
    ELSE (R)SI ← (R)SI – 8;
    FI;
FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS,
ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment
selector.
#SS(0) If a memory operand effective address is outside the SS
segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory
reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS,
ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS
segment limit.
LODS/LODSB/LODSW/LODSD/LODSQ—Load String

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
LOOP/LOOPcc—Loop According to ECX Counter

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E2 cb</td>
<td>LOOP rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement count; jump short if count ≠ 0.</td>
</tr>
<tr>
<td>E1 cb</td>
<td>LOOPE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement count; jump short if count ≠ 0 and ZF = 1.</td>
</tr>
<tr>
<td>E0 cb</td>
<td>LOOPNE rel8</td>
<td>D</td>
<td>Valid</td>
<td>Valid</td>
<td>Decrement count; jump short if count ≠ 0 and ZF = 0.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>Offset</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a loop operation using the RCX, ECX or CX register as a counter (depending on whether address size is 64 bits, 32 bits, or 16 bits). Note that the LOOP instruction ignores REX.W; but 64-bit address size can be over-ridden using a 67H prefix.

Each time the LOOP instruction is executed, the count register is decremented, then checked for 0. If the count is 0, the loop is terminated and program execution continues with the instruction following the LOOP instruction. If the count is not zero, a near jump is performed to the destination (target) operand, which is presumably the instruction at the beginning of the loop.

The target instruction is specified with a relative offset (a signed offset relative to the current value of the instruction pointer in the IP/EIP/RIP register). This offset is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed, 8-bit immediate value, which is added to the instruction pointer. Offsets of –128 to +127 are allowed with this instruction.

Some forms of the loop instruction (LOOPcc) also accept the ZF flag as a condition for terminating the loop before the count reaches zero. With these forms of the instruction, a condition code (cc) is associated with each instruction to indicate the condition being tested for. Here, the LOOPcc instruction itself does not affect the state of the ZF flag; the ZF flag is changed by other instructions in the loop.
Operation

IF (AddressSize = 32)
    THEN Count is ECX;
ELSE IF (AddressSize = 64)
    Count is RCX;
ELSE Count is CX;
FI;

Count ← Count - 1;

IF Instruction is not LOOP
    THEN
        IF (Instruction ← LOOPE) or (Instruction ← LOOPZ)
            THEN IF (ZF = 1) and (Count ≠ 0)
                THEN BranchCond ← 1;
                ELSE BranchCond ← 0;
            FI;
            ELSE (Instruction = LOOPNE) or (Instruction = LOOPNZ)
                IF (ZF = 0 ) and (Count ≠ 0)
                    THEN BranchCond ← 1;
                    ELSE BranchCond ← 0;
                FI;
        ELSE (* Instruction = LOOP *)
            IF (Count ≠ 0)
                THEN BranchCond ← 1;
                ELSE BranchCond ← 0;
            FI;
    FI;

IF BranchCond = 1
    THEN
        IF OperandSize = 32
            THEN EIP ← EIP + SignExtend(DEST);
        ELSE IF OperandSize = 64
            THEN RIP ← RIP + SignExtend(DEST);
        FI;
        ELSE IF OperandSize = 16
            THEN EIP ← EIP AND 0000FFFFH;
        FI;
        ELSE IF OperandSize = (32 or 64)
            THEN IF (R/E)IP < CS.Base or (R/E)IP > CS.Limit
                #GP; FI;
        FI;

LOOP/LOOPcc—Loop According to ECX Counter
Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the offset being jumped to is beyond the limits of the CS segment.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If the offset being jumped to is beyond the limits of the CS segment or is outside of the effective address space from 0 to FFFFH. This condition can occur if a 32-bit address size override prefix is used.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in real address mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the offset being jumped to is in a non-canonical form.
#UD If the LOCK prefix is used.
**LSL—Load Segment Limit**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 03 /r</td>
<td>LSL r16, r16/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load: r16 ← segment limit, selector r16/m16.</td>
</tr>
<tr>
<td>OF 03 /r</td>
<td>LSL r32, r32/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load: r32 ← segment limit, selector r32/m16.</td>
</tr>
<tr>
<td>REX.W + OF 03 /r</td>
<td>LSL r64, r32/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Load: r64 ← segment limit, selector r32/m16</td>
</tr>
</tbody>
</table>

**NOTES:**
* For all loads (regardless of destination sizing), only bits 16-0 are used. Other bits are ignored.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Loads the unscrambled segment limit from the segment descriptor specified with the second operand (source operand) into the first operand (destination operand) and sets the ZF flag in the EFLAGS register. The source operand (which can be a register or a memory location) contains the segment selector for the segment descriptor being accessed. The destination operand is a general-purpose register.

The processor performs access checks as part of the loading process. Once loaded in the destination register, software can compare the segment limit with the offset of a pointer.

The segment limit is a 20-bit value contained in bytes 0 and 1 and in the first 4 bits of byte 6 of the segment descriptor. If the descriptor has a byte granular segment limit (the granularity flag is set to 0), the destination operand is loaded with a byte granular value (byte limit). If the descriptor has a page granular segment limit (the granularity flag is set to 1), the LSL instruction will translate the page granular limit (page limit) into a byte limit before loading it into the destination operand. The translation is performed by shifting the 20-bit “raw” limit left 12 bits and filling the low-order 12 bits with 1s.

When the operand size is 32 bits, the 32-bit byte limit is stored in the destination operand. When the operand size is 16 bits, a valid 32-bit limit is computed; however, the upper 16 bits are truncated and only the low-order 16 bits are loaded into the destination operand.

This instruction performs the following checks before it loads the segment limit into the destination register:

* Checks that the segment selector is not NULL.
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- Checks that the segment selector points to a descriptor that is within the limits of the GDT or LDT being accessed
- Checks that the descriptor type is valid for this instruction. All code and data segment descriptors are valid for (can be accessed with) the LSL instruction. The valid special segment and gate descriptor types are given in the following table.
- If the segment is not a conforming code segment, the instruction checks that the specified segment descriptor is visible at the CPL (that is, if the CPL and the RPL of the segment selector are less than or equal to the DPL of the segment selector).

If the segment descriptor cannot be accessed or is an invalid type for the instruction, the ZF flag is cleared and no value is loaded in the destination operand.

Table 3-65. Segment and Gate Descriptor Types

<table>
<thead>
<tr>
<th>Type</th>
<th>Protected Mode</th>
<th>IA-32e Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Name</td>
<td>Valid</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>Available 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>LDT</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>Busy 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>16-bit call gate</td>
<td>No</td>
</tr>
<tr>
<td>5</td>
<td>16-bit/32-bit task gate</td>
<td>No</td>
</tr>
<tr>
<td>6</td>
<td>16-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>7</td>
<td>16-bit trap gate</td>
<td>No</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>9</td>
<td>Available 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>A</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>B</td>
<td>Busy 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>C</td>
<td>32-bit call gate</td>
<td>No</td>
</tr>
<tr>
<td>D</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>E</td>
<td>32-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>F</td>
<td>32-bit trap gate</td>
<td>No</td>
</tr>
</tbody>
</table>
Operation

IF SRC(Offset) > descriptor table limit
    THEN ZF ← 0; FI;

Read segment descriptor;

IF SegmentDescriptor(Type) ≠ conforming code segment
    and (CPL > DPL) OR (RPL > DPL)
    or Segment type is not valid for instruction
    THEN
        ZF ← 0;
    ELSE
        temp ← SegmentLimit([SRC]);
        IF (G ← 1)
            THEN temp ← ShiftLeft(12, temp) OR 00000FFFH;
        ELSE IF OperandSize = 32
            THEN DEST ← temp; FI;
        ELSE IF OperandSize = 64 (* REX.W used *)
            THEN DEST (* Zero-extended *) ← temp; FI;
        ELSE (* OperandSize = 16 *)
            DEST ← temp AND FFFFH;
    FI;
FI;

Flags Affected

The ZF flag is set to 1 if the segment limit is loaded successfully; otherwise, it is set to 0.

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and the memory operand effective address is unaligned while the current privilege level is 3.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#UD The LSL instruction cannot be executed in real-address mode.
Virtual-8086 Mode Exceptions
#UD The LSL instruction cannot be executed in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If the memory operand effective address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory operand effective address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and the memory operand effective address is unaligned while the current privilege level is 3.
#UD If the LOCK prefix is used.
LTR—Load Task Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Log Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /3</td>
<td>LTR r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Load r/m16 into task register.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

 Loads the source operand into the segment selector field of the task register. The source operand (a general-purpose register or a memory location) contains a segment selector that points to a task state segment (TSS). After the segment selector is loaded in the task register, the processor uses the segment selector to locate the segment descriptor for the TSS in the global descriptor table (GDT). It then loads the segment limit and base address for the TSS from the segment descriptor into the task register. The task pointed to by the task register is marked busy, but a switch to the task does not occur.

 The LTR instruction is provided for use in operating-system software; it should not be used in application programs. It can only be executed in protected mode when the CPL is 0. It is commonly used in initialization code to establish the first task to be executed.

 The operand-size attribute has no effect on this instruction.

 In 64-bit mode, the operand size is still fixed at 16 bits. The instruction references a 16-byte descriptor to load the 64-bit base.

**Operation**

 IF SRC is a NULL selector  
 THEN #GP(0);  

 IF SRC(Offset) > descriptor table limit OR IF SRC(type) ≠ global  
 THEN #GP(segment selector); Fl;  

 Read segment descriptor;  

 IF segment descriptor is not for an available TSS  
 THEN #GP(segment selector); Fl;  

 IF segment descriptor is not present  
 THEN #NP(segment selector); Fl;  

LTR—Load Task Register
TSSSegmentDescriptor(busy) ← 1;
(* Locked read-modify-write operation on the entire descriptor when setting busy flag *)
TaskRegister(SegmentSelector) ← SRC;
TaskRegister(SegmentDescriptor) ← TSSSegmentDescriptor;

Flags Affected
None.

Protected Mode Exceptions
- #GP(0) If the current privilege level is not 0.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the source operand contains a NULL segment selector.
- #GP(selector) If the source selector points to a segment that is not a TSS or to one for a task that is already busy.
- #NP(selector) If the TSS is marked not present.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
- #UD If the LOCK prefix is used.

Real-Address Mode Exceptions
- #UD The LTR instruction is not recognized in real-address mode.

Virtual-8086 Mode Exceptions
- #UD The LTR instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
- #SS(0) If a memory address referencing the SS segment is in a non-canonical form.
- #GP(0) If the current privilege level is not 0.
  - If the memory address is in a non-canonical form.
  - If the source operand contains a NULL segment selector.
<table>
<thead>
<tr>
<th>Opcode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP(selector)</td>
<td>If the source selector points to a segment that is not a TSS or to one for a task that is already busy.</td>
</tr>
<tr>
<td></td>
<td>If the selector points to LDT or is beyond the GDT limit.</td>
</tr>
<tr>
<td></td>
<td>If the descriptor type of the upper 8-byte of the 16-byte descriptor is non-zero.</td>
</tr>
<tr>
<td>#NP(selector)</td>
<td>If the TSS is marked not present.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#UD</td>
<td>If the LOCK prefix is used.</td>
</tr>
</tbody>
</table>
CHAPTER 4
INSTRUCTION SET REFERENCE, M-Z

4.1 IMM8 CONTROL BYTE OPERATION FOR PCMPESTRI / PCMPESTRM / PCMPISTRI / PCMPISTRM

The notations introduced in this section are referenced in the reference pages of PCMPESTRI, PCMPESTRM, PCMPISTRI, PCMPISTRM. The operation of the immediate control byte is common to these four string text processing instructions of SSE4.2. This section describes the common operations.

4.1.1 General Description

The operation of PCMPESTRI, PCMPESTRM, PCMPISTRI, PCMPISTRM is defined by the combination of the respective opcode and the interpretation of an immediate control byte that is part of the instruction encoding.

The opcode controls the relationship of input bytes/words to each other (determines whether the inputs terminated strings or whether lengths are expressed explicitly) as well as the desired output (index or mask).

The Imm8 Control Byte for PCMPESTRM/PCMPESTRI/PCMPISTRM/PCMPISTRI encodes a significant amount of programmable control over the functionality of those instructions. Some functionality is unique to each instruction while some is common across some or all of the four instructions. This section describes functionality which is common across the four instructions.

The arithmetic flags (ZF, CF, SF, OF, AF, PF) are set as a result of these instructions. However, the meanings of the flags have been overloaded from their typical meanings in order to provide additional information regarding the relationships of the two inputs.

PCMPxSTRx instructions perform arithmetic comparisons between all possible pairs of bytes or words, one from each packed input source operand. The boolean results of those comparisons are then aggregated in order to produce meaningful results. The Imm8 Control Byte is used to affect the interpretation of individual input elements as well as control the arithmetic comparisons used and the specific aggregation scheme.

Specifically, the Imm8 Control Byte consists of bit fields that control the following attributes:

- **Source data format** — Byte/word data element granularity, signed or unsigned elements
• **Aggregation operation** — Encodes the mode of per-element comparison operation and the aggregation of per-element comparisons into an intermediate result

• **Polarity** — Specifies intermediate processing to be performed on the intermediate result

• **Output selection** — Specifies final operation to produce the output (depending on index or mask) from the intermediate result

### 4.1.2 Source Data Format

Table 4-1. Source Data Format

<table>
<thead>
<tr>
<th>Imm8[1:0]</th>
<th>Meaning</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>Unsigned bytes</td>
<td>Both 128-bit sources are treated as packed, unsigned bytes.</td>
</tr>
<tr>
<td>01b</td>
<td>Unsigned words</td>
<td>Both 128-bit sources are treated as packed, unsigned words.</td>
</tr>
<tr>
<td>10b</td>
<td>Signed bytes</td>
<td>Both 128-bit sources are treated as packed, signed bytes.</td>
</tr>
<tr>
<td>11b</td>
<td>Signed words</td>
<td>Both 128-bit sources are treated as packed, signed words.</td>
</tr>
</tbody>
</table>

If the Imm8 Control Byte has bit[0] cleared, each source contains 16 packed bytes. If the bit is set each source contains 8 packed words. If the Imm8 Control Byte has bit[1] cleared, each input contains unsigned data. If the bit is set each source contains signed data.
4.1.3 Aggregation Operation

Table 4-2. Aggregation Operation

<table>
<thead>
<tr>
<th>Imm8[3:2]</th>
<th>Mode</th>
<th>Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>Equal any</td>
<td>The arithmetic comparison is “equal.”</td>
</tr>
<tr>
<td>01b</td>
<td>Ranges</td>
<td>Arithmetic comparison is “greater than or equal” between even indexed bytes/words of reg and each byte/word of reg/mem. Arithmetic comparison is “less than or equal” between odd indexed bytes/words of reg and each byte/word of reg/mem. (reg/mem[m] &gt;= reg[n] for n = even, reg/mem[m] &lt;= reg[n] for n = odd)</td>
</tr>
<tr>
<td>10b</td>
<td>Equal each</td>
<td>The arithmetic comparison is “equal.”</td>
</tr>
<tr>
<td>11b</td>
<td>Equal ordered</td>
<td>The arithmetic comparison is “equal.”</td>
</tr>
</tbody>
</table>

All 256 (64) possible comparisons are always performed. The individual Boolean results of those comparisons are referred by “BoolRes[Reg/Mem element index, Reg element index].” Comparisons evaluating to “True” are represented with a 1, False with a 0 (positive logic). The initial results are then aggregated into a 16-bit (8-bit) intermediate result (IntRes1) using one of the modes described in the table below, as determined by Imm8 Control Byte bit[3:2].
See Section 4.1.6 for a description of the overrideIfDataInvalid() function used in Table 4-3.

Table 4-3. Aggregation Operation

<table>
<thead>
<tr>
<th>Mode</th>
<th>Pseudocode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equal any (find characters from a set)</td>
<td>UpperBound = imm8[0] ? 7 : 15;</td>
</tr>
<tr>
<td></td>
<td>IntRes1 = 0;</td>
</tr>
<tr>
<td></td>
<td>For j = 0 to UpperBound, j++</td>
</tr>
<tr>
<td></td>
<td>For i = 0 to UpperBound, i++</td>
</tr>
<tr>
<td></td>
<td>IntRes1[j] OR= overrideIfDataInvalid(BoolRes[j,i])</td>
</tr>
<tr>
<td>Ranges (find characters from ranges)</td>
<td>UpperBound = imm8[0] ? 7 : 15;</td>
</tr>
<tr>
<td></td>
<td>IntRes1 = 0;</td>
</tr>
<tr>
<td></td>
<td>For j = 0 to UpperBound, j++</td>
</tr>
<tr>
<td></td>
<td>For i = 0 to UpperBound, i+=2</td>
</tr>
<tr>
<td></td>
<td>IntRes1[j] OR= (overrideIfDataInvalid(BoolRes[j,i]) AND overrideIfDataInvalid(BoolRes[j,i+1]))</td>
</tr>
<tr>
<td>Equal each (string compare)</td>
<td>UpperBound = imm8[0] ? 7 : 15;</td>
</tr>
<tr>
<td></td>
<td>IntRes1 = 0;</td>
</tr>
<tr>
<td></td>
<td>For i = 0 to UpperBound, i++</td>
</tr>
<tr>
<td></td>
<td>IntRes1[i] = overrideIfDataInvalid(BoolRes[i,i])</td>
</tr>
<tr>
<td>Equal ordered (substring search)</td>
<td>UpperBound = imm8[0] ? 7 :15;</td>
</tr>
<tr>
<td></td>
<td>IntRes1 = imm8[0] ? 0xFF : 0xFFFF</td>
</tr>
<tr>
<td></td>
<td>For j = 0 to UpperBound, j++</td>
</tr>
<tr>
<td></td>
<td>For i = 0 to UpperBound-j, k=j to UpperBound, k++, i++</td>
</tr>
<tr>
<td></td>
<td>IntRes1[j] AND= overrideIfDataInvalid(BoolRes[k,i])</td>
</tr>
</tbody>
</table>

4.1.4 Polarity

IntRes1 may then be further modified by performing a 1’s complement, according to the value of the Imm8 Control Byte bit[4]. Optionally, a mask may be used such that only those IntRes1 bits which correspond to “valid” reg/mem input elements are complemented (note that the definition of a valid input element is dependant on the specific opcode and is defined in each opcode’s description). The result of the possible negation is referred to as IntRes2.
4.1.5 Output Selection

Table 4-4. Polarity

<table>
<thead>
<tr>
<th>Imm8[5:4]</th>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>Positive Polarity (+)</td>
<td>IntRes2 = IntRes1</td>
</tr>
<tr>
<td>01b</td>
<td>Negative Polarity (-)</td>
<td>IntRes2 = -1 XOR IntRes1</td>
</tr>
<tr>
<td>10b</td>
<td>Masked (+)</td>
<td>IntRes2 = IntRes1</td>
</tr>
</tbody>
</table>

Table 4-5. Output Selection

<table>
<thead>
<tr>
<th>Imm8[6]</th>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b</td>
<td>Least significant index</td>
<td>The index returned to ECX is of the least significant set bit in IntRes2.</td>
</tr>
<tr>
<td>1b</td>
<td>Most significant index</td>
<td>The index returned to ECX is of the most significant set bit in IntRes2.</td>
</tr>
</tbody>
</table>

For PCMPESTRI/PCMPISTRI, the Imm8 Control Byte bit[6] is used to determine if the index is of the least significant or most significant bit of IntRes2.

Table 4-6. Output Selection

<table>
<thead>
<tr>
<th>Imm8[6]</th>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b</td>
<td>Bit mask</td>
<td>IntRes2 is returned as the mask to the least significant bits of XMM0 with zero extension to 128 bits.</td>
</tr>
<tr>
<td>1b</td>
<td>Byte/word mask</td>
<td>IntRes2 is expanded into a byte/word mask (based on imm8[1]) and placed in XMM0. The expansion is performed by replicating each bit into all of the bits of the byte/word of the same index.</td>
</tr>
</tbody>
</table>

Specifically for PCMPESTRM/PCMPISTRM, the Imm8 Control Byte bit[6] is used to determine if the mask is a 16 (8) bit mask or a 128 bit byte/word mask.
4.1.6 Valid/Invalid Override of Comparisons

PCMPxSTRx instructions allow for the possibility that an end-of-string (EOS) situation may occur within the 128-bit packed data value (see the instruction descriptions below for details). Any data elements on either source that are determined to be past the EOS are considered to be invalid, and the treatment of invalid data within a comparison pair varies depending on the aggregation function being performed.

In general, the individual comparison result for each element pair BoolRes[i,j] can be forced true or false if one or more elements in the pair are invalid. See Table 4-7.

<table>
<thead>
<tr>
<th>xmm1 byte/word</th>
<th>xmm2/m128 byte/word</th>
<th>Imm8[3:2] = 00b (equal any)</th>
<th>Imm8[3:2] = 01b (ranges)</th>
<th>Imm8[3:2] = 10b (equal each)</th>
<th>Imm8[3:2] = 11b (equal ordered)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invalid</td>
<td>Invalid</td>
<td>Force false</td>
<td>Force false</td>
<td>Force true</td>
<td>Force true</td>
</tr>
<tr>
<td>Invalid</td>
<td>Valid</td>
<td>Force false</td>
<td>Force false</td>
<td>Force false</td>
<td>Force true</td>
</tr>
<tr>
<td>Valid</td>
<td>Invalid</td>
<td>Force false</td>
<td>Force false</td>
<td>Force false</td>
<td>Force false</td>
</tr>
<tr>
<td>Valid</td>
<td>Valid</td>
<td>Do not force</td>
<td>Do not force</td>
<td>Do not force</td>
<td>Do not force</td>
</tr>
</tbody>
</table>

Table 4-7. Comparison Result for Each Element Pair BoolRes[i,j]
### 4.1.7 Summary of Imm8 Control byte

#### Table 4-8. Summary of Imm8 Control Byte

<table>
<thead>
<tr>
<th>Imm8</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>------0b</td>
<td>128-bit sources treated as 16 packed bytes.</td>
</tr>
<tr>
<td>------1b</td>
<td>128-bit sources treated as 8 packed words.</td>
</tr>
<tr>
<td>------0-b</td>
<td>Packed bytes/words are unsigned.</td>
</tr>
<tr>
<td>------1-b</td>
<td>Packed bytes/words are signed.</td>
</tr>
<tr>
<td>----00-b</td>
<td>Mode is equal any.</td>
</tr>
<tr>
<td>----01-b</td>
<td>Mode is ranges.</td>
</tr>
<tr>
<td>----10-b</td>
<td>Mode is equal each.</td>
</tr>
<tr>
<td>----11-b</td>
<td>Mode is equal ordered.</td>
</tr>
<tr>
<td>----0----b</td>
<td>IntRes1 is unmodified.</td>
</tr>
<tr>
<td>----1----b</td>
<td>IntRes1 is negated (1’s complement).</td>
</tr>
<tr>
<td>---0-----b</td>
<td>Negation of IntRes1 is for all 16 (8) bits.</td>
</tr>
<tr>
<td>---1-----b</td>
<td>Negation of IntRes1 is masked by reg/mem validity.</td>
</tr>
<tr>
<td>-0------b</td>
<td>Index of the least significant, set, bit is used (regardless of corresponding input element validity). IntRes2 is returned in least significant bits of XMM0.</td>
</tr>
<tr>
<td>-1------b</td>
<td>Index of the most significant, set, bit is used (regardless of corresponding input element validity). Each bit of IntRes2 is expanded to byte/word.</td>
</tr>
<tr>
<td>0------b</td>
<td>This bit currently has no defined effect, should be 0.</td>
</tr>
<tr>
<td>1------b</td>
<td>This bit currently has no defined effect, should be 0.</td>
</tr>
</tbody>
</table>
4.1.8 Diagram Comparison and Aggregation Process

4.2 INSTRUCTIONS (M-Z)

MASKMOVDQU—Store Selected Bytes of Double Quadword

**Op/En Instruction** | **Op En** | **64/32-bit Mode** | **CPUID Feature Flag** | **Description**
---|---|---|---|---
66 0F F7 /r | RM | V/V | SSE2 | Selectively write bytes from \( xmm1 \) to memory location using the byte mask in \( xmm2 \). The default memory location is specified by DS:EDI/RDI.
VEX.128.66.0F:WIG F7 /r | RM | V/V | AVX | Selectively write bytes from \( xmm1 \) to memory location using the byte mask in \( xmm2 \). The default memory location is specified by DS:DI/EDI/RDI.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Stores selected bytes from the source operand (first operand) into an 128-bit memory location. The mask operand (second operand) selects which bytes from the source operand are written to memory. The source and mask operands are XMM registers. The memory location specified by the effective address in the DI/EDI/RDI register (the default segment register is DS, but this may be overridden with a segment-override prefix). The memory location does not need to be aligned on a natural boundary. (The size of the store address depends on the address-size attribute.)

The most significant bit in each byte of the mask operand determines whether the corresponding byte in the source operand is written to the corresponding byte location in memory: 0 indicates no write and 1 indicates write.

The MASKMOVDQU instruction generates a non-temporal hint to the processor to minimize cache pollution. The non-temporal hint is implemented by using a write combining (WC) memory type protocol (see "Caching of Temporal vs. Non-Temporal Data" in Chapter 10, of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MASKMOVDQU instructions if multiple

1.ModRM.MOD = 011B required
processors might use different memory types to read/write the destination memory locations.

Behavior with a mask of all 0s is as follows:

- No data will be written to memory.
- Signaling of breakpoints (code or data) is not guaranteed; different processor implementations may signal or not signal these breakpoints.
- Exceptions associated with addressing memory and page faults may still be signaled (implementation dependent).
- If the destination memory region is mapped as UC or WP, enforcement of associated semantics for these memory types is not guaranteed (that is, is reserved) and is implementation-specific.

The MASKMOVDQU instruction can be used to improve performance of algorithms that need to merge data on a byte-by-byte basis. MASKMOVDQU should not cause a read for ownership; doing so generates unnecessary bandwidth since data is to be written directly using the byte-mask without allocating old data prior to the store.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

If VMASKMOVDQU is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.

**Operation**

IF (MASK[7] = 1)
    THEN DEST[DI/EDI] ← SRC[7:0] ELSE (* Memory location unchanged *); Fl;
IF (MASK[15] = 1)
    THEN DEST[DI/EDI +1] ← SRC[15:8] ELSE (* Memory location unchanged *); Fl;
    (* Repeat operation for 3rd through 14th bytes in source operand *)
IF (MASK[127] = 1)
    THEN DEST[DI/EDI +15] ← SRC[127:120] ELSE (* Memory location unchanged *); Fl;

**Intel C/C++ Compiler Intrinsic Equivalent**

`void _mm_maskmoveu_si128(__m128i d, __m128i n, char * p)`

**Other Exceptions**

See Exceptions Type 4; additionally

#UD
    If VEX.L= 1
    If VEX.vvvv != 1111B.
MASKMOVQ—Store Selected Bytes of Quadword

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F F7 r</td>
<td>MASKMOVQ mm1, mm2</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Selectively write bytes from mm1 to memory location using the byte mask in mm2. The default memory location is specified by DS:DI/EDI/RDI.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Stores selected bytes from the source operand (first operand) into a 64-bit memory location. The mask operand (second operand) selects which bytes from the source operand are written to memory. The source and mask operands are MMX technology registers. The memory location specified by the effective address in the DI/EDI/RDI register (the default segment register is DS, but this may be overridden with a segment-override prefix). The memory location does not need to be aligned on a natural boundary. (The size of the store address depends on the address-size attribute.)

The most significant bit in each byte of the mask operand determines whether the corresponding byte in the source operand is written to the corresponding byte location in memory: 0 indicates no write and 1 indicates write.

The MASKMOVQ instruction generates a non-temporal hint to the processor to minimize cache pollution. The non-temporal hint is implemented by using a write combining (WC) memory type protocol (see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10, of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MASKMOVQ instructions if multiple processors might use different memory types to read/write the destination memory locations.

This instruction causes a transition from x87 FPU to MMX technology state (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]).

The behavior of the MASKMOVQ instruction with a mask of all 0s is as follows:

- No data will be written to memory.
- Transition from x87 FPU to MMX technology state will occur.

MASKMOVQ—Store Selected Bytes of Quadword
INSTRUCTION SET REFERENCE, M-Z

• Exceptions associated with addressing memory and page faults may still be signaled (implementation dependent).
• Signaling of breakpoints (code or data) is not guaranteed (implementation dependent).
• If the destination memory region is mapped as UC or WP, enforcement of associated semantics for these memory types is not guaranteed (that is, is reserved) and is implementation-specific.

The MASKMOVQ instruction can be used to improve performance for algorithms that need to merge data on a byte-by-byte basis. It should not cause a read for ownership; doing so generates unnecessary bandwidth since data is to be written directly using the byte-mask without allocating old data prior to the store.

In 64-bit mode, the memory address is specified by DS:RDI.

Operation

IF (MASK[7] = 1)
   THEN DEST[DI/EDI] ← SRC[7:0] ELSE (* Memory location unchanged *); FI;
IF (MASK[15] = 1)
   THEN DEST[DI/EDI +1] ← SRC[15:8] ELSE (* Memory location unchanged *); FI;
   (* Repeat operation for 3rd through 6th bytes in source operand *)
IF (MASK[63] = 1)
   THEN DEST[DI/EDI +15] ← SRC[63:56] ELSE (* Memory location unchanged *); FI;

Intel C/C++ Compiler Intrinsic Equivalent

void _mm_maskmove_si64(__m64d, __m64n, char * p)

Other Exceptions

See Table 22-8, “Exception Conditions for Legacy SIMD/MMX Instructions without FP Exception,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.
MAXPD—Return Maximum Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 5F /r MAXPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Return the maximum double-precision floating-point values between xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 5F /r VMAXPD xmm1,xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the maximum double-precision floating-point values between xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 5F /r VMAXPD ymm1, ymm2, ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the maximum packed double-precision floating-point values between ymm2 and ymm3/mem.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs an SIMD compare of the packed double-precision floating-point values in the first source operand and the second source operand and returns the maximum value for each pair of values to the destination operand.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is a NaN, that NaN is forwarded unchanged to the destination (that is, a QNaN version of the NaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MAXPD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register.
and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

MAX(SRC1, SRC2)

```
{ 
  IF ((SRC1 = 0.0) and (SRC2 = 0.0)) THEN DEST ← SRC2;
  ELSE IF (SRC1 = SNaN) THEN DEST ← SRC2; FI;
  ELSE IF (SRC2 = SNaN) THEN DEST ← SRC2; FI;
  ELSE IF (SRC1 > SRC2) THEN DEST ← SRC1;
  ELSE DEST ← SRC2;
  FI;
}
```

**MAXPD (128-bit Legacy SSE version)**

```
DEST[63:0] ← MAX(DEST[63:0], SRC[63:0])
DEST[127:64] ← MAX(DEST[127:64], SRC[127:64])
DEST[VLMAX-1:128] (Unmodified)
```

**VMAXPD (VEX.128 encoded version)**

```
DEST[63:0] ← MAX(SRC1[63:0], SRC2[63:0])
DEST[127:64] ← MAX(SRC1[127:64], SRC2[127:64])
DEST[VLMAX-1:128] ← 0
```

**VMAXPD (VEX.256 encoded version)**

```
DEST[63:0] ← MAX(SRC1[63:0], SRC2[63:0])
DEST[127:64] ← MAX(SRC1[127:64], SRC2[127:64])
DEST[255:192] ← MAX(SRC1[255:192], SRC2[255:192])
```

**Intel C/C++ Compiler Intrinsic Equivalent**

**MAXPD:**  `__m128d _mm_max_pd(__m128d a, __m128d b);`

**VMAXPD:**  `__m256d _mm256_max_pd(__m256d a, __m256d b);`
**SIMD Floating-Point Exceptions**
Invalid (including QNaN source operand), Denormal.

**Other Exceptions**
See Exceptions Type 2.
MAXPS—Return Maximum Packed Single-Precision Floating-Point Values

Description
Performs an SIMD compare of the packed single-precision floating-point values in the first source operand and the second source operand and returns the maximum value for each pair of values to the destination operand.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is forwarded unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MAXPS can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register.
and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

MAX(SRC1, SRC2)
{
    IF ((SRC1 = 0.0) and (SRC2 = 0.0)) THEN DEST ← SRC2;
    ELSE IF (SRC1 = SNaN) THEN DEST ← SRC2; FI;
    ELSE IF SRC2 = SNaN) THEN DEST ← SRC2; FI;
    ELSE IF (SRC1 > SRC2) THEN DEST ← SRC1;
    ELSE DEST ← SRC2;
    FI;
}

**MAXPS (128-bit Legacy SSE version)**
DEST[31:0] ← MAX(DEST[31:0], SRC[31:0])
DEST[63:32] ← MAX(DEST[63:32], SRC[63:32])
DEST[95:64] ← MAX(DEST[95:64], SRC[95:64])
DEST[127:96] ← MAX(DEST[127:96], SRC[127:96])
DEST[VLMAX-1:128] (Unmodified)

**VMAXPS (VEX.128 encoded version)**
DEST[31:0] ← MAX(SRC1[31:0], SRC2[31:0])
DEST[63:32] ← MAX(SRC1[63:32], SRC2[63:32])
DEST[95:64] ← MAX(SRC1[95:64], SRC2[95:64])
DEST[127:96] ← MAX(SRC1[127:96], SRC2[127:96])
DEST[VLMAX-1:128] ← 0

**VMAXPS (VEX.256 encoded version)**
DEST[31:0] ← MAX(SRC1[31:0], SRC2[31:0])
DEST[63:32] ← MAX(SRC1[63:32], SRC2[63:32])
DEST[95:64] ← MAX(SRC1[95:64], SRC2[95:64])
DEST[127:96] ← MAX(SRC1[127:96], SRC2[127:96])
DEST[159:128] ← MAX(SRC1[159:128], SRC2[159:128])
DEST[191:160] ← MAX(SRC1[191:160], SRC2[191:160])
INSTRUCTION SET REFERENCE, M-Z

DEST[255:224] ← MAX(SRC1[255:224], SRC2[255:224])

Intel C/C++ Compiler Intrinsic Equivalent
MAXPS:  __m128 _mm_max_ps (__m128 a, __m128 b);
VMAXPS:  __m256 _mm256_max_ps (__m256 a, __m256 b);

SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Other Exceptions
See Exceptions Type 2.
MAXSD—Return Maximum Scalar Double-Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 5F /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Return the maximum scalar double-precision floating-point value between xmm2/mem64 and xmm1.</td>
</tr>
<tr>
<td>MAXSD xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F:W1G 5F /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the maximum scalar double-precision floating-point value between xmm3/mem64 and xmm2.</td>
</tr>
<tr>
<td>VMAXSD xmm1, xmm2, xmm3/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Compares the low double-precision floating-point values in the first source operand and second the source operand, and returns the maximum value to the low quadword of the destination operand. The second source operand can be an XMM register or a 64-bit memory location. The first source and destination operands are XMM registers. When the second source operand is a memory operand, only 64 bits are accessed. The high quadword of the destination operand is copied from the same bits of first source operand.

If the values being compared are both 0.0s (of either sign), the value in the second source operand is returned. If a value in the second source operand is an NaN, that NaN is returned unchanged to the destination (that is, a QNaN version of the NaN is not returned).

If only one value is a NaN (SNan or QNaN) for this instruction, the second source operand, either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN of either source operand be returned, the action of MAXSD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

The second source operand can be an XMM register or a 64-bit memory location. The first source and destination operands are XMM registers.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
INSTRUCTION SET REFERENCE, M-Z

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VLMAX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:64) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Operation

MAX(SRC1, SRC2)
{
   IF ((SRC1 = 0.0) and (SRC2 = 0.0)) THEN DEST ← SRC2;
   ELSE IF (SRC1 = SNaN) THEN DEST ← SRC2; FI;
   ELSE IF SRC2 = SNaN) THEN DEST ← SRC2; FI;
   ELSE IF (SRC1 > SRC2) THEN DEST ← SRC1;
   ELSE DEST ← SRC2;
   FI;
}

MAXSD (128-bit Legacy SSE version)
DEST[63:0] ← MAX(DEST[63:0], SRC[63:0])
DEST[VLMAX-1:64] (Unmodified)

VMAXSD (VEX.128 encoded version)
DEST[63:0] ← MAX(SRC1[63:0], SRC2[63:0])
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
MAXSD:     __m128d _mm_max_sd(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Other Exceptions
See Exceptions Type 3.
MAXSS—Return Maximum Scalar Single-Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 5F /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Return the maximum scalar single-precision floating-point value between xmm2/mem32 and xmm1.</td>
</tr>
<tr>
<td>MAXSS xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.WIG 5F /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the maximum scalar single-precision floating-point value between xmm3/mem32 and xmm2.</td>
</tr>
<tr>
<td>VMAXSS xmm1, xmm2, xmm3/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Compares the low single-precision floating-point values in the first source operand and the second source operand, and returns the maximum value to the low double-word of the destination operand.

If the values being compared are both 0.0s (of either sign), the value in the second source operand is returned. If a value in the second source operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second source operand, either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN from either source operand be returned, the action of MAXSS can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

The second source operand can be an XMM register or a 32-bit memory location. The first source and destination operands are XMM registers.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:32) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed.
INSTRUCTION SET REFERENCE, M-Z

Operation

MAX(SRC1, SRC2)
{
  IF ((SRC1 = 0.0) and (SRC2 = 0.0)) THEN DEST ← SRC2;
  ELSE IF (SRC1 = SNaN) THEN DEST ← SRC2; FI;
  ELSE IF SRC2 = SNaN) THEN DEST ← SRC2; FI;
  ELSE IF (SRC1 > SRC2) THEN DEST ← SRC1;
  ELSE DEST ← SRC2;
  FI;
}

MAXSS (128-bit Legacy SSE version)
DEST[31:0] ← MAX(DEST[31:0], SRC[31:0])
DEST[VLMAX-1:32] (Unmodified)

VMAXSS (VEX.128 encoded version)
DEST[31:0] ← MAX(SRC1[31:0], SRC2[31:0])
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
__m128d _mm_max_ss(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Other Exceptions
See Exceptions Type 3.
**MFENCE—Memory Fence**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Log Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /6</td>
<td>MFENCE</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Serializes load and store operations.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a serializing operation on all load-from-memory and store-to-memory instructions that were issued prior the MFENCE instruction. This serializing operation guarantees that every load and store instruction that precedes the MFENCE instruction in program order becomes globally visible before any load or store instruction that follows the MFENCE instruction. The MFENCE instruction is ordered with respect to all load and store instructions, other MFENCE instructions, any LFENCE and SFENCE instructions, and any serializing instructions (such as the CPUID instruction). MFENCE does not serialize the instruction stream.

Weakly ordered memory types can be used to achieve higher processor performance through such techniques as out-of-order issue, speculative reads, write-combining, and write-collapsing. The degree to which a consumer of data recognizes or knows that the data is weakly ordered varies among applications and may be unknown to the producer of this data. The MFENCE instruction provides a performance-efficient way of ensuring load and store ordering between routines that produce weakly-ordered results and routines that consume that data.

Processors are free to fetch and cache data speculatively from regions of system memory that use the WB, WC, and WT memory types. This speculative fetching can occur at any time and is not tied to instruction execution. Thus, it is not ordered with respect to executions of the MFENCE instruction; data can be brought into the caches speculatively just before, during, or after the execution of an MFENCE instruction. Processors are free to fetch and cache data speculatively from regions of system memory that use the WB, WC, and WT memory types. This speculative fetching can occur at any time and is not tied to instruction execution. Thus, it is not ordered with respect to executions of the MFENCE instruction; data can be brought into the caches speculatively just before, during, or after the execution of an MFENCE instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

---

1. A load instruction is considered to become globally visible when the value to be loaded into its destination register is determined.
INSTRUCTION SET REFERENCE, M-Z

Operation
Wait_On_Following_Loads_And_Stores_Until(preceding_loads_and_stores_globally_visible);

Intel C/C++ Compiler Intrinsic Equivalent
void _mm_mfence(void)

Exceptions (All Modes of Operation)
#UD If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
MINPD—Return Minimum Packed Double-Precision Floating-Point Values

**VARCHAR**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 5D /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Return the minimum double-precision floating-point values between xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>MINPD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 5D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the minimum double-precision floating-point values between xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VMINPD xmm1,xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 5D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the minimum packed double-precision floating-point values between ymm2 and ymm3/mem.</td>
</tr>
<tr>
<td>VMINPD ymm1, ymm2, ymm3/m256</td>
<td></td>
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<td></td>
<td></td>
</tr>
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**Instruction Encoding**

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<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an SIMD compare of the packed double-precision floating-point values in the first source operand and the second source operand and returns the minimum value for each pair of values to the destination operand.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is a NaN, that NaN is forwarded unchanged to the destination (that is, a QNaN version of the NaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MINPD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register.
MINPD—Return Minimum Packed Double-Precision Floating-Point Values

and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

Operation

MIN(SRC1, SRC2)
{
  IF ((SRC1 = 0.0) and (SRC2 = 0.0)) THEN DEST ← SRC2;
  ELSE IF (SRC1 = SNaN) THEN DEST ← SRC2; FI;
  ELSE IF (SRC2 = SNaN) THEN DEST ← SRC2; FI;
  ELSE IF (SRC1 < SRC2) THEN DEST ← SRC1;
  ELSE DEST ← SRC2;
  FI;
}

MINPD (128-bit Legacy SSE version)
DEST[63:0] ← MIN(SRC1[63:0], SRC2[63:0])
DEST[127:64] ← MIN(SRC1[127:64], SRC2[127:64])
DEST[VLMAX-1:128] (Unmodified)

VMINPD (VEX.128 encoded version)
DEST[63:0] ← MIN(SRC1[63:0], SRC2[63:0])
DEST[127:64] ← MIN(SRC1[127:64], SRC2[127:64])
DEST[VLMAX-1:128] ← 0

VMINPD (VEX.256 encoded version)
DEST[63:0] ← MIN(SRC1[63:0], SRC2[63:0])
DEST[127:64] ← MIN(SRC1[127:64], SRC2[127:64])
DEST[255:192] ← MIN(SRC1[255:192], SRC2[255:192])

Intel C/C++ Compiler Intrinsic Equivalent
MINPD:  __m128d _mm_min_pd(__m128d a, __m128d b);
VMINPD:  __m256d _mm256_min_pd (__m256d a, __m256d b);

SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.
Other Exceptions
See Exceptions Type 2.
MINPS—Return Minimum Packed Single-Precision Floating-Point Values

**Opcode/Instruction** | **Op/En** | **64/32-bit Mode** | **CPUID Feature Flag** | **Description**
--- | --- | --- | --- | ---
0F 5D /r | RM | V/V | SSE | Return the minimum single-precision floating-point values between xmm2/m128 and xmm1.
VEX.NDS.128.0F.WIG 5D /r | RVM | V/V | AVX | Return the minimum single-precision floating-point values between xmm2 and xmm3/mem.
VEX.NDS.256.0F.WIG 5D /r | RVM | V/V | AVX | Return the minimum single double-precision floating-point values between ymm2 and ymm3/mem.

**Instruction Operand Encoding**

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<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an SIMD compare of the packed single-precision floating-point values in the first source operand and the second source operand and returns the minimum value for each pair of values to the destination operand.

If the values being compared are both 0.0s (of either sign), the value in the second operand (source operand) is returned. If a value in the second operand is an SNaN, that SNaN is forwarded unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second operand (source operand), either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second operand) be returned, the action of MINPS can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register.
and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

\[
\text{MIN(SRC1, SRC2)}
\]

\[
\begin{align*}
\text{IF } (\text{SRC1} = 0.0) \text{ and } (\text{SRC2} = 0.0) \text{ THEN } \text{DEST} & \leftarrow \text{SRC2}; \\
\text{ELSE IF } (\text{SRC1} = \text{SNaN}) \text{ THEN } \text{DEST} & \leftarrow \text{SRC2}; \text{ FI;}
\end{align*}
\]

\[
\begin{align*}
\text{ELSE IF } (\text{SRC2} = \text{SNaN}) \text{ THEN } \text{DEST} & \leftarrow \text{SRC2}; \text{ FI;}
\end{align*}
\]

\[
\begin{align*}
\text{ELSE IF } (\text{SRC1} < \text{SRC2}) \text{ THEN } \text{DEST} & \leftarrow \text{SRC1};
\end{align*}
\]

\[
\text{ELSE } \text{DEST} \leftarrow \text{SRC2};
\]

\[\text{FI;}\]

**MINPS (128-bit Legacy SSE version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{MIN(SRC1}[31:0], \text{SRC2}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{MIN(SRC1}[63:32], \text{SRC2}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{MIN(SRC1}[95:64], \text{SRC2}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{MIN(SRC1}[127:96], \text{SRC2}[127:96]) \\
\text{DEST}[VLMAX-1:128] & \leftarrow 0
\end{align*}
\]

**VMINPS (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{MIN(SRC1}[31:0], \text{SRC2}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{MIN(SRC1}[63:32], \text{SRC2}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{MIN(SRC1}[95:64], \text{SRC2}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{MIN(SRC1}[127:96], \text{SRC2}[127:96]) \\
\text{DEST}[VLMAX-1:128] & \leftarrow 0
\end{align*}
\]

**VMINPS (VEX.256 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{MIN(SRC1}[31:0], \text{SRC2}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{MIN(SRC1}[63:32], \text{SRC2}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{MIN(SRC1}[95:64], \text{SRC2}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{MIN(SRC1}[127:96], \text{SRC2}[127:96]) \\
\text{DEST}[159:128] & \leftarrow \text{MIN(SRC1}[159:128], \text{SRC2}[159:128]) \\
\text{DEST}[191:160] & \leftarrow \text{MIN(SRC1}[191:160], \text{SRC2}[191:160]) \\
\text{DEST}[223:192] & \leftarrow \text{MIN(SRC1}[223:192], \text{SRC2}[223:192])
\end{align*}
\]
MINPS—Return Minimum Packed Single-Precision Floating-Point Values

\[ \text{DEST}[255:224] \leftarrow \min(\text{SRC1}[255:224], \text{SRC2}[255:224]) \]

**Intel C/C++ Compiler Intrinsic Equivalent**

- **MINPS**: `__m128d _mm_min_ps(__m128d a, __m128d b);
- **VMINPS**: `__m256 _mm256_min_ps (__m256 a, __m256 b);

**SIMD Floating-Point Exceptions**

Invalid (including QNaN source operand), Denormal.

**Other Exceptions**

See Exceptions Type 2.
MINSD—Return Minimum Scalar Double-Precision Floating-Point Value

<table>
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<tr>
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<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.NDS.LIG.F2.0F.WIG 5D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the minimum scalar double precision floating-point value between xmm3/mem64 and xmm2.</td>
</tr>
<tr>
<td>MINSD xmm1, xmm2/m64</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Return the minimum scalar double-precision floating-point value between xmm2/mem64 and xmm1.</td>
</tr>
</tbody>
</table>

**Description**

Compares the low double-precision floating-point values in the first source operand and the second source operand, and returns the minimum value to the low quadword of the destination operand. When the source operand is a memory operand, only the 64 bits are accessed. The high quadword of the destination operand is copied from the same bits in the first source operand.

If the values being compared are both 0.0s (of either sign), the value in the second source operand is returned. If a value in the second source operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second source operand, either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN source operand (from either the first or second source) be returned, the action of MINSD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

The second source operand can be an XMM register or a 64-bit memory location. The first source and destination operands are XMM registers.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VLMAX-1:64) of the corresponding YMM destination register remain unchanged.
VEX.128 encoded version: Bits (127:64) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

```
MIN(SRC1, SRC2)
{
    IF ((SRC1 = 0.0) and (SRC2 = 0.0)) THEN DEST ← SRC2;
    ELSE IF (SRC1 = SNaN) THEN DEST ← SRC2; FI;
    ELSE IF SRC2 = SNaN) THEN DEST ← SRC2; FI;
    ELSE IF (SRC1 < SRC2) THEN DEST ← SRC1;
    ELSE DEST ← SRC2;
    FI;
}
```

**MINSD (128-bit Legacy SSE version)**

```
DEST[63:0] ← MIN(SRC1[63:0], SRC2[63:0])
DEST[VLMAX-1:64] (Unmodified)
```

**MINSD (VEX.128 encoded version)**

```
DEST[63:0] ← MIN(SRC1[63:0], SRC2[63:0])
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0
```

**Intel C/C++ Compiler Intrinsic Equivalent**

```
MINSD:       __m128d _mm_min_sd(__m128d a, __m128d b)
```

**SIMD Floating-Point Exceptions**

Invalid (including QNaN source operand), Denormal.

**Other Exceptions**

See Exceptions Type 3.
MINSS—Return Minimum Scalar Single-Precision Floating-Point Value

### Opcode/Instruction

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<tbody>
<tr>
<td>F3 0F 5D /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Return the minimum scalar single-precision floating-point value between xmm2/mem32 and xmm1.</td>
</tr>
<tr>
<td>MINSS xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F:WIG 5D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the minimum scalar single precision floating-point value between xmm3/mem32 and xmm2.</td>
</tr>
<tr>
<td>VMINSS xmm1,xmm2, xmm3/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Compares the low single-precision floating-point values in the first source operand and the second source operand and returns the minimum value to the low double-word of the destination operand.

If the values being compared are both 0.0s (of either sign), the value in the second source operand is returned. If a value in the second operand is an SNaN, that SNaN is returned unchanged to the destination (that is, a QNaN version of the SNaN is not returned).

If only one value is a NaN (SNaN or QNaN) for this instruction, the second source operand, either a NaN or a valid floating-point value, is written to the result. If instead of this behavior, it is required that the NaN in either source operand be returned, the action of MINSD can be emulated using a sequence of instructions, such as, a comparison followed by AND, ANDN and OR.

The second source operand can be an XMM register or a 32-bit memory location. The first source and destination operands are XMM registers.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:32) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VMAX-1:128) of the destination YMM register are zeroed.
INSTRUCTION SET REFERENCE, M-Z

Operation

MIN(SRC1, SRC2)
{
    IF ((SRC1 = 0.0) and (SRC2 = 0.0)) THEN DEST ← SRC2;
    ELSE IF (SRC1 = SNaN) THEN DEST ← SRC2; FI;
    ELSE IF SRC2 = SNaN) THEN DEST ← SRC2; FI;
    ELSE IF (SRC1 < SRC2) THEN DEST ← SRC1;
    ELSE DEST ← SRC2;
    FI;
}

MINSS (128-bit Legacy SSE version)
DEST[31:0] ← MIN(SRC1[31:0], SRC2[31:0])
DEST[VLMAX-1:32] (Unmodified)

VMINSS (VEX.128 encoded version)
DEST[31:0] ← MIN(SRC1[31:0], SRC2[31:0])
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
MINSS: __m128d _mm_min_ss(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid (including QNaN source operand), Denormal.

Other Exceptions
See Exceptions Type 3.
MONITOR—Set Up Monitor Address

<table>
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<tr>
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<tbody>
<tr>
<td>0F 01 C8</td>
<td>MONITOR</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Sets up a linear address range to be monitored by hardware and activates the monitor. The address range should be a write-back memory caching type. The address is DS:EAX (DS:RAX in 64-bit mode).</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

The MONITOR instruction arms address monitoring hardware using an address specified in EAX (the address range that the monitoring hardware checks for store operations can be determined by using CPUID). A store to an address within the specified address range triggers the monitoring hardware. The state of monitor hardware is used by MWAIT.

The content of EAX is an effective address (in 64-bit mode, RAX is used). By default, the DS segment is used to create a linear address that is monitored. Segment overrides can be used.

ECX and EDX are also used. They communicate other information to MONITOR. ECX specifies optional extensions. EDX specifies optional hints; it does not change the architectural behavior of the instruction. For the Pentium 4 processor (family 15, model 3), no extensions or hints are defined. Undefined hints in EDX are ignored by the processor; undefined extensions in ECX raises a general protection fault.

The address range must use memory of the write-back type. Only write-back memory will correctly trigger the monitoring hardware. Additional information on determining what address range to use in order to prevent false wake-ups is described in Chapter 8, “Multiple-Processor Management” of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

The MONITOR instruction is ordered as a load operation with respect to other memory transactions. The instruction is subject to the permission checking and faults associated with a byte load. Like a load, MONITOR sets the A-bit but not the D-bit in page tables.

The MONITOR CPUID feature flag (ECX bit 3; CPUID executed EAX = 1) indicates the availability of MONITOR and MWAIT in the processor. When set, MONITOR may be
executed only at privilege level 0 (use at any other privilege level results in an invalid-opcode exception). The operating system or system BIOS may disable this instruction by using the IA32_MISC_ENABLE MSR; disabling MONITOR clears the CPUID feature flag and causes execution to generate an illegal opcode exception. The instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

MONITOR sets up an address range for the monitor hardware using the content of EAX (RAX in 64-bit mode) as an effective address and puts the monitor hardware in armed state. Always use memory of the write-back caching type. A store to the specified address range will trigger the monitor hardware. The content of ECX and EDX are used to communicate other information to the monitor hardware.

**Intel C/C++ Compiler Intrinsic Equivalent**

MONITOR: void _mm_monitor(void const *p, unsigned extensions,unsigned hints)

**Numeric Exceptions**

None

**Protected Mode Exceptions**

#GP(0)  If the value in EAX is outside the CS, DS, ES, FS, or GS segment limit.
          If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
          If ECX ≠ 0.

#SS(0)  If the value in EAX is outside the SS segment limit.

#PF(fault-code)  For a page fault.

#UD  If CPUID.01H:ECX.MONITOR[bit 3] = 0.
     If current privilege level is not 0.

**Real Address Mode Exceptions**

#GP  If the CS, DS, ES, FS, or GS register is used to access memory and the value in EAX is outside of the effective address space from 0 to FFFFH.
     If ECX ≠ 0.

#SS  If the SS register is used to access memory and the value in EAX is outside of the effective address space from 0 to FFFFH.

#UD  If CPUID.01H:ECX.MONITOR[bit 3] = 0.
Virtual 8086 Mode Exceptions

#UD The MONITOR instruction is not recognized in virtual-8086 mode (even if CPUID.01H:ECX.MONITOR[bit 3] = 1).

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the linear address of the operand in the CS, DS, ES, FS, or GS segment is in a non-canonical form.
   If RCX ≠ 0.
#SS(0) If the SS register is used to access memory and the value in EAX is in a non-canonical form.
#PF(fault-code) For a page fault.
#UD If the current privilege level is not 0.
   If CPUID.01H:ECX.MONITOR[bit 3] = 0.
### MOV—Move

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<th>Description</th>
</tr>
</thead>
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<tr>
<td>88 /r</td>
<td>MOV r/m8,r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r8 to r/m8.</td>
</tr>
<tr>
<td>REX + 88 /r</td>
<td>MOV r/m8***,r8***</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r8 to r/m8.</td>
</tr>
<tr>
<td>89 /r</td>
<td>MOV r/m16,r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r16 to r/m16.</td>
</tr>
<tr>
<td>REX.W + 89 /r</td>
<td>MOV r/m64,r/m32</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r64 to r/m64.</td>
</tr>
<tr>
<td>8A /r</td>
<td>MOV r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r/m8 to r8.</td>
</tr>
<tr>
<td>REX + 8A /r</td>
<td>MOV r/m8***,r/m8***</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r/m8 to r8.</td>
</tr>
<tr>
<td>8B /r</td>
<td>MOV r/m16,r16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r/m16 to r16.</td>
</tr>
<tr>
<td>8B /r</td>
<td>MOV r/m32,r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r/m32 to r32.</td>
</tr>
<tr>
<td>REX.W + 8B /r</td>
<td>MOV r/m64,r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r/m64 to r64.</td>
</tr>
<tr>
<td>8C /r</td>
<td>MOV r/m16,Sreg**</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Move segment register to r/m16.</td>
</tr>
<tr>
<td>REX.W + 8C /r</td>
<td>MOV r/m64,Sreg**</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Move zero extended 16-bit segment register to r/m64.</td>
</tr>
<tr>
<td>8E /r</td>
<td>MOV Sreg,r/m16**</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move r/m16 to segment register.</td>
</tr>
<tr>
<td>REX.W + 8E /r</td>
<td>MOV Sreg,r/m64**</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move lower 16 bits of r/m64 to segment register.</td>
</tr>
<tr>
<td>A0</td>
<td>MOV moffs8*</td>
<td>FD</td>
<td>Valid</td>
<td>Valid</td>
<td>Move byte at (seg:offset) to AL.</td>
</tr>
<tr>
<td>REX.W + A0</td>
<td>MOV moffs8*</td>
<td>FD</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move byte at (offset) to AL.</td>
</tr>
<tr>
<td>A1</td>
<td>MOV AX,moffs16*</td>
<td>FD</td>
<td>Valid</td>
<td>Valid</td>
<td>Move word at (seg:offset) to AX.</td>
</tr>
<tr>
<td>A1</td>
<td>MOV EAX,moffs32*</td>
<td>FD</td>
<td>Valid</td>
<td>Valid</td>
<td>Move doubleword at (seg:offset) to EAX.</td>
</tr>
<tr>
<td>REX.W + A1</td>
<td>MOV RAX,moffs32*</td>
<td>FD</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move quadword at (offset) to RAX.</td>
</tr>
<tr>
<td>A2</td>
<td>MOV moffs8,AL</td>
<td>TD</td>
<td>Valid</td>
<td>Valid</td>
<td>Move AL to (seg:offset).</td>
</tr>
<tr>
<td>REX.W + A2</td>
<td>MOV moffs8**,AL</td>
<td>TD</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move AL to (offset).</td>
</tr>
<tr>
<td>A3</td>
<td>MOV moffs16**,AX</td>
<td>TD</td>
<td>Valid</td>
<td>Valid</td>
<td>Move AX to (seg:offset).</td>
</tr>
<tr>
<td>A3</td>
<td>MOV moffs32**,EAX</td>
<td>TD</td>
<td>Valid</td>
<td>Valid</td>
<td>Move EAX to (seg:offset).</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>Op/En</td>
<td>64-Bit Mode</td>
<td>Compat/Leg Mode</td>
<td>Description</td>
</tr>
<tr>
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<td>---------------------------</td>
<td>-------</td>
<td>-------------</td>
<td>-----------------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>REX.W + A3</td>
<td>MOV moffs64*,RAX</td>
<td>TD</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move RAX to (offset).</td>
</tr>
<tr>
<td>B0+ rb</td>
<td>MOV r8, imm8</td>
<td>OI</td>
<td>Valid</td>
<td>Valid</td>
<td>Move imm8 to r8.</td>
</tr>
<tr>
<td>REX + B0+ rb</td>
<td>MOV r8**, imm8</td>
<td>OI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move imm8 to r8.</td>
</tr>
<tr>
<td>B8+ rw</td>
<td>MOV r16, imm16</td>
<td>OI</td>
<td>Valid</td>
<td>Valid</td>
<td>Move imm16 to r16.</td>
</tr>
<tr>
<td>B8+ rd</td>
<td>MOV r32, imm32</td>
<td>OI</td>
<td>Valid</td>
<td>Valid</td>
<td>Move imm32 to r32.</td>
</tr>
<tr>
<td>REX.W + B8+ rd</td>
<td>MOV r64, imm64</td>
<td>OI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move imm64 to r64.</td>
</tr>
<tr>
<td>C6 /0</td>
<td>MOV r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Move imm8 to r/m8.</td>
</tr>
<tr>
<td>REX + C6 /0</td>
<td>MOV r/m8**, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move imm8 to r/m8.</td>
</tr>
<tr>
<td>C7 /0</td>
<td>MOV r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Move imm16 to r/m16.</td>
</tr>
<tr>
<td>C7 /0</td>
<td>MOV r/m32, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Move imm32 to r/m32.</td>
</tr>
<tr>
<td>REX.W + C7 /0</td>
<td>MOV r/m64, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move imm32 sign extended to 64-bits to r/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* The moffs8, moffs16, moffs32 and moffs64 operands specify a simple offset relative to the segment base, where 8, 16, 32 and 64 refer to the size of the data. The address-size attribute of the instruction determines the size of the offset, either 16, 32 or 64 bits.

**In 32-bit mode, the assembler may insert the 16-bit operand-size prefix with this instruction (see the following “Description” section for further information).**

***In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.**
Description
Copies the second operand (source operand) to the first operand (destination operand). The source operand can be an immediate value, general-purpose register, segment register, or memory location; the destination register can be a general-purpose register, segment register, or memory location. Both operands must be the same size, which can be a byte, a word, a doubleword, or a quadword.

The MOV instruction cannot be used to load the CS register. Attempting to do so results in an invalid opcode exception (#UD). To load the CS register, use the far JMP, CALL, or RET instruction.

If the destination operand is a segment register (DS, ES, FS, GS, or SS), the source operand must be a valid segment selector. In protected mode, moving a segment selector into a segment register automatically causes the segment descriptor information associated with that segment selector to be loaded into the hidden (shadow) part of the segment register. While loading this information, the segment selector and segment descriptor information is validated (see the "Operation" algorithm below). The segment descriptor data is obtained from the GDT or LDT entry for the specified segment selector.

A NULL segment selector (values 0000-0003) can be loaded into the DS, ES, FS, and GS registers without causing a protection exception. However, any subsequent attempt to reference a segment whose corresponding segment register is loaded with a NULL value causes a general protection exception (#GP) and no memory reference occurs.

Loading the SS register with a MOV instruction inhibits all interrupts until after the execution of the next instruction. This operation allows a stack pointer to be loaded into the ESP register with the next instruction (MOV ESP, stack-pointer value) before an interrupt occurs. Be aware that the LSS instruction offers a more efficient method of loading the SS and ESP registers.

When operating in 32-bit mode and moving data between a segment register and a general-purpose register, the 32-bit IA-32 processors do not require the use of the 16-bit operand-size prefix (a byte with the value 66H) with this instruction, but most assemblers will insert it if the standard form of the instruction is used (for example, MOV DS, AX). The processor will execute this instruction correctly, but it will usually
require an extra clock. With most assemblers, using the instruction form MOV DS, EAX will avoid this unneeded 66H prefix. When the processor executes the instruction with a 32-bit general-purpose register, it assumes that the 16 least-significant bits of the general-purpose register are the destination or source operand. If the register is a destination operand, the resulting value in the two high-order bytes of the register is implementation dependent. For the Pentium 4, Intel Xeon, and P6 family processors, the two high-order bytes are filled with zeros; for earlier 32-bit IA-32 processors, the two high order bytes are undefined.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

```
DEST ← SRC;
```

Loading a segment register while in protected mode results in special checks and actions, as described in the following listing. These checks are performed on the segment selector and the segment descriptor to which it points.

IF SS is loaded

THEN

IF segment selector is NULL

THEN #GP(0); FI;

IF segment selector index is outside descriptor table limits

or segment selector’s RPL ≠ CPL

or segment is not a writable data segment

or DPL ≠ CPL

THEN #GP(selector); FI;

IF segment not marked present

THEN #SS(selector);

ELSE

SS ← segment selector;

SS ← segment descriptor; FI;

1. If a code instruction breakpoint (for debug) is placed on an instruction located immediately after a MOV SS instruction, the breakpoint may not be triggered. However, in a sequence of instructions that load the SS register, only the first instruction in the sequence is guaranteed to delay an interrupt.

In the following sequence, interrupts may be recognized before MOV ESP, EBP executes:

```
MOV SS, EDX
MOV SS, EAX
MOV ESP, EBP
```
FROM MOV—Move

INSTRUCTION SET REFERENCE, M-Z

FI;

IF DS, ES, FS, or GS is loaded with non-NULL selector
THEN
  IF segment selector index is outside descriptor table limits
  or segment is not a data or readable code segment
  or ((segment is a data or nonconforming code segment)
  and (both RPL and CPL > DPL))
  THEN #GP(selector); FI;
  IF segment not marked present
  THEN #NP(selector);
  ELSE
    SegmentRegister ← segment selector;
    SegmentRegister ← segment descriptor; FI;
  FI;

IF DS, ES, FS, or GS is loaded with NULL selector
THEN
  SegmentRegister ← segment selector;
  SegmentRegister ← segment descriptor;
FI;

Flags Affected
None.

Protected Mode Exceptions

#GP(0)  If attempt is made to load SS register with NULL segment selector.
        If the destination operand is in a non-writable segment.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register contains a NULL segment selector.

#GP(selector)  If segment selector index is outside descriptor table limits.
    If the SS register is being loaded and the segment selector's RPL and the segment descriptor's DPL are not equal to the CPL.
    If the SS register is being loaded and the segment pointed to is a non-writable data segment.
    If the DS, ES, FS, or GS register is being loaded and the segment pointed to is not a data or readable code segment.
    If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.
#SS(0)  
If a memory operand effective address is outside the SS segment limit.

#SS(selector)  
If the SS register is being loaded and the segment pointed to is marked not present.

#NP  
If the DS, ES, FS, or GS register is being loaded and the segment pointed to is marked not present.

#PF(fault-code)  
If a page fault occurs.

#AC(0)  
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  
If attempt is made to load the CS register.

If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP  
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  
If a memory operand effective address is outside the SS segment limit.

#UD  
If attempt is made to load the CS register.

If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0)  
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  
If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  
If a page fault occurs.

#AC(0)  
If alignment checking is enabled and an unaligned memory reference is made.

#UD  
If attempt is made to load the CS register.

If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#GP(0)  
If the memory address is in a non-canonical form.

If an attempt is made to load SS register with NULL segment selector when CPL = 3.

If an attempt is made to load SS register with NULL segment selector when CPL < 3 and CPL ≠ RPL.
INSTRUCTION SET REFERENCE, M-Z

#GP(selector)  If segment selector index is outside descriptor table limits.
   If the memory access to the descriptor table is non-canonical.
   If the SS register is being loaded and the segment selector's RPL
   and the segment descriptor's DPL are not equal to the CPL.
   If the SS register is being loaded and the segment pointed to is
   a nonwritable data segment.
   If the DS, ES, FS, or GS register is being loaded and the
   segment pointed to is not a data or readable code segment.
   If the DS, ES, FS, or GS register is being loaded and the
   segment pointed to is a data or nonconforming code segment,
   but both the RPL and the CPL are greater than the DPL.

#SS(0)  If the stack address is in a non-canonical form.
#SS(selector)  If the SS register is being loaded and the segment pointed to is
   marked not present.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
   reference is made while the current privilege level is 3.
#UD  If attempt is made to load the CS register.
   If the LOCK prefix is used.
MOV—Move to/from Control Registers

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<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 20/r MOV r32, CR0-CR7</td>
<td>MR</td>
<td>N.E.</td>
<td>Valid</td>
<td>Move control register to r32.</td>
</tr>
<tr>
<td>OF 20/r MOV r64, CR0-CR7</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move extended control register to r64.</td>
</tr>
<tr>
<td>REX.R + OF 20 /0 MOV r64, CR8</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move extended CR8 to r64.</td>
</tr>
<tr>
<td>OF 22 /r MOV CR0-CR7, r32</td>
<td>RM</td>
<td>N.E.</td>
<td>Valid</td>
<td>Move r32 to control register.</td>
</tr>
<tr>
<td>OF 22 /r MOV CR0-CR7, r64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r64 to extended control register.</td>
</tr>
<tr>
<td>REX.R + OF 22 /0 MOV CR8, r64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r64 to extended CR8.</td>
</tr>
</tbody>
</table>

NOTE:
1. MOV CR* instructions, except for MOV CR8, are serializing instructions. MOV CR8 is not architecturally defined as a serializing instruction. For more information, see Chapter 8 in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRMreg (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Moves the contents of a control register (CR0, CR2, CR3, CR4, or CR8) to a general-purpose register or the contents of a general purpose register to a control register. The operand size for these instructions is always 32 bits in non-64-bit modes, regardless of the operand-size attribute. (See “Control Registers” in Chapter 2 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A, for a detailed description of the flags and fields in the control registers.) This instruction can be executed only when the current privilege level is 0.

At the opcode level, the reg field within the ModR/M byte specifies which of the control registers is loaded or read. The 2 bits in the mod field are ignored. The r/m field specifies the general-purpose register loaded or read. Attempts to reference CR1, CR5, CR6, CR7, and CR9–CR15 result in undefined opcode (#UD) exceptions.
When loading control registers, programs should not attempt to change the reserved bits; that is, always set reserved bits to the value previously read. An attempt to change CR4’s reserved bits will cause a general protection fault. Reserved bits in CR0 and CR3 remain clear after any load of those registers; attempts to set them have no impact. On Pentium 4, Intel Xeon and P6 family processors, CR0.ET remains set after any load of CR0; attempts to clear this bit have no impact.

In certain cases, these instructions have the side effect of invalidating entries in the TLBs and the paging-structure caches. See Section 4.10.4.1, “Operations that Invalidate TLBs and Paging-Structure Caches,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A for details.

The following side effects are implementation-specific for the Pentium 4, Intel Xeon, and P6 processor family: when modifying PE or PG in register CR0, or PSE or PAE in register CR4, all TLB entries are flushed, including global entries. Software should not depend on this functionality in all Intel 64 or IA-32 processors.

In 64-bit mode, the instruction’s default operation size is 64 bits. The REX.R prefix must be used to access CR8. Use of REX.B permits access to additional registers (R8-R15). Use of the REX.W prefix or 66H prefix is ignored. Use of the REX.R prefix to specify a register other than CR8 causes an invalid-opcode exception. See the summary chart at the beginning of this section for encoding data and limits.

If CR4.PCIDE = 1, bit 63 of the source operand to MOV to CR3 determines whether the instruction invalidates entries in the TLBs and the paging-structure caches (see Section 4.10.4.1, “Operations that Invalidate TLBs and Paging-Structure Caches,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A). The instruction does not modify bit 63 of CR3, which is reserved and always 0.

See “Changes to Instruction Behavior in VMX Non-Root Operation” in Chapter 25 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, for more information about the behavior of this instruction in VMX non-root operation.

**Operation**

DEST ← SRC;

**Flags Affected**

The OF, SF, ZF, AF, PF, and CF flags are undefined.

**Protected Mode Exceptions**

#GP(0) If the current privilege level is not 0.
If an attempt is made to write invalid bit combinations in CR0 (such as setting the PG flag to 1 when the PE flag is set to 0, or setting the CD flag to 0 when the NW flag is set to 1).
If an attempt is made to write a 1 to any reserved bit in CR4.
If an attempt is made to write 1 to CR4.PCIDE.
If any of the reserved bits are set in the page-directory pointers table (PDPT) and the loading of a control register causes the PDPT to be loaded into the processor.

#UD If the LOCK prefix is used.
If an attempt is made to access CR1, CR5, CR6, or CR7.

**Real-Address Mode Exceptions**

#GP If an attempt is made to write a 1 to any reserved bit in CR4.
If an attempt is made to write 1 to CR4.PCIDE.
If an attempt is made to write invalid bit combinations in CR0 (such as setting the PG flag to 1 when the PE flag is set to 0).

#UD If the LOCK prefix is used.
If an attempt is made to access CR1, CR5, CR6, or CR7.

**Virtual-8086 Mode Exceptions**

#GP(0) These instructions cannot be executed in virtual-8086 mode.

**Compatibility Mode Exceptions**

#GP(0) If an attempt is made to write invalid bit combinations in CR0 (such as setting the PG flag to 1 when the PE flag is set to 0, or setting the CD flag to 0 when the NW flag is set to 1).
If an attempt is made to change CR4.PCIDE from 0 to 1 while CR3[11:0] ≠ 000H.
If an attempt is made to clear CR0.PG[bit 31] while CR4.PCIDE = 1.
If an attempt is made to write a 1 to any reserved bit in CR3.
If an attempt is made to leave IA-32e mode by clearing CR4.PAE[bit 5].

#UD If the LOCK prefix is used.
If an attempt is made to access CR1, CR5, CR6, or CR7.

**64-Bit Mode Exceptions**

#GP(0) If an attempt is made to write invalid bit combinations in CR0 (such as setting the PG flag to 1 when the PE flag is set to 0, or setting the CD flag to 0 when the NW flag is set to 1).
If an attempt is made to change CR4.PCIDE from 0 to 1 while CR3[11:0] ≠ 000H.
If an attempt is made to clear CR0.PG[bit 31].
If an attempt is made to write a 1 to any reserved bit in CR4.
If an attempt is made to write a 1 to any reserved bit in CR8.
If an attempt is made to write a 1 to any reserved bit in CR3.
If an attempt is made to leave IA-32e mode by clearing CR4.PAE[bit 5].

#UD
If the LOCK prefix is used.
If an attempt is made to access CR1, CR5, CR6, or CR7.
If the REX.R prefix is used to specify a register other than CR8.
MOV—Move to/from Debug Registers

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 21/r MOV r32, DR0–DR7</td>
<td>MR</td>
<td>N.E.</td>
<td>Valid</td>
<td>Move debug register to r32.</td>
</tr>
<tr>
<td>0F 21/r MOV r64, DR0–DR7</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move extended debug register to r64.</td>
</tr>
<tr>
<td>0F 23/r MOV DR0-DR7, r32</td>
<td>RM</td>
<td>N.E.</td>
<td>Valid</td>
<td>Move r32 to debug register.</td>
</tr>
<tr>
<td>0F 23/r MOV DR0-DR7, r64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move r64 to extended debug register.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM/r/m (w)</td>
<td>ModRM/reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RM</td>
<td>ModRM/reg (w)</td>
<td>ModRM/r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Moves the contents of a debug register (DR0, DR1, DR2, DR3, DR4, DR5, DR6, or DR7) to a general-purpose register or vice versa. The operand size for these instructions is always 32 bits in non-64-bit modes, regardless of the operand-size attribute. (See Section 17.2, “Debug Registers”, of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A,* for a detailed description of the flags and fields in the debug registers.)

The instructions must be executed at privilege level 0 or in real-address mode.

When the debug extension (DE) flag in register CR4 is clear, these instructions operate on debug registers in a manner that is compatible with Intel386 and Intel486 processors. In this mode, references to DR4 and DR5 refer to DR6 and DR7, respectively. When the DE flag in CR4 is set, attempts to reference DR4 and DR5 result in an undefined opcode (#UD) exception. (The CR4 register was added to the IA-32 Architecture beginning with the Pentium processor.)

At the opcode level, the *reg* field within the ModR/M byte specifies which of the debug registers is loaded or read. The two bits in the *mod* field are ignored. The *r/m* field specifies the general-purpose register loaded or read.

In 64-bit mode, the instruction’s default operation size is 64 bits. Use of the REX.B prefix permits access to additional registers (R8–R15). Use of the REX.W or 66H prefix is ignored. Use of the REX.R prefix causes an invalid-opcode exception. See the summary chart at the beginning of this section for encoding data and limits.
INSTRUCTION SET REFERENCE, M-Z

Operation

IF ((DE = 1) and (SRC or DEST = DR4 or DR5))
THEN
    #UD;
ELSE
    DEST ← SRC;
FI;

Flags Affected

The OF, SF, ZF, AF, PF, and CF flags are undefined.

Protected Mode Exceptions

#GP(0)  If the current privilege level is not 0.
#UD     If CR4.DE[bit 3] = 1 (debug extensions) and a MOV instruction is executed involving DR4 or DR5.
         If the LOCK prefix is used.
#DB     If any debug register is accessed while the DR7.GD[bit 13] = 1.

Real-Address Mode Exceptions

#UD     If CR4.DE[bit 3] = 1 (debug extensions) and a MOV instruction is executed involving DR4 or DR5.
         If the LOCK prefix is used.
#DB     If any debug register is accessed while the DR7.GD[bit 13] = 1.

Virtual-8086 Mode Exceptions

#GP(0)  The debug registers cannot be loaded or read when in virtual-8086 mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0)  If the current privilege level is not 0.
         If an attempt is made to write a 1 to any of bits 63:32 in DR6.
         If an attempt is made to write a 1 to any of bits 63:32 in DR7.
#UD     If CR4.DE[bit 3] = 1 (debug extensions) and a MOV instruction is executed involving DR4 or DR5.
         If the LOCK prefix is used.
         If the REX.R prefix is used.
MOV—Move to/from Debug Registers

#DB If any debug register is accessed while the DR7.GD[bit 13] = 1.
## MOVAPD—Move Aligned Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 28 /r MOVAPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>66 0F 29 /r MOVAPD xmm2/m128, xmm1</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move packed double-precision floating-point values from xmm1 to xmm2/m128.</td>
</tr>
<tr>
<td>VEX.128.66.0F.WIG 28 /r VMOVAPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move aligned packed double-precision floating-point values from xmm2/mem to xmm1.</td>
</tr>
<tr>
<td>VEX.128.66.0F.WIG 29 /r VMOVAPD xmm2/m128, xmm1</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move aligned packed double-precision floating-point values from xmm1 to xmm2/mem.</td>
</tr>
<tr>
<td>VEX.256.66.0F.WIG 28 /r VMOVAPD ymm1, ymm2/m256</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move aligned packed double-precision floating-point values from ymm2/mem to ymm1.</td>
</tr>
<tr>
<td>VEX.256.66.0F.WIG 29 /r VMOVAPD ymm2/m256, ymm1</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move aligned packed double-precision floating-point values from ymm1 to ymm2/mem.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Moves 2 or 4 double-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM or YMM register from an 128-bit or 256-bit memory location, to store the contents of an XMM or YMM register into a 128-bit or 256-bit memory location, or to move data between two XMM or two YMM registers. When the source or destina-
operation operand is a memory operand, the operand must be aligned on a 16-byte (128-bit version) or 32-byte (VEX.256 encoded version) boundary or a general-protection exception (#GP) will be generated.

To move double-precision floating-point values to and from unaligned memory locations, use the (V)MOVUPD instruction.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

128-bit versions:
Moves 128 bits of packed double-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, to store the contents of an XMM register into a 128-bit memory location, or to move data between two XMM registers. When the source or destination operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated. To move single-precision floating-point values to and from unaligned memory locations, use the VMOVUPD instruction.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register destination are zeroed.

VEX.256 encoded version:
Moves 256 bits of packed double-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load a YMM register from a 256-bit memory location, to store the contents of a YMM register into a 256-bit memory location, or to move data between two YMM registers. When the source or destination operand is a memory operand, the operand must be aligned on a 32-byte boundary or a general-protection exception (#GP) will be generated. To move single-precision floating-point values to and from unaligned memory locations, use the VMOVUPD instruction.

Operation

MOVAPD (128-bit load- and register-copy- form Legacy SSE version)
DEST[127:0] ← SRC[127:0]
DEST[VLMAX-1:128] (Unmodified)

(V)MOVAPD (128-bit store-form version)
DEST[127:0] ← SRC[127:0]

VMOVAPD (VEX.128 encoded version)
DEST[127:0] ← SRC[127:0]
DEST[VLMAX-1:128] ← 0

**VMOVAPD (VEX.256 encoded version)**

DEST[255:0] ← SRC[255:0]

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVAPD:  __m128d _mm_load_pd (double const * p);
MOVAPD:  _mm_store_pd(double * p, __m128d a);
VMOVAPD:  __m256d _mm256_load_pd (double const * p);
VMOVAPD:  _mm256_store_pd(double * p, __m256d a);

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 1.SSE2; additionally

#UD  If VEX.vvvv != 1111B.
MOVAPS—Move Aligned Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 28 /r MOVAPS xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Move packed single-precision floating-point values from xmm2/m128 to xmm1.</td>
<td></td>
</tr>
<tr>
<td>0F 29 /r MOVAPS xmm2/m128, xmm1</td>
<td>MR V/V</td>
<td>SSE</td>
<td>Move packed single-precision floating-point values from xmm1 to xmm2/m128.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F:WIG 28 /r VMOVAPS xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Move aligned packed single-precision floating-point values from xmm2/mem to xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F:WIG 29 /r VMOVAPS xmm2/m128, xmm1</td>
<td>MR V/V</td>
<td>AVX</td>
<td>Move aligned packed single-precision floating-point values from xmm1 to xmm2/mem.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.0F:WIG 28 /r VMOVAPS ymm1, ymm2/m256</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Move aligned packed single-precision floating-point values from ymm2/mem to ymm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.0F:WIG 29 /r VMOVAPS ymm2/m256, ymm1</td>
<td>MR V/V</td>
<td>AVX</td>
<td>Move aligned packed single-precision floating-point values from ymm1 to ymm2/mem.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
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<th>Operand 2</th>
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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMrw/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRMrw/m (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Moves 4 or 8 single-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM or YMM register from an 128-bit or 256-bit memory location, to store the contents of an XMM or YMM register into a 128-bit or 256-bit memory location, or to move data between two XMM or two YMM registers. When the source or destination operand is a memory operand, the operand must be aligned on a 16-byte (128-bit) boundary.
bit version) or 32-byte (VEX.256 encoded version) boundary or a general-protection exception (#GP) will be generated.

To move single-precision floating-point values to and from unaligned memory locations, use the (V)MOVUPS instruction.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

128-bit versions:
Moves 128 bits of packed single-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, to store the contents of an XMM register into a 128-bit memory location, or to move data between two XMM registers. When the source or destination operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated. To move single-precision floating-point values to and from unaligned memory locations, use the VMOVUPS instruction.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

VEX.256 encoded version:
Moves 256 bits of packed single-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load a YMM register from a 256-bit memory location, to store the contents of a YMM register into a 256-bit memory location, or to move data between two YMM registers.

Operation

MOVAPS (128-bit load- and register-copy- form Legacy SSE version)
DEST[127:0] ← SRC[127:0]
DEST[VLMAX-1:128] (Unmodified)

(V)MOVAPS (128-bit store form)
DEST[127:0] ← SRC[127:0]

VMOVAPS (VEX.128 encoded version)
DEST[127:0] ← SRC[127:0]
DEST[VLMAX-1:128] ← 0

VMOVAPS (VEX.256 encoded version)
DEST[255:0] ← SRC[255:0]

Intel C/C++ Compiler Intrinsic Equivalent

MOVAPS: __m128 _mm_load_ps (float const * p);
MOVAPS: _mm_store_ps(float * p, __m128 a);
VMOVAPS: __m256 _mm256_load_ps (float const * p);
VMOVAPS: _mm256_store_ps(float * p, __m256 a);

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 1.SSE; additionally
#UD If VEX.vvvv != 1111B.
MOVBE—Move Data After Swapping Bytes

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 F0 /r</td>
<td>MOVBE r16, m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse byte order in m16 and move to r16</td>
</tr>
<tr>
<td>0F 38 F0 /r</td>
<td>MOVBE r32, m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse byte order in m32 and move to r32</td>
</tr>
<tr>
<td>REX.W + 0F 38 F0 /r</td>
<td>MOVBE r64, m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Reverse byte order in m64 and move to r64</td>
</tr>
<tr>
<td>0F 38 F1 /r</td>
<td>MOVBE m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse byte order in r16 and move to m16</td>
</tr>
<tr>
<td>0F 38 F1 /r</td>
<td>MOVBE m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse byte order in r32 and move to m32</td>
</tr>
<tr>
<td>REX.W + 0F 38 F1 /r</td>
<td>MOVBE m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Reverse byte order in r64 and move to m64</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
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<tr>
<th>Op/En</th>
<th>Operand 1</th>
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<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a byte swap operation on the data copied from the second operand (source operand) and store the result in the first operand (destination operand). The source operand can be a general-purpose register, or memory location; the destination register can be a general-purpose register, or a memory location; however, both operands can not be registers, and only one operand can be a memory location. Both operands must be the same size, which can be a word, a doubleword or quadword.

The MOVBE instruction is provided for swapping the bytes on a read from memory or on a write to memory; thus providing support for converting little-endian values to big-endian format and vice versa.

In 64-bit mode, the instruction's default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

TEMP ← SRC
IF (OperandSize = 16)
   THEN
      DEST[7:0] ← TEMP[15:8];
      DEST[15:8] ← TEMP[7:0];
   ELSIF (OperandSize = 32)
      DEST[7:0] ← TEMP[31:24];
      DEST[15:8] ← TEMP[23:16];
      DEST[23:16] ← TEMP[15:8];
      DEST[31:23] ← TEMP[7:0];
   ELSEIF (OperandSize = 64)
      DEST[7:0] ← TEMP[63:56];
      DEST[15:8] ← TEMP[55:48];
      DEST[23:16] ← TEMP[47:40];
      DEST[39:32] ← TEMP[31:24];
      DEST[47:40] ← TEMP[23:16];
      DEST[55:48] ← TEMP[15:8];
      DEST[63:56] ← TEMP[7:0];
   FI;
Flags Affected

None.

Protected Mode Exceptions

#GP(0)  If the destination operand is in a non-writable segment.
   If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If CPUID.01H:ECX.MOVBE[bit 22] = 0.
   If the LOCK prefix is used.
   If REP (F3H) prefix is used.

Real-Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
MOVBE—Move Data After Swapping Bytes

INSTRUCTION SET REFERENCE, M-Z

#SS If a memory operand effective address is outside the SS segment limit.

#UD If CPUID.01H:ECX.MOVBE[bit 22] = 0.
If the LOCK prefix is used.
If REP (F3H) prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD If CPUID.01H:ECX.MOVBE[bit 22] = 0.
If the LOCK prefix is used.
If REP (F3H) prefix is used.
If REPNE (F2H) prefix is used and CPUID.01H:ECX.SSE4_2[bit 20] = 0.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
#SS(0) If the stack address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If CPUID.01H:ECX.MOVBE[bit 22] = 0.
If the LOCK prefix is used.
If REP (F3H) prefix is used.
MOVD/MOVQ—Move Doubleword/Move Quadword

<table>
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<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 6E /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Move doubleword from r/m32 to mm.</td>
</tr>
<tr>
<td>MOVQ mm, r/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REX.W + OF 6E /r</td>
<td>RM</td>
<td>V/N.E.</td>
<td>MMX</td>
<td>Move quadword from r/m64 to mm.</td>
</tr>
<tr>
<td>MOVQ mm, r/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF 7E /r</td>
<td>MR</td>
<td>V/V</td>
<td>MMX</td>
<td>Move doubleword from mm to r/m32.</td>
</tr>
<tr>
<td>MOVQ r/m32, mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REX.W + OF 7E /r</td>
<td>MR</td>
<td>V/N.E.</td>
<td>MMX</td>
<td>Move quadword from mm to r/m64.</td>
</tr>
<tr>
<td>MOVQ r/m64, mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:W0 6E /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move doubleword from r/m32 to xmm1.</td>
</tr>
<tr>
<td>VMOVD xmm1, r32/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:W1 6E /r</td>
<td>RM</td>
<td>V/N.E.</td>
<td>AVX</td>
<td>Move quadword from r/m64 to xmm1.</td>
</tr>
<tr>
<td>VMOVQ xmm1, r64/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF 6E /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move doubleword from r/m32 to xmm.</td>
</tr>
<tr>
<td>MOVQ xmm, r/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 REX.W 0F 6E /r</td>
<td>RM</td>
<td>V/N.E.</td>
<td>SSE2</td>
<td>Move quadword from r/m64 to xmm.</td>
</tr>
<tr>
<td>MOVQ xmm, r/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF 7E /r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move doubleword from xmm register to r/m32.</td>
</tr>
<tr>
<td>MOVQ r/m32, xmm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 REX.W 0F 7E /r</td>
<td>MR</td>
<td>V/N.E.</td>
<td>SSE2</td>
<td>Move quadword from xmm register to r/m64.</td>
</tr>
<tr>
<td>MOVQ r/m64, xmm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:W0 7E /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move doubleword from xmm1 register to r/m32.</td>
</tr>
<tr>
<td>VMOVQ r32/m32, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:W1 7E /r</td>
<td>MR</td>
<td>V/N.E.</td>
<td>AVX</td>
<td>Move quadword from xmm1 register to r/m64.</td>
</tr>
<tr>
<td>VMOVQ r64/m64, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRMreg (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Copies a doubleword from the source operand (second operand) to the destination
INSTRUCTION SET REFERENCE, M-Z

operand (first operand). The source and destination operands can be general-purpose registers, MMX technology registers, XMM registers, or 32-bit memory locations. This instruction can be used to move a doubleword to and from the low doubleword of an MMX technology register and a general-purpose register or a 32-bit memory location, or to and from the low doubleword of an XMM register and a general-purpose register or a 32-bit memory location. The instruction cannot be used to transfer data between MMX technology registers, between XMM registers, between general-purpose registers, or between memory locations.

When the destination operand is an MMX technology register, the source operand is written to the low doubleword of the register, and the register is zero-extended to 64 bits. When the destination operand is an XMM register, the source operand is written to the low doubleword of the register, and the register is zero-extended to 128 bits.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

MOVD (when destination operand is MMX technology register)
\[
\text{DEST}[31:0] \leftarrow \text{SRC}; \\
\text{DEST}[63:32] \leftarrow 00000000H;
\]

MOVD (when destination operand is XMM register)
\[
\text{DEST}[31:0] \leftarrow \text{SRC}; \\
\text{DEST}[127:32] \leftarrow 000000000000000000000000H; \\
\text{DEST}[\text{VLMAX}-1:128] \text{ (Unmodified)}
\]

MOVD (when source operand is MMX technology or XMM register)
\[
\text{DEST} \leftarrow \text{SRC}[31:0];
\]

VMOVD (VEX-encoded version when destination is an XMM register)
\[
\text{DEST}[31:0] \leftarrow \text{SRC}[31:0] \\
\text{DEST}[\text{VLMAX}-1:32] \leftarrow 0
\]

MOVQ (when destination operand is XMM register)
\[
\text{DEST}[63:0] \leftarrow \text{SRC}[63:0]; \\
\text{DEST}[127:64] \leftarrow 000000000000000000000000H; \\
\text{DEST}[\text{VLMAX}-1:128] \text{ (Unmodified)}
\]

MOVQ (when destination operand is r/m64)
\[
\text{DEST}[63:0] \leftarrow \text{SRC}[63:0];
\]

MOVQ (when source operand is XMM register or r/m64)
\[
\text{DEST} \leftarrow \text{SRC}[63:0];
\]
VMOVQ (VEX-encoded version when destination is an XMM register)
DEST[63:0] ← SRC[63:0]
DEST[VLMAX-1:64] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
MOVD: 

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD If VEX.L = 1.
If VEX.vvvv != 1111B.
MOVDDUP—Move One Double-FP and Duplicate

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 12 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE3</td>
<td>Move one double-precision floating-point value from the lower 64-bit operand in xmm2/m64 to xmm1 and duplicate.</td>
</tr>
<tr>
<td>MOVDDUP xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.F2.0F.WIG 12 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move double-precision floating-point values from xmm2/mem and duplicate into xmm1.</td>
</tr>
<tr>
<td>VMOVDDUP xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.F2.0F.WIG 12 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move even index double-precision floating-point values from ymm2/mem and duplicate each element into ymm1.</td>
</tr>
<tr>
<td>VMOVDDUP ymm1, ymm2/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 8 bytes of data at memory location m64 are loaded. When the register-register form of this operation is used, the lower half of the 128-bit source register is duplicated and copied into the 128-bit destination register. See Figure 4-2.
**MOVDDUP—Move One Double-FP and Duplicate**

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

IF (Source = m64)
   THEN
      (* Load instruction *)
      xmm1[63:0] = m64;
      xmm1[127:64] = m64;
   ELSE
      (* Move instruction *)
      xmm1[63:0] = xmm2[63:0];
      xmm1[127:64] = xmm2[63:0];
FI;

**MOVDDUP (128-bit Legacy SSE version)**
DEST[63:0] ← SRC[63:0]
DEST[127:64] ← SRC[63:0]
DEST[VLMAX-1:128] (Unmodified)

**VMOVDDUP (VEX.128 encoded version)**
DEST[63:0] ← SRC[63:0]
DEST[127:64] ← SRC[63:0]
DEST[VLMAX-1:128] ← 0

**VMOVDDUP (VEX.256 encoded version)**

DEST[63:0] ← SRC[63:0]
DEST[127:64] ← SRC[63:0]

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVDDUP: __m128d _mm_movedup_pd(__m128d a)
MOVDDUP: __m128d _mm_loaddup_pd(double const * dp)

**SIMD Floating-Point Exceptions**

None

**Other Exceptions**

See Exceptions Type 5; additionally

#UD If VEX.vvvv != 1111B.
MOVDQA—Move Aligned Double Quadword

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<th>64/32-bit Mode</th>
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</tr>
</thead>
<tbody>
<tr>
<td>66 0F 6F /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move aligned double quadword from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>MOVDQA xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 7F /r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move aligned double quadword from xmm1 to xmm2/m128.</td>
</tr>
<tr>
<td>MOVDQA xmm2/m128, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:WIG 6F /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move aligned packed integer values from xmm2/mem to xmm1.</td>
</tr>
<tr>
<td>VMOVQDXA xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:WIG 7F /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move aligned packed integer values from xmm1 to xmm2/mem.</td>
</tr>
<tr>
<td>VMOVQDXA xmm2/m128, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F:WIG 6F /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move aligned packed integer values from ymm2/mem to ymm1.</td>
</tr>
<tr>
<td>VMOVQDXA ymm1, ymm2/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F:WIG 7F /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move aligned packed integer values from ymm1 to ymm2/mem.</td>
</tr>
<tr>
<td>VMOVQDXA ymm2/m256, ymm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

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</tr>
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<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
128-bit versions:
Moves 128 bits of packed integer values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, to store the contents of an XMM register into a 128-bit memory location, or to move data between two XMM registers.

When the source or destination operand is a memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated. To move integer data to and from unaligned memory locations, use the VMOVQDXA instruction.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
INSTRUCTION SET REFERENCE, M-Z

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

VEX.256 encoded version:
Moves 256 bits of packed integer values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load a YMM register from a 256-bit memory location, to store the contents of a YMM register into a 256-bit memory location, or to move data between two YMM registers.

When the source or destination operand is a memory operand, the operand must be aligned on a 32-byte boundary or a general-protection exception (#GP) will be generated. To move integer data to and from unaligned memory locations, use the VMOVDQU instruction.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

Operation

MOVDQA (128-bit load- and register-form Legacy SSE version)
DEST[127:0] ← SRC[127:0]
DEST[VLMAX-1:128] (Unmodified)
(* #GP if SRC or DEST unaligned memory operand *)

(V)MOVDQA (128-bit store forms)
DEST[127:0] ← SRC[127:0]

VMOVDA (VEX.128 encoded version)
DEST[127:0] ← SRC[127:0]
DEST[VLMAX-1:128] ← 0

VMOVDA (VEX.256 encoded version)
DEST[255:0] ← SRC[255:0]

Intel C/C++ Compiler Intrinsic Equivalent

MOVDQA: __m128i _mm_load_si128(__m128i *p)
MOVDQA: void _mm_store_si128(__m128i *p, __m128i a)
VMOVDA: __m256i _mm256_load_si256(__m256i *p);
VMOVDA: _mm256_store_si256(__m256i *p, __m256i a);
SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 1.SSE2; additionally
#UD If VEX.vvvv != 1111B.
MOVDQU—Move Unaligned Double Quadword

<table>
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<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
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<tbody>
<tr>
<td>F3 0F 6F /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move unaligned double quadword from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>MOVDQU xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F3 0F 7F /r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move unaligned double quadword from xmm1 to xmm2/m128.</td>
</tr>
<tr>
<td>MOVDQU xmm2/m128, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VMOVQDU xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.F3.0F:WIG 7F /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move unaligned packed integer values from xmm1 to xmm2/mem.</td>
</tr>
<tr>
<td>VMOVQDU xmm2/m128, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VMOVQDU ymm1, ymm2/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.F3.0F:WIG 7F /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move unaligned packed integer values from ymm1 to ymm2/mem.</td>
</tr>
<tr>
<td>VMOVQDU ymm2/m256, ymm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

128-bit versions:
Moves 128 bits of packed integer values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, to store the contents of an XMM register into a 128-bit memory location, or to move data between two XMM registers. When the source or destination operand is a memory operand, the operand may be unaligned on a 16-byte boundary without causing a general-protection exception (#GP) to be generated.1

To move a double quadword to or from memory locations that are known to be aligned on 16-byte boundaries, use the MOVDQA instruction.
While executing in 16-bit addressing mode, a linear address for a 128-bit data access that overlaps the end of a 16-bit segment is not allowed and is defined as reserved behavior. A specific processor implementation may or may not generate a general-protection exception (#GP) in this situation, and the address that spans the end of the segment may or may not wrap around to the beginning of the segment.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**128-bit Legacy SSE version:** Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

When the source or destination operand is a memory operand, the operand may be unaligned to any alignment without causing a general-protection exception (#GP) to be generated.

**VEX.128 encoded version:** Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**VEX.256 encoded version:**

Moves 256 bits of packed integer values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load a YMM register from a 256-bit memory location, to store the contents of a YMM register into a 256-bit memory location, or to move data between two YMM registers.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

**MOVDQU load and register copy (128-bit Legacy SSE version)**

DEST[127:0] ← SRC[127:0]

DEST[VLMAX-1:128] (Unmodified)

**(V)MOVDQU 128-bit store-form versions**

DEST[127:0] ← SRC[127:0]

**VM0VDQU (VEX.128 encoded version)**

DEST[127:0] ← SRC[127:0]

DEST[VLMAX-1:128] ← 0

**VM0VDQU (VEX.256 encoded version)**

DEST[255:0] ← SRC[255:0]

1. If alignment checking is enabled (CR0.AM = 1, RFLAGS.AC = 1, and CPL = 3), an alignment-check exception (#AC) may or may not be generated (depending on processor implementation) when the operand is not aligned on an 8-byte boundary.
**Intel C/C++ Compiler Intrinsic Equivalent**

MOVDQU: `void _mm_storeu_si128 ( __m128i *p, __m128i a)`

MOVDQU: `__m128i _mm_loadu_si128 ( __m128i *p)`

VMOVDQU: `__m256i _mm256_loadu_si256 ( __m256i *p);`

VMOVDQU: `__m256i _mm256_storeu_si256( __m256i *p, __m256i a);`

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD "If VEX.vvvv != 1111B."
**MOVDQ2Q—Move Quadword from XMM to MMX Technology Register**

**InstructionOperand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMcr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Moves the low quadword from the source operand (second operand) to the destination operand (first operand). The source operand is an XMM register and the destination operand is an MMX technology register.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the MOVDQ2Q instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST ← SRC[63:0];

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVDQ2Q: __m64 _mm_movepi64_pi64 ( __m128i a)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

#NM If CR0.TS[bit 3] = 1.
#UD If CR0.EM[bit 2] = 1.
If CR4.OSFXSR[bit 9] = 0.
If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#MF If there is a pending x87 FPU exception.
Instructions Set Reference, M-Z

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
MOVHLPS—Move Packed Single-Precision Floating-Point Values High to Low

### Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 12 /r MOVHLPS xmm1, xmm2</td>
<td>RM V/V</td>
<td>SSE3</td>
<td>Move two packed single-precision floating-point values from high quadword of xmm2 to low quadword of xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 12 /r VMOVHLPS xmm1, xmm2, xmm3</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Merge two packed single-precision floating-point values from high quadword of xmm3 and low quadword of xmm2.</td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

This instruction cannot be used for memory to register moves.

**128-bit two-argument form:**

Moves two packed single-precision floating-point values from the high quadword of the second XMM argument (second operand) to the low quadword of the first XMM register (first argument). The high quadword of the destination operand is left unchanged. Bits (VLMAX-1:64) of the corresponding YMM destination register are unmodified.

**128-bit three-argument form**

Moves two packed single-precision floating-point values from the high quadword of the third XMM argument (third operand) to the low quadword of the destination (first operand). Copies the high quadword from the second XMM argument (second operand) to the high quadword of the destination (first operand). Bits (VLMAX-1:128) of the destination YMM register are zeroed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

If VMOVHLPS is encoded with VEX.L=1, an attempt to execute the instruction encoded with VEX.L=1 will cause an #UD exception.
INSTRUCTION SET REFERENCE, M-Z

Operation

MOVHLPS (128-bit two-argument form)
DEST[63:0] ← SRC[127:64]
DEST[VLMAX-1:64] (Unmodified)

VMOVHLPS (128-bit three-argument form)
DEST[63:0] ← SRC2[127:64]
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
MOVHLPS: __m128 _mm_movehl_ps(__m128 a, __m128 b)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 7; additionally
#UD If VEX.L= 1.
MOVHPD—Move High Packed Double-Precision Floating-Point Value

### Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 16 //r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move double-precision floating-point value from <code>m64</code> to high quadword of <code>xmm</code>.</td>
</tr>
<tr>
<td>MOVHPD <code>xmm</code>, <code>m64</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 17 //r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move double-precision floating-point value from high quadword of <code>xmm</code> to <code>m64</code>.</td>
</tr>
<tr>
<td>MOVHPD <code>m64</code>, <code>xmm</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F:WIG 16 //r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Merge double-precision floating-point value from <code>m64</code> and the low quadword of <code>xmm1</code>.</td>
</tr>
<tr>
<td>VMOVHPD <code>xmm2</code>, <code>xmm1</code>, <code>m64</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX128.66.0F:WIG 17//r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move double-precision floating-point values from high quadword of <code>xmm1</code> to <code>m64</code>.</td>
</tr>
<tr>
<td>VMOVHPD <code>m64</code>, <code>xmm1</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### InstructionOperand Encoding

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

This instruction cannot be used for register to register or memory to memory moves.

**128-bit Legacy SSE load:**

Moves a double-precision floating-point value from the source 64-bit memory operand and stores it in the high 64-bits of the destination XMM register. The lower 64-bits of the XMM register are preserved. The upper 128-bits of the corresponding YMM destination register are preserved.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**VEX.128 encoded load:**

Loads a double-precision floating-point value from the source 64-bit memory operand (third operand) and stores it in the upper 64-bits of the destination XMM register (first operand). The low 64-bits from second XMM register (second operand)
are stored in the lower 64-bits of the destination. The upper 128-bits of the destination YMM register are zeroed.

128-bit store:
Stores a double-precision floating-point value from the high 64-bits of the XMM register source (second operand) to the 64-bit memory location (first operand).

Note: VMOVHPD (store) (VEX.128.66.0F 17 /r) is legal and has the same behavior as the existing 66 0F 17 store. For VMOVHPD (store) (VEX.128.66.0F 17 /r) instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.
If VMOVHPD is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.

Operation

MOVHPD (128-bit Legacy SSE load)
DEST[63:0] (Unmodified)
DEST[127:64] ← SRC[63:0]
DEST[VLMAX-1:128] (Unmodified)

VMOVHPD (VEX.128 encoded load)
DEST[63:0] ← SRC1[63:0]
DEST[127:64] ← SRC2[63:0]
DEST[VLMAX-1:128] ← 0

VMOVHPD (store)
DEST[63:0] ← SRC[127:64]

Intel C/C++ Compiler Intrinsic Equivalent
MOVHPD: __m128d _mm_loadh_pd ( __m128d a, double *p)
MOVHPD: void _mm_storeh_pd (double *p, __m128d a)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD If VEX.L= 1.
MOVHPS—Move High Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 16 /r MOVHPS xmm, m64</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Move two packed single-precision floating-point values from m64 to high quadword of xmm.</td>
<td></td>
</tr>
<tr>
<td>OF 17 /r MOVHPS m64, xmm</td>
<td>MR V/V</td>
<td>SSE</td>
<td>Move two packed single-precision floating-point values from high quadword of xmm to m64.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 16 /r VMOVHPS xmm2, xmm1, m64</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Merge two packed single-precision floating-point values from m64 and the low quadword of xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F.WIG 17/r VMOVHPS m64, xmm1</td>
<td>MR V/V</td>
<td>AVX</td>
<td>Move two packed single-precision floating-point values from high quadword of xmm1 to m64.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
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</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX:vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

This instruction cannot be used for register to register or memory to memory moves.

**128-bit Legacy SSE load:**
Moves two packed single-precision floating-point values from the source 64-bit memory operand and stores them in the high 64-bits of the destination XMM register. The lower 64-bits of the XMM register are preserved. The upper 128-bits of the corresponding YMM destination register are preserved.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**VEX.128 encoded load:**
Loads two single-precision floating-point values from the source 64-bit memory operand (third operand) and stores it in the upper 64-bits of the destination XMM register (first operand). The low 64-bits from second XMM register (second operand)
are stored in the lower 64-bits of the destination. The upper 128-bits of the destination YMM register are zeroed.

**128-bit store:**
Stores two packed single-precision floating-point values from the high 64-bits of the XMM register source (second operand) to the 64-bit memory location (first operand).
Note: VMOVHPS (store) (VEX.NDS.128.0F 17 /r) is legal and has the same behavior as the existing 0F 17 store. For VMOVHPS (store) (VEX.NDS.128.0F 17 /r) instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.
If VMOVHPS is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.

**Operation**

**MOVHPS (128-bit Legacy SSE load)**
DEST[63:0] (Unmodified)
DEST[127:64] ← SRC[63:0]
DEST[VLMAX-1:128] (Unmodified)

**VMOVHPS (VEX.128 encoded load)**
DEST[63:0] ← SRC1[63:0]
DEST[127:64] ← SRC2[63:0]
DEST[VLMAX-1:128] ← 0

**VMOVHPS (store)**
DEST[63:0] ← SRC[127:64]

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVHPS: __m128d _mm_loadh_pi ( __m128d a, __m64 *p)
MOVHPS: void _mm_storeh_pi ( __m64 *p, __m128d a)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 5; additionally
#UD If VEX.L= 1.
MOVLOHP—Move Packed Single-Precision Floating-Point Values Low to High

<table>
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<tr>
<th>Opcode/Instruction</th>
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<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
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</thead>
<tbody>
<tr>
<td>0F 16 /r MOVLOHPS xmm1, xmm2</td>
<td>RM V/V SSE</td>
<td></td>
<td>Move two packed single-precision floating-point values from the low quadword of xmm2 to the high quadword of xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 16 /r VMOVLOHP xmm1, xmm2, xmm3</td>
<td>RVM V/V AVX</td>
<td></td>
<td>Merge two packed single-precision floating-point values from the low quadword of xmm3 and the low quadword of xmm2.</td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

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<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg/r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (v)</td>
<td>ModRMreg/r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

This instruction cannot be used for memory to register moves.

**128-bit two-argument form:**

Moves two packed single-precision floating-point values from the low quadword of the second XMM argument (second operand) to the high quadword of the first XMM register (first argument). The low quadword of the destination operand is left unchanged. The upper 128 bits of the corresponding YMM destination register are unmodified.

**128-bit three-argument form**

Moves two packed single-precision floating-point values from the low quadword of the third XMM argument (third operand) to the high quadword of the destination (first operand). Copies the low quadword from the second XMM argument (second operand) to the low quadword of the destination (first operand). The upper 128-bits of the destination YMM register are zeroed.

If VMOVLOHP is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).
INSTRUCTION SET REFERENCE, M-Z

Operation

MOVLHPS (128-bit two-argument form)
DEST[63:0] (Unmodified)
DEST[127:64] ← SRC[63:0]
DEST[VLMAX-1:128] (Unmodified)

VMOVLHPS (128-bit three-argument form)
DEST[63:0] ← SRC1[63:0]
DEST[127:64] ← SRC2[63:0]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
MOVHLPS: __m128 _mm_movelh_ps(__m128 a, __m128 b)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 7; additionally
#UD If VEX.L= 1.
MOVLPD—Move Low Packed Double-Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 12 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move double-precision floating-point value from m64 to low quadword of xmm register.</td>
</tr>
<tr>
<td>MOVLPD xmm, m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 13 /r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move double-precision floating-point value from low quadword of xmm register to m64.</td>
</tr>
<tr>
<td>MOVLPD m64, xmm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 12 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Merge double-precision floating-point value from m64 and the high quadword of xmm1.</td>
</tr>
<tr>
<td>VMOVLPD xmm2, xmm1, m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F.WIG 13/r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move double-precision floating-point values from low quadword of xmm1 to m64.</td>
</tr>
<tr>
<td>VMOVLPD m64, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction Operand Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Op/En</td>
</tr>
<tr>
<td>RM</td>
</tr>
<tr>
<td>MR</td>
</tr>
<tr>
<td>RVM</td>
</tr>
</tbody>
</table>

**Description**

This instruction cannot be used for register to register or memory to memory moves.

**128-bit Legacy SSE load:**

Moves a double-precision floating-point value from the source 64-bit memory operand and stores it in the low 64-bits of the destination XMM register. The upper 64-bits of the XMM register are preserved. The upper 128-bits of the corresponding YMM destination register are preserved.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**VEX.128 encoded load:**

 Loads a double-precision floating-point value from the source 64-bit memory operand (third operand), merges it with the upper 64-bits of the first source XMM register (second operand), and stores it in the low 128-bits of the destination XMM register.
register (first operand). The upper 128-bits of the destination YMM register are zeroed.

**128-bit store:**
Stores a double-precision floating-point value from the low 64-bits of the XMM register source (second operand) to the 64-bit memory location (first operand).

Note: VMOVLPD (store) (VEX.128.66.0F 13 /r) is legal and has the same behavior as the existing 66 0F 13 store. For VMOVLPD (store) (VEX.128.66.0F 13 /r) instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD. If VMOVLPD is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.

**Operation**

**MOVLPD (128-bit Legacy SSE load)**

\[
\text{DEST}[63:0] \leftarrow \text{SRC}[63:0] \\
\text{DEST}[\text{VLMAX}-1:64] \text{ (Unmodified)}
\]

**VMOVLPD (VEX.128 encoded load)**

\[
\text{DEST}[63:0] \leftarrow \text{SRC2}[63:0] \\
\text{DEST}[127:64] \leftarrow \text{SRC1}[127:64] \\
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0
\]

**VMOVLPD (store)**

\[
\text{DEST}[63:0] \leftarrow \text{SRC}[63:0]
\]

** Intel C/C++ Compiler Intrinsic Equivalent**

MOVLPD: 
\[
\_\_m128\_d\_mm\_loadl\_pd (\_\_m128d\_a, \text{double} *\_p)
\]

MOVLPD: 
\[
\text{void}\_\_mm\_storel\_pd (\text{double} *\_p, \_\_m128d\_a)
\]

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 5; additionally

<table>
<thead>
<tr>
<th>Exception</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>#UD</td>
<td>If VEX.L= 1.</td>
</tr>
<tr>
<td></td>
<td>If VEX.vvv != 1111B.</td>
</tr>
</tbody>
</table>
### MOVLPS—Move Low Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 12 /r MOVLPS xmm, m64</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Move two packed single-precision floating-point values from m64 to low quadword of xmm.</td>
<td></td>
</tr>
<tr>
<td>0F 13 /r MOVLPS m64, xmm</td>
<td>MR V/V</td>
<td>SSE</td>
<td>Move two packed single-precision floating-point values from low quadword of xmm to m64.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 12 /r VMOVLPS xmm2, xmm1, m64</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Merge two packed single-precision floating-point values from m64 and the high quadword of xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F.WIG 13/r VMOVLPS m64, xmm1</td>
<td>MR V/V</td>
<td>AVX</td>
<td>Move two packed single-precision floating-point values from low quadword of xmm1 to m64.</td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

This instruction cannot be used for register to register or memory to memory moves.

**128-bit Legacy SSE load:**

Move two packed single-precision floating-point values from the source 64-bit memory operand and stores them in the low 64-bits of the destination XMM register. The upper 64-bits of the XMM register are preserved. The upper 128-bits of the corresponding YMM destination register are preserved.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**VEX.128 encoded load:**

Loads two packed single-precision floating-point values from the source 64-bit memory operand (third operand), merges them with the upper 64-bits of the first source XMM register (second operand), and stores them in the low 128-bits of the
destination XMM register (first operand). The upper 128-bits of the destination YMM register are zeroed.

**128-bit store:**
Loads two packed single-precision floating-point values from the low 64-bits of the XMM register source (second operand) to the 64-bit memory location (first operand).

Note: VMOVLPS (store) (VEX.128.0F 13 /r) is legal and has the same behavior as the existing 0F 13 store. For VMOVLPS (store) (VEX.128.0F 13 /r) instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.

If VMOVLPS is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.

**Operation**

**MOVLPS (128-bit Legacy SSE load)**
DEST[63:0] ← SRC[63:0]
DEST[VLMAX-1:64] (Unmodified)

**VMOVLPS (VEX.128 encoded load)**
DEST[63:0] ← SRC2[63:0]
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

**VMOVLPS (store)**
DEST[63:0] ← SRC[63:0]

**Intel C/C++ Compiler Intrinsic Equivalent**
MOVLPS: __m128 _mm_loadl_pi ( __m128 a, __m64 *p)
MOVLPS: void _mm_storel_pi ( __m64 *p, __m128 a)

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 5; additionally
#UD
   If VEX.L= 1.
   If VEX.vvvv != 1111B.
MOVMSKPD—Extract Packed Double-Precision Floating-Point Sign Mask

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 50 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Extract 2-bit sign mask from xmm and store in reg. The upper bits of r32 or r64 are filled with zeros.</td>
</tr>
<tr>
<td>MOVMSKPD reg, xmm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:WIG 50 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Extract 2-bit sign mask from xmm2 and store in reg. The upper bits of r32 or r64 are zeroed.</td>
</tr>
<tr>
<td>VMOVMSKPD reg, xmm2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F:WIG 50 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Extract 4-bit sign mask from ymm2 and store in reg. The upper bits of r32 or r64 are zeroed.</td>
</tr>
<tr>
<td>VMOVMSKPD reg, ymm2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Extracts the sign bits from the packed double-precision floating-point values in the source operand (second operand), formats them into a 2-bit mask, and stores the mask in the destination operand (first operand). The source operand is an XMM register, and the destination operand is a general-purpose register. The mask is stored in the 2 low-order bits of the destination operand. Zero-extend the upper bits of the destination.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. The default operand size is 64-bit in 64-bit mode.

128-bit versions: The source operand is a YMM register. The destination operand is a general purpose register.

VEX.256 encoded version: The source operand is a YMM register. The destination operand is a general purpose register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

**Operation**
(V)MOVMSKPD (128-bit versions)
DEST[0] ← SRC[63]
DEST[1] ← SRC[127]
IF DEST = r32
    THEN DEST[31:2] ← 0;
    ELSE DEST[63:2] ← 0;
FI

VMOVMSKPD (VEX.256 encoded version)
DEST[0] ← SRC[63]
DEST[1] ← SRC[127]
DEST[2] ← SRC[191]
DEST[3] ← SRC[255]
IF DEST = r32
    THEN DEST[31:4] ← 0;
    ELSE DEST[63:4] ← 0;
FI

Intel C/C++ Compiler Intrinsic Equivalent
MOVMSKPD: int _mm_movemask_pd (__m128d a)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 7; additionally
#UD If VEX.vvvv != 1111B.
### MOVMSKPS—Extract Packed Single-Precision Floating-Point Sign Mask

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 50 /r MOVMSKPS reg, xmm</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Extract 4-bit sign mask from xmm and store in reg. The upper bits of r32 or r64 are filled with zeros.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F.WIG 50 /r VMOVMSKPS reg, xmm2</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Extract 4-bit sign mask from xmm2 and store in reg. The upper bits of r32 or r64 are zeroed.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.0F.WIG 50 /r VMOVMSKPS reg, ymm2</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Extract 8-bit sign mask from ymm2 and store in reg. The upper bits of r32 or r64 are zeroed.</td>
<td></td>
</tr>
</tbody>
</table>

#### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Description

Extracts the sign bits from the packed single-precision floating-point values in the source operand (second operand), formats them into a 4- or 8-bit mask, and stores the mask in the destination operand (first operand). The source operand is an XMM or YMM register, and the destination operand is a general-purpose register. The mask is stored in the 4 or 8 low-order bits of the destination operand. The upper bits of the destination operand beyond the mask are filled with zeros.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. The default operand size is 64-bit in 64-bit mode.

128-bit versions: The source operand is a YMM register. The destination operand is a general purpose register.

VEX.256 encoded version: The source operand is a YMM register. The destination operand is a general purpose register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

---

1. ModRM.MOD = 011B required
**Operation**

DEST[0] ← SRC[31];
DEST[1] ← SRC[63];
DEST[2] ← SRC[95];
DEST[3] ← SRC[127];

IF DEST = r32
    THEN DEST[31:4] ← ZeroExtend;
    ELSE DEST[63:4] ← ZeroExtend;
FI;

**(V)**MOVMSKPS (128-bit version)

DEST[0] ← SRC[31]
DEST[1] ← SRC[63]
DEST[2] ← SRC[95]
DEST[3] ← SRC[127]

IF DEST = r32
    THEN DEST[31:4] ← 0;
    ELSE DEST[63:4] ← 0;
FI

VMOVMSKPS (VEX.256 encoded version)

DEST[0] ← SRC[31]
DEST[1] ← SRC[63]
DEST[2] ← SRC[95]
DEST[3] ← SRC[127]
DEST[4] ← SRC[159]
DEST[5] ← SRC[191]
DEST[6] ← SRC[223]
DEST[7] ← SRC[255]

IF DEST = r32
    THEN DEST[31:8] ← 0;
    ELSE DEST[63:8] ← 0;
FI

**Intel C/C++ Compiler Intrinsic Equivalent**

int _mm_movemask_ps(__m128 a)
int _mm256_movemask_ps(__m256 a)

**SIMD Floating-Point Exceptions**

None.
Other Exceptions
See Exceptions Type 7; additionally

#UD If VEX.vvv != 111B.
MOVNTDQA — Load Double Quadword Non-Temporal Aligned Hint

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 2A /r MOVNTDQA xmm1, m128</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Move double quadword from m128 to xmm using non-temporal hint if WC memory type.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 2A /r VMOVNTDQA xmm1, m128</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Move double quadword from m128 to xmm using non-temporal hint if WC memory type.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

MOVNTDQA loads a double quadword from the source operand (second operand) to the destination operand (first operand) using a non-temporal hint. A processor implementation may make use of the non-temporal hint associated with this instruction if the memory source is WC (write combining) memory type. An implementation may also make use of the non-temporal hint associated with this instruction if the memory source is WB (write back) memory type.

A processor’s implementation of the non-temporal hint does not override the effective memory type semantics, but the implementation of the hint is processor dependent. For example, a processor implementation may choose to ignore the hint and process the instruction as a normal MOVDQA for any memory type. Another implementation of the hint for WC memory type may optimize data transfer throughput of WC reads. A third implementation may optimize cache reads generated by MOVNTDQA on WB memory type to reduce cache evictions.

WC Streaming Load Hint

For WC memory type in particular, the processor never appears to read the data into the cache hierarchy. Instead, the non-temporal hint may be implemented by loading a temporary internal buffer with the equivalent of an aligned cache line without filling this data to the cache. Any memory-type aliased lines in the cache will be snooped and flushed. Subsequent MOVNTDQA reads to unread portions of the WC cache line will receive data from the temporary internal buffer if data is available. The temporary internal buffer may be flushed by the processor at any time for any reason, for example:

- A load operation other than a MOVNTDQA which references memory already resident in a temporary internal buffer.
A non-WC reference to memory already resident in a temporary internal buffer.

- Interleaving of reads and writes to memory currently residing in a single temporary internal buffer.

- Repeated (V)MOVNTDQA loads of a particular 16-byte item in a streaming line.

- Certain micro-architectural conditions including resource shortages, detection of a mis-speculation condition, and various fault conditions.

The memory type of the region being read can override the non-temporal hint, if the memory address specified for the non-temporal read is not a WC memory region. Information on non-temporal reads and writes can be found in Chapter 11, "Memory Cache Control" of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*.

Because the WC protocol uses a weakly-ordered memory consistency model, an MFENCE or locked instruction should be used in conjunction with MOVNTDQA instructions if multiple processors might reference the same WC memory locations or in order to synchronize reads of a processor with writes by other agents in the system. Because of the speculative nature of fetching due to MOVNTDQA, Streaming loads must not be used to reference memory addresses that are mapped to I/O devices having side effects or when reads to these devices are destructive. For additional information on MOVNTDQA usages, see Section 12.10.3 in Chapter 12, "Programming with SSE3, SSSE3 and SSE4" of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*.

The 128-bit (V)MOVNTDQA addresses must be 16-byte aligned or the instruction will cause a #GP.

Note: In VEX-128 encoded versions, VEX.vvvv is reserved and must be 1111b, VEX.L must be 0; otherwise instructions will #UD.

**Operation**

MOVNTDQA (128bit- Legacy SSE form)

\[
\text{DEST} \leftarrow \text{SRC} \\
\text{DEST}[\text{VLMAX}-1:128] \text{ (Unmodified)}
\]

VMOVNTDQA (VEX.128 encoded form)

\[
\text{DEST} \leftarrow \text{SRC} \\
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0
\]

Intel C/C++ Compiler Intrinsic Equivalent

MOVNTDQA: \_m128 \_mm_stream_load_si128 (__m128i *p);

**Flags Affected**

None
Other Exceptions
See Exceptions Type 1.SSE4.1; additionally

#UD
If VEX.L = 1.
If VEX.vvvv != 1111B.
MOVNTDQ—Store Double Quadword Using Non-Temporal Hint

### Opcode/Instruction
<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F E7 /r MOVNTDQ m128, xmm</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move double quadword from xmm to m128 using non-temporal hint.</td>
</tr>
<tr>
<td>VEX.128.66.0F:WIG E7 /r VMOVNTDQ m128, xmm1</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move packed integer values in xmm1 to m128 using non-temporal hint.</td>
</tr>
<tr>
<td>VEX.256.66.0F:WIG E7 /r VMOVNTDQ m256, ymm1</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move packed integer values in ymm1 to m256 using non-temporal hint.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Moves the packed integers in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to prevent caching of the data during the write to memory. The source operand is an XMM register or YMM register, which is assumed to contain integer data (packed bytes, words, doublewords, or quadwords). The destination operand is a 128-bit or 256-bit memory location. The memory operand must be aligned on a 16-byte (128-bit version) or 32-byte (VEX.256 encoded version) boundary otherwise a general-protection exception (#GP) will be generated.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTDQ instructions if multiple processors might use different memory types to read/write the destination memory locations.

1. ModRM.MOD = 011B is not permitted
In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-128 encoded versions, VEX.vvvv is reserved and must be 1111b, VEX.L must be 0; otherwise instructions will #UD.

**Operation**

\[
\text{DEST} \leftarrow \text{SRC};
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

\[
\text{MOVNTDQ: } \text{void } \text{mm_stream_si128}(\text{m128i } \ast \text{p}, \text{m128i } \text{a});
\]

\[
\text{VMOVNTDQ: } \text{void } \text{mm256_stream_si256}(\text{m256i } \ast \text{p}, \text{m256i } \text{a});
\]

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 1.SSE2; additionally

#UD \hspace{1cm} \text{If VEX.vvvv } \neq 1111\text{B.}
MOVNTI—Store Doubleword Using Non-Temporal Hint

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C3 /r</td>
<td>MOVNTI m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Move doubleword from r32 to m32 using non-temporal hint.</td>
</tr>
<tr>
<td>REX.W + 0F C3 /r</td>
<td>MOVNTI m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move quadword from r64 to m64 using non-temporal hint.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRMr/m (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Moves the doubleword integer in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to minimize cache pollution during the write to memory. The source operand is a general-purpose register. The destination operand is a 32-bit memory location.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see "Caching of Temporal vs. Non-Temporal Data" in Chapter 10 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*.

Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTI instructions if multiple processors might use different memory types to read/write the destination memory locations.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

DEST ← SRC;
INSTRUCTION SET REFERENCE, M-Z

Intel C/C++ Compiler Intrinsic Equivalent

MOVNTI: void _mm_stream_si32 (int *p, int a)
MOVNTI: void _mm_stream_si64((__int64 *p, __int64 a)

SIMD Floating-Point Exceptions

None.

Protected Mode Exceptions

#GP(0) For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
#SS(0) For an illegal address in the SS segment.
#PF(fault-code) For a page fault.
#UD If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand is not aligned on a 16-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#UD If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in real address mode.
#PF(fault-code) For a page fault.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) For a page fault.
#UD If CPUID.01H:EDX.SSE2[bit 26] = 0.
If the LOCK prefix is used.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

MOVNTI—Store Doubleword Using Non-Temporal Hint
MOVNTPD—Store Packed Double-Precision Floating-Point Values Using Non-Temporal Hint

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 2B /r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move packed double-precision floating-point values from xmm to m128 using non-temporal hint.</td>
</tr>
<tr>
<td>MOVNTPD m128, xmm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:WIG 2B /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move packed double-precision values in xmm1 to m128 using non-temporal hint.</td>
</tr>
<tr>
<td>VMOVNTPD m128, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F:WIG 2B /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move packed double-precision values in ymm1 to m256 using non-temporal hint.</td>
</tr>
<tr>
<td>VMOVNTPD m256, ymm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Moves the packed double-precision floating-point values in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to prevent caching of the data during the write to memory. The source operand is an XMM register or YMM register, which is assumed to contain packed double-precision, floating-pointing data. The destination operand is a 128-bit or 256-bit memory location. The memory operand must be aligned on a 16-byte (128-bit version) or 32-byte (VEX.256 encoded version) boundary otherwise a general-protection exception (#GP) will be generated.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

1. ModRM.MOD = 011B is not permitted
Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTPD instructions if multiple processors might use different memory types to read/write the destination memory locations.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-128 encoded versions, VEX.vvvv is reserved and must be 1111b, VEX.L must be 0; otherwise instructions will #UD.

**Operation**

\[
\text{DEST} \leftarrow \text{SRC};
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

- MOVNTPD: \( \text{void } \_\text{mm}_\text{stream}\_\text{pd}(\text{double } * \_\text{m128d } a) \)
- VMOVNTPD: \( \text{void } \_\text{mm256}_\text{stream}\_\text{pd}(\text{double } * \_\text{m256d } a) \)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 1.SSE2; additionally

\#UD

If VEX.vvvv \(!=\) 1111B.
MOVNTPS—Store Packed Single-Precision Floating-Point Values Using Non-Temporal Hint

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 2B /r MOVNTPS m128, xmm</td>
<td>MR V/V</td>
<td>SSE</td>
<td>Move packed single-precision floating-point values from xmm to m128 using non-temporal hint.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F.WIG 2B /r VMOVNTPS m128, xmm1</td>
<td>MR V/V</td>
<td>AVX</td>
<td>Move packed single-precision values xmm1 to mem using non-temporal hint.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.0F.WIG 2B /r VMOVNTPS m256, ymm1</td>
<td>MR V/V</td>
<td>AVX</td>
<td>Move packed single-precision values ymm1 to mem using non-temporal hint.</td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Moves the packed single-precision floating-point values in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to prevent caching of the data during the write to memory. The source operand is an XMM register or YMM register, which is assumed to contain packed single-precision, floating-pointing. The destination operand is a 128-bit or 256-bit memory location. The memory operand must be aligned on a 16-byte (128-bit version) or 32-byte (VEX.256 encoded version) boundary otherwise a general-protection exception (#GP) will be generated.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*.

1. ModRM.MOD = 011B is not permitted
Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTPS instructions if multiple processors might use different memory types to read/write the destination memory locations.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

\[ \text{DEST} \leftarrow \text{SRC}; \]

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVNTDQ: void _mm_stream_ps(float * p, __m128 a)

VMOVNTPS: void _mm256_stream_ps (float * p, __m256 a);

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 1.SSE; additionally

#UD If VEX.vvvv != 1111B.
MOVNTQ—Store of Quadword Using Non-Temporal Hint

### Instruction Opcode

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F E7</td>
<td>MOVNTQ m64, mm</td>
<td>r</td>
<td>MR</td>
<td>Valid</td>
<td>Move quadword from mm to m64 using non-temporal hint.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRMr/m (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Moves the quadword in the source operand (second operand) to the destination operand (first operand) using a non-temporal hint to minimize cache pollution during the write to memory. The source operand is an MMX technology register, which is assumed to contain packed integer data (packed bytes, words, or doublewords). The destination operand is a 64-bit memory location.

The non-temporal hint is implemented by using a write combining (WC) memory type protocol when writing the data to memory. Using this protocol, the processor does not write the data into the cache hierarchy, nor does it fetch the corresponding cache line from memory into the cache hierarchy. The memory type of the region being written to can override the non-temporal hint, if the memory address specified for the non-temporal store is in an uncacheable (UC) or write protected (WP) memory region. For more information on non-temporal stores, see “Caching of Temporal vs. Non-Temporal Data” in Chapter 10 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*.

Because the WC protocol uses a weakly-ordered memory consistency model, a fencing operation implemented with the SFENCE or MFENCE instruction should be used in conjunction with MOVNTQ instructions if multiple processors might use different memory types to read/write the destination memory locations.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

### Operation

DEST ← SRC;

### Intel C/C++ Compiler Intrinsic Equivalent

MOVNTQ:  void _mm_stream_pi(__m64 * p, __m64 a)
SIMD Floating-Point Exceptions
None.

Other Exceptions
See Table 22-8, “Exception Conditions for Legacy SIMD/MMX Instructions without FP Exception,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.
**MOVQ—Move Quadword**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 6F /r</td>
<td>MOVQ mm, mm/m64</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Move quadword from mm/m64 to mm.</td>
</tr>
<tr>
<td>0F 7F /r</td>
<td>MOVQ mm/m64, mm</td>
<td>MR</td>
<td>V/V</td>
<td>MMX</td>
<td>Move quadword from mm to mm/m64.</td>
</tr>
<tr>
<td>F3 0F 7E</td>
<td>MOVQ xmm1, xmm2/m64</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move quadword from xmm2/mem64 to xmm1.</td>
</tr>
<tr>
<td>66 0F D6</td>
<td>MOVQ xmm2/m64, xmm1</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move quadword from xmm1 to xmm2/mem64.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Copies a quadword from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be MMX technology registers, XMM registers, or 64-bit memory locations. This instruction can be used to move a quadword between two MMX technology registers or between an MMX technology register and a 64-bit memory location, or to move data between two XMM registers or between an XMM register and a 64-bit memory location. The instruction cannot be used to transfer data between memory locations.

When the source operand is an XMM register, the low quadword is moved; when the destination operand is an XMM register, the quadword is stored to the low quadword of the register, and the high quadword is cleared to all 0s.

In 64-bit mode, use of the REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

MOVQ instruction when operating on MMX technology registers and memory locations:

\[ \text{DEST} \leftarrow \text{SRC}; \]

MOVQ instruction when source and destination operands are XMM registers:

\[ \text{DEST}[63:0] \leftarrow \text{SRC}[63:0]; \]
\[ \text{DEST}[127:64] \leftarrow 0000000000000000; \]
MOVQ instruction when source operand is XMM register and destination operand is memory location:
   DEST ← SRC[63:0];

MOVQ instruction when source operand is memory location and destination operand is XMM register:
   DEST[63:0] ← SRC;
   DEST[127:64] ← 0000000000000000H;

**Flags Affected**
None.

**Intel C/C++ Compiler Intrinsic Equivalent**
MOVQ:       m128i _mm_mov_epi64(__m128i a)

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Table 22-8, “Exception Conditions for Legacy SIMD/MMX Instructions without FP Exception,” in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*. 
MOVQ2DQ—Move Quadword from MMX Technology to XMM Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 OF D6</td>
<td>MOVQ2DQ xmm, mm</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move quadword from mmx to low quadword of xmm.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Moves the quadword from the source operand (second operand) to the low quadword of the destination operand (first operand). The source operand is an MMX technology register and the destination operand is an XMM register.

This instruction causes a transition from x87 FPU to MMX technology operation (that is, the x87 FPU top-of-stack pointer is set to 0 and the x87 FPU tag word is set to all 0s [valid]). If this instruction is executed while an x87 FPU floating-point exception is pending, the exception is handled before the MOVQ2DQ instruction is executed.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

DEST[63:0] ← SRC[63:0];
DEST[127:64] ← 0000000000000000H;

**Intel C/C++ Compiler Intrinsic Equivalent**

MOVQ2DQ: _m128i _mm_movpi64_pi64 (__m64 a)

**SIMD Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- #NM: If CR0.TS[bit 3] = 1.
- #UD: If CR0.EM[bit 2] = 1.
  - If CR4.OSFXSR[bit 9] = 0.
  - If CPUID.01H:EDX.SSE2[bit 26] = 0.
  - If the LOCK prefix is used.
- #MF: If there is a pending x87 FPU exception.
Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
## MOVS/MOVSB/MOVSW/MOVSD/MOVSQ—Move Data from String to String

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A4</td>
<td>MOVS m8, m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Move byte from address DS:(E)SI to ES:(E)DI. For 64-bit mode move byte from address (R</td>
</tr>
<tr>
<td>A5</td>
<td>MOVS m16, m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, move word from address DS:(E)SI to ES:(E)DI. For 64-bit mode move word at address (R</td>
</tr>
<tr>
<td>A5</td>
<td>MOVS m32, m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, move dword from address DS:(E)SI to ES:(E)DI. For 64-bit mode move dword from address (R</td>
</tr>
<tr>
<td>REX.W + A5</td>
<td>MOVS m64, m64</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move qword from address (R</td>
</tr>
<tr>
<td>A4</td>
<td>MOVSB</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, Move byte from address DS:(E)SI to ES:(E)DI. For 64-bit mode move byte from address (R</td>
</tr>
<tr>
<td>A5</td>
<td>MOVSW</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, move word from address DS:(E)SI to ES:(E)DI. For 64-bit mode move word at address (R</td>
</tr>
<tr>
<td>A5</td>
<td>MOVSD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, move dword from address DS:(E)SI to ES:(E)DI. For 64-bit mode move dword from address (R</td>
</tr>
<tr>
<td>REX.W + A5</td>
<td>MOVSQ</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move qword from address (R</td>
</tr>
</tbody>
</table>
Description

Moves the byte, word, or doubleword specified with the second operand (source operand) to the location specified with the first operand (destination operand). Both the source and destination operands are located in memory. The address of the source operand is read from the DS:ESI or the DS:SI registers (depending on the address-size attribute of the instruction, 32 or 16, respectively). The address of the destination operand is read from the ES:EDI or the ES:DI registers (again depending on the address-size attribute of the instruction). The DS segment may be overridden with a segment override prefix, but the ES segment cannot be overridden.

At the assembly-code level, two forms of this instruction are allowed: the "explicit-operands" form and the "no-operands" form. The explicit-operands form (specified with the MOVS mnemonic) allows the source and destination operands to be specified explicitly. Here, the source and destination operands should be symbols that indicate the size and location of the source value and the destination, respectively. This explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the source and destination operand symbols must specify the correct type (size) of the operands (bytes, words, or doublewords), but they do not have to specify the correct location. The locations of the source and destination operands are always specified by the DS:(E)SI and ES:(E)DI registers, which must be loaded correctly before the move string instruction is executed.

The no-operands form provides "short forms" of the byte, word, and doubleword versions of the MOVS instructions. Here also DS:(E)SI and ES:(E)DI are assumed to be the source and destination operands, respectively. The size of the source and destination operands is selected with the mnemonic: MOVSB (byte move), MOVSW (word move), or MOVSD (doubleword move).

After the move operation, the (E)SI and (E)DI registers are incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E)SI and (E)DI register are incremented; if the DF flag is 1, the (E)SI and (E)DI registers are decremented.) The registers are incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The MOVS, MOVSB, MOVSW, and MOVSD instructions can be preceded by the REP prefix (see "REP/REPE/REPZ /REPNE/REPNZ—Repeat String Operation Prefix" in Chapter 4 of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B, for a description of the REP prefix) for block moves of ECX bytes, words, or doublewords.

In 64-bit mode, the instruction’s default address size is 64 bits, 32-bit address size is supported using the prefix 67H. The 64-bit addresses are specified by RSI and RDI;
32-bit address are specified by ESI and EDI. Use of the REX.W prefix promotes doubleword operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

DEST ← SRC;

Non-64-bit Mode:

IF (Byte move)
    THEN IF DF = 0
        THEN
            (E)SI ← (E)SI + 1;
            (E)DI ← (E)DI + 1;
        ELSE
            (E)SI ← (E)SI - 1;
            (E)DI ← (E)DI - 1;
        FI;
    ELSE IF (Word move)
        THEN IF DF = 0
            (E)SI ← (E)SI + 2;
            (E)DI ← (E)DI + 2;
        FI;
    ELSE IF (Doubleword move)
        THEN IF DF = 0
            (E)SI ← (E)SI + 4;
            (E)DI ← (E)DI + 4;
        FI;
    ELSE
        (E)SI ← (E)SI - 2;
        (E)DI ← (E)DI - 2;
    FI;
ELSE
    (E)SI ← (E)SI - 4;
    (E)DI ← (E)DI - 4;
FI;

64-bit Mode:

IF (Byte move)
    THEN IF DF = 0
        THEN
            (R|E)SI ← (R|E)SI + 1;
            (R|E)DI ← (R|E)DI + 1;
        FI;
    ELSE
        (E)SI ← (E)SI - 4;
        (E)DI ← (E)DI - 4;
    FI;
ELSE
   (R|E)SI ← (R|E)SI + 1;
   (R|E)DI ← (R|E)DI + 1;
   FI;
ELSE IF (Word move)
   THEN IF DF = 0
      (R|E)SI ← (R|E)SI + 2;
      (R|E)DI ← (R|E)DI + 2;
      FI;
   ELSE
      (R|E)SI ← (R|E)SI - 2;
      (R|E)DI ← (R|E)DI - 2;
      FI;
   ELSE IF (Doubleword move)
      THEN IF DF = 0
         (R|E)SI ← (R|E)SI + 4;
         (R|E)DI ← (R|E)DI + 4;
         FI;
      ELSE
         (R|E)SI ← (R|E)SI - 4;
         (R|E)DI ← (R|E)DI - 4;
         FI;
      ELSE IF (Quadword move)
         THEN IF DF = 0
            (R|E)SI ← (R|E)SI + 8;
            (R|E)DI ← (R|E)DI + 8;
            FI;
         ELSE
            (R|E)SI ← (R|E)SI - 8;
            (R|E)DI ← (R|E)DI - 8;
            FI;
      FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
   If a memory operand effective address is outside the CS, DS,
   ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a NULL segment
   selector.
MOVS/MOVSB/MOVSW/MOVSD/MOVSD—Move Data from String to String

INSTRUCTION SET REFERENCE, M-Z

#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**MOVSD—Move Scalar Double-Precision Floating-Point Value**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 10 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move scalar double-precision floating-point value from xmm2/m64 to xmm1 register.</td>
</tr>
<tr>
<td>MOVSD xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F.WIG 10 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Merge scalar double-precision floating-point value from xmm2 and xmm3 to xmm1 register.</td>
</tr>
<tr>
<td>VMOVSD xmm1, xmm2, xmm3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F2.0F.WIG 10 /r</td>
<td>XM</td>
<td>V/V</td>
<td>AVX</td>
<td>Load scalar double-precision floating-point value from m64 to xmm1 register.</td>
</tr>
<tr>
<td>VMOVSD xmm1, m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F2 0F 11 /r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move scalar double-precision floating-point value from xmm1 register to xmm2/m64.</td>
</tr>
<tr>
<td>MOVSD xmm2/m64, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F.WIG 11 /r</td>
<td>MVR</td>
<td>V/V</td>
<td>AVX</td>
<td>Merge scalar double-precision floating-point value from xmm2 and xmm3 registers to xmm1.</td>
</tr>
<tr>
<td>VMOVSD xmm1, xmm2, xmm3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F2.0F.WIG 11 /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move scalar double-precision floating-point value from xmm1 register to m64.</td>
</tr>
<tr>
<td>VMOVSD m64, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>XM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MVR</td>
<td>ModRM:r/m (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

MOVSD moves a scalar double-precision floating-point value from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be XMM registers or 64-bit memory locations. This instruc-
MOVSD can be used to move a double-precision floating-point value to and from the low quadword of an XMM register and a 64-bit memory location, or to move a double-precision floating-point value between the low quadwords of two XMM registers. The instruction cannot be used to transfer data between memory locations.

For non-VEX encoded instruction syntax and when the source and destination operands are XMM registers, the high quadword of the destination operand remains unchanged. When the source operand is a memory location and destination operand is an XMM register, the high quadword of the destination operand is cleared to all 0s.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

Note: For the “VMOVSD m64, xmm1” (memory store form) instruction version, VEX.vvvv is reserved and must be 1111b, otherwise instruction will #UD.

Note: For the “VMOVSD xmm1, m64” (memory load form) instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.

VEX encoded instruction syntax supports two source operands and a destination operand if ModR/M.mod field is 11B. VEX.vvvv is used to encode the first source operand (the second operand). The low 128 bits of the destination operand stores the result of merging the low quadword of the second source operand with the quadword in bits 127:64 of the first source operand. The upper bits of the destination operand are cleared.

**Operation**

**MOVSD (128-bit Legacy SSE version: MOVSD XMM1, XMM2)**

```
DEST[63:0] ← SRC[63:0]
DEST[VLMAX-1:64] (Unmodified)
```

**MOVSD/VMOVSD (128-bit versions: MOVSD m64, xmm1 or VMOVSD m64, xmm1)**

```
DEST[63:0] ← SRC[63:0]
```

**MOVSD (128-bit Legacy SSE version: MOVSD XMM1, m64)**

```
DEST[63:0] ← SRC[63:0]
DEST[127:64] ← 0
DEST[VLMAX-1:128] (Unmodified)
```

**VMOVSD (VEX.NDS.128.F2.0F 11 /r: VMOVSD xmm1, xmm2, xmm3)**

```
DEST[63:0] ← SRC2[63:0]
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0
```

**VMOVSD (VEX.NDS.128.F2.0F 10 /r: VMOVSD xmm1, xmm2, xmm3)**

```
DEST[63:0] ← SRC2[63:0]
DEST[127:64] ← SRC1[127:64]
```
INSTRUCTION SET REFERENCE, M-Z

DEST[VLMAX-1:128] ← 0

VMOVSD (VEX.NDS.128.F2.0F 10 /r: VMOVSD xmm1, m64)
DEST[63:0] ← SRC[63:0]
DEST[VLMAX-1:64] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
MOVSD: __m128d _mm_load_sd (double *p)
MOVSD: void _mm_store_sd (double *p, __m128d a)
MOVSD: __m128d _mm_store_sd (__m128d a, __m128d b)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD If VEX.vvvv ≠ 1111B.
MOVSHPDUP—Move Packed Single-FP High and Duplicate

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 16 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE3</td>
<td>Move two single-precision floating-point values from the higher 32-bit operand of each qword in xmm2/m128 to xmm1 and duplicate each 32-bit operand to the lower 32-bits of each qword.</td>
</tr>
<tr>
<td>MOVSHDUP xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.F3.0F.W16 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move odd index single-precision floating-point values from xmm2/mem and duplicate each element into xmm1.</td>
</tr>
<tr>
<td>VMOVSHDUP xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.F3.0F.W16 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move odd index single-precision floating-point values from ymm2/mem and duplicate each element into ymm1.</td>
</tr>
<tr>
<td>VMOVSHDUP ymm1, ymm2/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Description

The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 16 bytes of data at memory location m128 are loaded and the single-precision elements in positions 1 and 3 are duplicated. When the register-register form of this operation is used, the same operation is performed but with data coming from the 128-bit source register. See Figure 4-3.
In 64-bit mode, use of the REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

Operation

**MOVSHDUP (128-bit Legacy SSE version)**

DEST[31:0] ← SRC[63:32]
DEST[95:64] ← SRC[127:96]
DEST[127:96] ← SRC[127:96]
DEST[VLMAX-1:128] (Unmodified)

**VMOVSHDUP (VEX.128 encoded version)**

DEST[31:0] ← SRC[63:32]
DEST[95:64] ← SRC[127:96]
DEST[127:96] ← SRC[127:96]
DEST[VLMAX-1:128] ← 0

**VMOVSHDUP (VEX.256 encoded version)**
DEST[31:0] ← SRC[63:32]
DEST[95:64] ← SRC[127:96]
DEST[127:96] ← SRC[127:96]
DEST[255:224] ← SRC[255:224]

**Intel C/C++ Compiler Intrinsic Equivalent**
(V)MOVSHDUP: __m128 _mm_movehdup_ps(__m128 a)
VMOVSHDUP: __m256 _mm256_movehdup_ps (__m256 a);

**Exceptions**
General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions**
None

**Other Exceptions**
See Exceptions Type 2.
MOVSLDUP—Move Packed Single-FP Low and Duplicate

**Opcode/Instruction**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 12 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE3</td>
<td>Move two single-precision floating-point values from the lower 32-bit operand of each qword in xmm2/m128 to xmm1 and duplicate each 32-bit operand to the higher 32-bits of each qword.</td>
</tr>
<tr>
<td>MOVSLDUP xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.F3.0F.WIG 12 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move even index single-precision floating-point values from xmm2/mem and duplicate each element into xmm1.</td>
</tr>
<tr>
<td>VMOVSLDUP xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.F3.0F.WIG 12 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move even index single-precision floating-point values from ymm2/mem and duplicate each element into ymm1.</td>
</tr>
<tr>
<td>VMOVSLDUP ymm1, ymm2/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 16 bytes of data at memory location m128 are loaded and the single-precision elements in positions 0 and 2 are duplicated. When the register-register form of this operation is used, the same operation is performed but with data coming from the 128-bit source register. See Figure 4-4.
In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

**MOVSLDUP (128-bit Legacy SSE version)**

DEST[31:0] ← SRC[31:0]
DEST[63:32] ← SRC[31:0]
DEST[95:64] ← SRC[95:64]
DEST[127:96] ← SRC[95:64]
DEST[VLMAX-1:128] (Unmodified)

**VMOVSLDUP (VEX.128 encoded version)**

DEST[31:0] ← SRC[31:0]
DEST[63:32] ← SRC[31:0]
DEST[95:64] ← SRC[95:64]
DEST[127:96] ← SRC[95:64]

**Figure 4-4. MOVSLDUP—Move Packed Single-FP Low and Duplicate**

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.
INSTRUCTION SET REFERENCE, M-Z

DEST[VLMAX-1:128] ← 0

VMOVSLDUP (VEX.256 encoded version)
DEST[31:0] ← SRC[31:0]
DEST[63:32] ← SRC[31:0]
DEST[95:64] ← SRC[95:64]
DEST[127:96] ← SRC[95:64]
DEST[159:128] ← SRC[159:128]

Intel C/C++ Compiler Intrinsic Equivalent

(V)MOVSLDUP: __m128 _mm_moveldup_ps(__m128 a)
VMOVSLDUP: __m256 _mm256_moveldup_ps (__m256 a);

Exceptions
General protection exception if not aligned on 16-byte boundary, regardless of segment.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.vvvv != 1111B.
## MOVSS—Move Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 10 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Move scalar single-precision floating-point value from xmm2/m32 to xmm1 register.</td>
</tr>
<tr>
<td>MOVSS xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.W10 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Merge scalar single-precision floating-point value from xmm2 and xmm3 to xmm1 register.</td>
</tr>
<tr>
<td>VMOVSS xmm1, xmm2, xmm3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F3.0F.W10 /r</td>
<td>XM</td>
<td>V/V</td>
<td>AVX</td>
<td>Load scalar single-precision floating-point value from m32 to xmm1 register.</td>
</tr>
<tr>
<td>VMOVSS xmm1, m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F3 0F 11 /r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE</td>
<td>Move scalar single-precision floating-point value from xmm1 register to xmm2/m32.</td>
</tr>
<tr>
<td>MOVSS xmm2/m32, xmm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.W11 /r</td>
<td>MVR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move scalar single-precision floating-point value from xmm2 and xmm3 to xmm1 register.</td>
</tr>
<tr>
<td>VMOVSS xmm1, xmm2, xmm3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.F3.0F.W11 /r</td>
<td>MVR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move scalar single-precision floating-point value from xmm1 register to m32.</td>
</tr>
<tr>
<td>VMOVSS m32, xmm1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRMreg (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>XM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MVR</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Moves a scalar single-precision floating-point value from the source operand (second operand) to the destination operand (first operand). The source and destination operands can be XMM registers or 32-bit memory locations. This instruction can be used to move a single-precision floating-point value to and from the low doubleword.
of an XMM register and a 32-bit memory location, or to move a single-precision floating-point value between the low doublewords of two XMM registers. The instruction cannot be used to transfer data between memory locations.

For non-VEX encoded syntax and when the source and destination operands are XMM registers, the high doublewords of the destination operand remains unchanged. When the source operand is a memory location and destination operand is an XMM registers, the high doublewords of the destination operand is cleared to all 0s.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

VEX encoded instruction syntax supports two source operands and a destination operand if ModR/M.mod field is 11B. VEX.vvvv is used to encode the first source operand (the second operand). The low 128 bits of the destination operand stores the result of merging the low dword of the second source operand with three dwords in bits 127:32 of the first source operand. The upper bits of the destination operand are cleared.

Note: For the “VMOVSS m32, xmm1” (memory store form) instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.

Note: For the “VMOVSS xmm1, m32” (memory load form) instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.

Operation

MOVSS (Legacy SSE version when the source and destination operands are both XMM registers)
DEST[31:0] ← SRC[31:0]
DEST[VLMAX-1:32] (Unmodified)

MOVSS/VMOVSS (when the source operand is an XMM register and the destination is memory)
DEST[31:0] ← SRC[31:0]

MOVSS (Legacy SSE version when the source operand is memory and the destination is an XMM register)
DEST[31:0] ← SRC[31:0]
DEST[127:32] ← 0
DEST[VLMAX-1:128] (Unmodified)

VMOVSS (VEX.NDS.128.F3.0F 11 /r where the destination is an XMM register)
DEST[31:0] ← SRC2[31:0]
DEST[VLMAX-1:128] ← 0

VMOVSS (VEX.NDS.128.F3.0F 10 /r where the source and destination are XMM registers)
MOVSS—Move Scalar Single-Precision Floating-Point Values

**DEST[31:0] ← SRC2[31:0]**
**DEST[127:32] ← SRC1[127:32]**
**DEST[VLMAX-1:128] ← 0**

**VMOVSS (VEX.NDS.128.F3.0F 101r when the source operand is memory and the destination is an XMM register)**
**DEST[31:0] ← SRC[31:0]**
**DEST[VLMAX-1:32] ← 0**

**Intel C/C++ Compiler Intrinsic Equivalent**
MOVSS: __m128 _mm_load_ss(float * p)
MOVSS: void _mm_store_ss(float * p, __m128 a)
MOVSS: __m128 _mm_move_ss(__m128 a, __m128 b)

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 5; additionally
#UD If VEX.vvvv != 1111B.
MOVSX/MOVSDX—Move with Sign-Extension

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BE /r</td>
<td>MOVSX r16, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move byte to word with sign-extension.</td>
</tr>
<tr>
<td>0F BE /r</td>
<td>MOVSX r32, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move byte to doubleword with sign-extension.</td>
</tr>
<tr>
<td>REX + 0F BE /r</td>
<td>MOVSX r64, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move byte to quadword with sign-extension.</td>
</tr>
<tr>
<td>0F BF /r</td>
<td>MOVSX r32, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move word to doubleword, with sign-extension.</td>
</tr>
<tr>
<td>REX.W + 0F BF /r</td>
<td>MOVSX r64, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move word to quadword with sign-extension.</td>
</tr>
<tr>
<td>REX.W** + 63 /r</td>
<td>MOVSDX r64, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move doubleword to quadword with sign-extension.</td>
</tr>
</tbody>
</table>

**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
** The use of MOVSDX without REX.W in 64-bit mode is discouraged, Regular MOV should be used instead of using MOVSDX without REX.W.

**Description**
Copies the contents of the source operand (register or memory location) to the destination operand (register) and sign extends the value to 16 or 32 bits (see Figure 7-6 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). The size of the converted value depends on the operand-size attribute.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**
```
DEST ← SignExtend(SRC);
```
Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
MOVUPD—Move Unaligned Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 10 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move packed double-precision floating-point values from xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>VEX.128.66.0F:WIG 10 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move unaligned packed double-precision floating-point from xmm2/mem to xmm1.</td>
</tr>
<tr>
<td>VEX.256.66.0F:WIG 10 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move unaligned packed double-precision floating-point from ymm2/mem to ymm1.</td>
</tr>
<tr>
<td>66 0F 11 /r</td>
<td>MR</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move packed double-precision floating-point values from xmm1 to xmm2/m128.</td>
</tr>
<tr>
<td>VEX.128.66.0F:WIG 11 /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move unaligned packed double-precision floating-point from xmm1 to xmm2/mem.</td>
</tr>
<tr>
<td>VEX.256.66.0F:WIG 11 /r</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Move unaligned packed double-precision floating-point from ymm1 to ymm2/mem.</td>
</tr>
</tbody>
</table>

InstructionOperand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

128-bit versions:
Moves a double quadword containing two packed double-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location.
memory location, store the contents of an XMM register into a 128-bit memory location, or move data between two XMM registers.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

When the source or destination operand is a memory operand, the operand may be unaligned on a 16-byte boundary without causing a general-protection exception (#GP) to be generated.1

To move double-precision floating-point values to and from memory locations that are known to be aligned on 16-byte boundaries, use the MOVAPD instruction.

While executing in 16-bit addressing mode, a linear address for a 128-bit data access that overlaps the end of a 16-bit segment is not allowed and is defined as reserved behavior. A specific processor implementation may or may not generate a general-protection exception (#GP) in this situation, and the address that spans the end of the segment may or may not wrap around to the beginning of the segment.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

VEX.256 encoded version:
Moves 256 bits of packed double-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load a YMM register from a 256-bit memory location, to store the contents of a YMM register into a 256-bit memory location, or to move data between two YMM registers.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

Operation

MOVUPD (128-bit load and register-copy form Legacy SSE version)
DEST[127:0] ← SRC[127:0]
DEST[VLMAX-1:128] (Unmodified)

(V)MOVUPD (128-bit store form)
DEST[127:0] ← SRC[127:0]

1. If alignment checking is enabled (CR0.AM = 1, RFLAGS.AC = 1, and CPL = 3), an alignment-check exception (#AC) may or may not be generated (depending on processor implementation) when the operand is not aligned on an 8-byte boundary.
**VMOVUPD (VEX.128 encoded version)**
DEST[127:0] ← SRC[127:0]
DEST[VLMAX-1:128] ← 0

**VMOVUPD (VEX.256 encoded version)**
DEST[255:0] ← SRC[255:0]

**Intel C/C++ Compiler Intrinsic Equivalent**
MOVUPD: __m128 _mm_loadu_pd(double * p)
MOVUPD: void _mm_storeu_pd(double *p, __m128 a)
VMOVUPD: __m256d _mm256_loadu_pd(__m256d * p);
VMOVUPD: _mm256_storeu_pd(_m256d *p, __m256d a);

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 4
Note treatment of #AC varies; additionally
#UD If VEX.vvvv != 1111B.
INSTRUCTION SET REFERENCE, M-Z

MOVUPS—Move Unaligned Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 10 /r MOVUPS xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Move packed single-precision floating-point values from xmm2/m128 to xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F.WIG 10 /r VMOVUPS xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Move unaligned packed single-precision floating-point from xmm2/mem to xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.0F.WIG 10 /r VMOVUPS ymm1, ymm2/m256</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Move unaligned packed single-precision floating-point from ymm2/mem to ymm1.</td>
<td></td>
</tr>
<tr>
<td>0F 11 /r MOVUPS xmm2/m128, xmm1</td>
<td>MR V/V</td>
<td>SSE</td>
<td>Move packed single-precision floating-point values from xmm1 to xmm2/m128.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.0F.WIG 11 /r VMOVUPS xmm2/m128, xmm1</td>
<td>MR V/V</td>
<td>AVX</td>
<td>Move unaligned packed single-precision floating-point from xmm1 to xmm2/mem.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.0F.WIG 11 /r VMOVUPS ymm2/m256, ymm1</td>
<td>MR V/V</td>
<td>AVX</td>
<td>Move unaligned packed single-precision floating-point from ymm1 to ymm2/mem.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

**128-bit versions:** Moves a double quadword containing four packed single-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load an XMM register from a 128-bit memory location, store the contents of an XMM register into a 128-bit memory location, or move data between two XMM registers.
128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

When the source or destination operand is a memory operand, the operand may be unaligned on a 16-byte boundary without causing a general-protection exception (#GP) to be generated.\(^1\)

To move packed single-precision floating-point values to and from memory locations that are known to be aligned on 16-byte boundaries, use the MOVAPS instruction.

While executing in 16-bit addressing mode, a linear address for a 128-bit data access that overlaps the end of a 16-bit segment is not allowed and is defined as reserved behavior. A specific processor implementation may or may not generate a general-protection exception (#GP) in this situation, and the address that spans the end of the segment may or may not wrap around to the beginning of the segment.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

VEX.256 encoded version: Moves 256 bits of packed single-precision floating-point values from the source operand (second operand) to the destination operand (first operand). This instruction can be used to load a YMM register from a 256-bit memory location, to store the contents of a YMM register into a 256-bit memory location, or to move data between two YMM registers.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

MOVUPS (128-bit load and register-copy form Legacy SSE version)
\[
\text{DEST}[127:0] \leftarrow \text{SRC}[127:0] \\
\text{DEST}[\text{VLMAX}-1:128] \text{ (Unmodified)}
\]

(V)MOVUPS (128-bit store form)
\[
\text{DEST}[127:0] \leftarrow \text{SRC}[127:0]
\]

VMOVUPS (VEX.128 encoded load-form)
\[
\text{DEST}[127:0] \leftarrow \text{SRC}[127:0] \\
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0
\]

VMOVUPS (VEX.256 encoded version)

---

1. If alignment checking is enabled (CR0.AM = 1, RFLAGS.AC = 1, and CPL = 3), an alignment-check exception (#AC) may or may not be generated (depending on processor implementation) when the operand is not aligned on an 8-byte boundary.
INSTRUCTION SET REFERENCE, M-Z

DEST[255:0] ← SRC[255:0]

Intel C/C++ Compiler Intrinsic Equivalent
MOVUPS: __m128 _mm_loadu_ps(double * p)
MOVUPS: void _mm_storeu_ps(double *p, __m128 a)
VMOVUPS: __m256 _mm256_loadu_ps (__m256 * p);
VMOVUPS: _mm256_storeu_ps(_m256 *p, __m256 a);

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4
Note treatment of #AC varies; additionally
#UD If VEX.vvvv != 1111B.
MOVZX—Move with Zero-Extend

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F B6 /r</td>
<td>MOVZX r16, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move byte to word with zero-extension.</td>
</tr>
<tr>
<td>0F B6 /r</td>
<td>MOVZX r32, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move byte to doubleword, zero-extension.</td>
</tr>
<tr>
<td>REX.w + 0F B6 /r</td>
<td>MOVZX r64, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move byte to quadword, zero-extension.</td>
</tr>
<tr>
<td>0F B7 /r</td>
<td>MOVZX r32, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Move word to doubleword, zero-extension.</td>
</tr>
<tr>
<td>REX.w + 0F B7 /r</td>
<td>MOVZX r64, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move word to quadword, zero-extension.</td>
</tr>
</tbody>
</table>

NOTES:
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if the REX prefix is used: AH, BH, CH, DH.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Copies the contents of the source operand (register or memory location) to the destination operand (register) and zero extends the value. The size of the converted value depends on the operand-size attribute.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bit operands. See the summary chart at the beginning of this section for encoding data and limits.

Operation

DEST ← ZeroExtend(SRC);

Flags Affected

None.
Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
MPSADBW — Compute Multiple Packed Sums of Absolute Difference

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 42 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Sums absolute 8-bit integer difference of adjacent groups of 4 byte integers in xmm1 and xmm2/m128 and writes the results in xmm1. Starting offsets within xmm1 and xmm2/m128 are determined by imm8.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.WIG 42 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Sums absolute 8-bit integer difference of adjacent groups of 4 byte integers in xmm2 and xmm3/m128 and writes the results in xmm1. Starting offsets within xmm2 and xmm3/m128 are determined by imm8.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM/reg (r, w)</td>
<td>ModRM/r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM/reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM/r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

**Description**

MPSADBW sums the absolute difference (SAD) of a pair of unsigned bytes for a group of 4 byte pairs, and produces 8 SAD results (one for each 4 byte-pairs) stored as 8 word integers in the destination operand (first operand). Each 4 byte pairs are selected from the source operand (first operand) and the destination according to the bit fields specified in the immediate byte (third operand).

The immediate byte provides two bit fields:

**SRC_OFFSET**: the value of Imm8[1:0]*32 specifies the offset of the 4 sequential source bytes in the source operand.

**DEST_OFFSET**: the value of Imm8[2]*32 specifies the offset of the first of 8 groups of 4 sequential destination bytes in the destination operand. The next four destination bytes starts at DEST_OFFSET + 8, etc.
The SAD operation is repeated 8 times, each time using the same 4 source bytes but selecting the next group of 4 destination bytes starting at the next higher byte in the destination. Each 16-bit sum is written to destination.

128-bit Legacy SSE version: The first source and destination are the same. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.
VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

If VMPSADBW is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.

**Operation**

**MPSADBW (128-bit Legacy SSE version)**

```
SRC_OFFSET ← imm8[1:0]*32
DEST_OFFSET ← imm8[2]*32
DEST_BYTE0 ← DEST[DEST_OFFSET+7:DEST_OFFSET]
DEST_BYTE1 ← DEST[DEST_OFFSET+15:DEST_OFFSET+8]
DEST_BYTE2 ← DEST[DEST_OFFSET+23:DEST_OFFSET+16]
DEST_BYTE3 ← DEST[DEST_OFFSET+31:DEST_OFFSET+24]
DEST_BYTE4 ← DEST[DEST_OFFSET+39:DEST_OFFSET+32]
DEST_BYTE5 ← DEST[DEST_OFFSET+47:DEST_OFFSET+40]
DEST_BYTE6 ← DEST[DEST_OFFSET+55:DEST_OFFSET+48]
DEST_BYTE7 ← DEST[DEST_OFFSET+63:DEST_OFFSET+56]
DEST_BYTE8 ← DEST[DEST_OFFSET+71:DEST_OFFSET+64]
DEST_BYTE9 ← DEST[DEST_OFFSET+79:DEST_OFFSET+72]
DEST_BYTE10 ← DEST[DEST_OFFSET+87:DEST_OFFSET+80]

SRC_BYTE0 ← SRC[SRC_OFFSET+7:SRC_OFFSET]
SRC_BYTE1 ← SRC[SRC_OFFSET+15:SRC_OFFSET+8]
SRC_BYTE2 ← SRC[SRC_OFFSET+23:SRC_OFFSET+16]
SRC_BYTE3 ← SRC[SRC_OFFSET+31:SRC_OFFSET+24]

TEMP0 ← ABS(DEST_BYTE0 - SRC_BYTE0)
TEMP1 ← ABS(DEST_BYTE1 - SRC_BYTE1)
TEMP2 ← ABS(DEST_BYTE2 - SRC_BYTE2)
TEMP3 ← ABS(DEST_BYTE3 - SRC_BYTE3)
DEST[15:0] ← TEMP0 + TEMP1 + TEMP2 + TEMP3

TEMP0 ← ABS(DEST_BYTE1 - SRC_BYTE0)
TEMP1 ← ABS(DEST_BYTE2 - SRC_BYTE1)
TEMP2 ← ABS(DEST_BYTE3 - SRC_BYTE2)
TEMP3 ← ABS(DEST_BYTE4 - SRC_BYTE3)
DEST[31:16] ← TEMP0 + TEMP1 + TEMP2 + TEMP3
```
VMPSADBW (VEX.128 encoded version)
SRC2_OFFSET ← imm8[1:0]*32
SRC1_OFFSET ← imm8[2]*32
SRC1_BYTE0 ← SRC1[SRC1_OFFSET+7:SRC1_OFFSET]
SRC1_BYTE1 ← SRC1[SRC1_OFFSET+15:SRC1_OFFSET+8]
SRC1_BYTE2 ← SRC1[SRC1_OFFSET+23:SRC1_OFFSET+16]
SRC1_BYTE3 ← SRC1[SRC1_OFFSET+31:SRC1_OFFSET+24]
SRC1_BYTE4 ← SRC1[SRC1_OFFSET+39:SRC1_OFFSET+32]
SRC1_BYTE5 ← SRC1[SRC1_OFFSET+47:SRC1_OFFSET+40]
SRC1_BYTE6 ← SRC1[SRC1_OFFSET+55:SRC1_OFFSET+48]
SRC1_BYTE7 ← SRC1[SRC1_OFFSET+63:SRC1_OFFSET+56]
SRC1_BYTE8 ← SRC1[SRC1_OFFSET+71:SRC1_OFFSET+64]
SRC1_BYTE9 ← SRC1[SRC1_OFFSET+79:SRC1_OFFSET+72]
SRC1_BYTE10 ← SRC1[SRC1_OFFSET+87:SRC1_OFFSET+80]

SRC2_BYTE0 ← SRC2[SRC2_OFFSET+7:SRC2_OFFSET]
SRC2_BYTE1 ← SRC2[SRC2_OFFSET+15:SRC2_OFFSET+8]
SRC2_BYTE2 ← SRC2[SRC2_OFFSET+23:SRC2_OFFSET+16]
SRC2_BYTE3 ← SRC2[SRC2_OFFSET+31:SRC2_OFFSET+24]

TEMP0 ← ABS(SRC1_BYTE0 - SRC2_BYTE0)
TEMP1 ← ABS(SRC1_BYTE1 - SRC2_BYTE1)
TEMP2 ← ABS(SRC1_BYTE2 - SRC2_BYTE2)
TEMP3 ← ABS(SRC1_BYTE3 - SRC2_BYTE3)
DEST[15:0] ← TEMP0 + TEMP1 + TEMP2 + TEMP3
TEMP0 ← ABS(SRC1_BYTE0 - SRC2_BYTE0)
TEMP1 ← ABS(SRC1_BYTE1 - SRC2_BYTE1)
TEMP2 ← ABS(SRC1_BYTE2 - SRC2_BYTE2)
TEMP3 ← ABS(SRC1_BYTE3 - SRC2_BYTE3)
DEST[31:16] ← TEMP0 + TEMP1 + TEMP2 + TEMP3
TEMP0 ← ABS(SRC1_BYTE0 - SRC2_BYTE0)
TEMP1 ← ABS(SRC1_BYTE1 - SRC2_BYTE1)
TEMP2 ← ABS(SRC1_BYTE2 - SRC2_BYTE2)
TEMP3 ← ABS(SRC1_BYTE3 - SRC2_BYTE3)
DEST[47:32] ← TEMP0 + TEMP1 + TEMP2 + TEMP3
TEMP0 ← ABS(SRC1_BYTE0 - SRC2_BYTE0)
TEMP1 ← ABS(SRC1_BYTE1 - SRC2_BYTE1)
TEMP2 ← ABS(SRC1_BYTE2 - SRC2_BYTE2)
TEMP3 ← ABS(SRC1_BYTE3 - SRC2_BYTE3)
DEST[63:48] ← TEMP0 + TEMP1 + TEMP2 + TEMP3
TEMP0 ← ABS(SRC1_BYTE0 - SRC2_BYTE0)
TEMP1 ← ABS(SRC1_BYTE1 - SRC2_BYTE1)
TEMP2 ← ABS(SRC1_BYTE2 - SRC2_BYTE2)
TEMP3 ← ABS(SRC1_BYTE3 - SRC2_BYTE3)
DEST[79:64] ← TEMP0 + TEMP1 + TEMP2 + TEMP3
TEMP0 ← ABS(SRC1_BYTE0 - SRC2_BYTE0)
TEMP1 ← ABS(SRC1_BYTE1 - SRC2_BYTE1)
TEMP2 ← ABS(SRC1_BYTE2 - SRC2_BYTE2)
MPSADBW — Compute Multiple Packed Sums of Absolute Difference

INSTRUCTION SET REFERENCE, M-Z

TEMP3 \leftarrow \text{ABS} (\text{SRC1\_BYTE8} - \text{SRC2\_BYTE3})
\text{DEST}[95:80] \leftarrow \text{TEMP0} + \text{TEMP1} + \text{TEMP2} + \text{TEMP3}
TEMP0 \leftarrow \text{ABS} (\text{SRC1\_BYTE6} - \text{SRC2\_BYTE0})
TEMP1 \leftarrow \text{ABS} (\text{SRC1\_BYTE7} - \text{SRC2\_BYTE1})
TEMP2 \leftarrow \text{ABS} (\text{SRC1\_BYTE8} - \text{SRC2\_BYTE2})
TEMP3 \leftarrow \text{ABS} (\text{SRC1\_BYTE9} - \text{SRC2\_BYTE3})
\text{DEST}[111:96] \leftarrow \text{TEMP0} + \text{TEMP1} + \text{TEMP2} + \text{TEMP3}

\text{TEMP0} \leftarrow \text{ABS} (\text{SRC1\_BYTE7} - \text{SRC2\_BYTE0})
\text{TEMP1} \leftarrow \text{ABS} (\text{SRC1\_BYTE8} - \text{SRC2\_BYTE1})
\text{TEMP2} \leftarrow \text{ABS} (\text{SRC1\_BYTE9} - \text{SRC2\_BYTE2})
\text{TEMP3} \leftarrow \text{ABS} (\text{SRC1\_BYTE10} - \text{SRC2\_BYTE3})
\text{DEST}[127:112] \leftarrow \text{TEMP0} + \text{TEMP1} + \text{TEMP2} + \text{TEMP3}
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0

\textbf{Intel C/C++ Compiler Intrinsic Equivalent}

\begin{verbatim}
MPSADBW:  __m128i _mm_mpsadbw_epu8 (__m128i s1, __m128i s2, const int mask);
\end{verbatim}

\textbf{Flags Affected}

None

\textbf{Other Exceptions}

See Exceptions Type 4; additionally

\#UD \quad \text{If} \ VEX.L = 1.
MUL—Unsigned Multiply

**Opcode—Instruction**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/ En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /4</td>
<td>MUL r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned multiply (AX ← AL * r/m8).</td>
</tr>
<tr>
<td>REX + F6 /4</td>
<td>MUL r/m8</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned multiply (AX ← AL * r/m8).</td>
</tr>
<tr>
<td>F7 /4</td>
<td>MUL r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned multiply (DX:AX ← AX * r/m16).</td>
</tr>
<tr>
<td>F7 /4</td>
<td>MUL r/m32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Unsigned multiply (EDX:EAX ← EAX * r/m32).</td>
</tr>
<tr>
<td>REX.W + F7 /4</td>
<td>MUL r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned multiply (RDX:RAX ← RAX * r/m64).</td>
</tr>
</tbody>
</table>

**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an unsigned multiplication of the first operand (destination operand) and the second operand (source operand) and stores the result in the destination operand. The destination operand is an implied operand located in register AL, AX or EAX (depending on the size of the operand); the source operand is located in a general-purpose register or a memory location. The action of this instruction and the location of the result depends on the opcode and the operand size as shown in Table 4-9.

The result is stored in register AX, register pair DX:AX, or register pair EDX:EAX (depending on the operand size), with the high-order bits of the product contained in register AH, DX, or EDX, respectively. If the high-order bits of the product are 0, the CF and OF flags are cleared; otherwise, the flags are set.

In 64-bit mode, the instruction’s default operation size is 32 bits. Use of the REX.R prefix permits access to additional registers (R8-R15). Use of the REX.W prefix promotes operation to 64 bits.

See the summary chart at the beginning of this section for encoding data and limits.
**Operation**

IF (Byte operation)
   THEN
      $AX \leftarrow AL \times SRC$;
   ELSE (* Word or doubleword operation *)
      IF $OperandSize = 16$
         THEN
            $DX:AX \leftarrow AX \times SRC$;
         ELSE IF $OperandSize = 32$
            THEN $EDX:EAX \leftarrow EAX \times SRC$; FI;
         ELSE (* $OperandSize = 64$ *)
            $RDX:RAX \leftarrow RAX \times SRC$;
       FI;
   FI;

**Flags Affected**

The OF and CF flags are set to 0 if the upper half of the result is 0; otherwise, they are set to 1. The SF, ZF, AF, and PF flags are undefined.

**Protected Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

---

**Table 4-9. MUL Results**

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Source 1</th>
<th>Source 2</th>
<th>Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
<td>AL</td>
<td>r/m8</td>
<td>AX</td>
</tr>
<tr>
<td>Word</td>
<td>AX</td>
<td>r/m16</td>
<td>DX:AX</td>
</tr>
<tr>
<td>Doubleword</td>
<td>EAX</td>
<td>r/m32</td>
<td>EDX:EAX</td>
</tr>
<tr>
<td>Quadword</td>
<td>RAX</td>
<td>r/m64</td>
<td>RDX:RAX</td>
</tr>
</tbody>
</table>
Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
MULPD—Multiply Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 59 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Multiply packed double-precision floating-point values in xmm2/m128 by xmm1.</td>
</tr>
<tr>
<td>MULPD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F:WIG 59 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply packed double-precision floating-point values from xmm3/mem to xmm2 and stores result in xmm1.</td>
</tr>
<tr>
<td>VMULPD xmm1,xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F:WIG 59 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply packed double-precision floating-point values from ymm3/mem to ymm2 and stores result in ymm1.</td>
</tr>
<tr>
<td>VMULPD ymm1, ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD multiply of the two or four packed double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the packed double-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 11-3 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a SIMD double-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the destination YMM register destination are zeroed.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**MULPD (128-bit Legacy SSE version)**
DEST[63:0] ← DEST[63:0] * SRC[63:0]
DEST[127:64] ← DEST[127:64] * SRC[127:64]
DEST[VLMAX-1:128] (Unmodified)

**VMULPD (VEX.128 encoded version)**
DEST[63:0] ← SRC1[63:0] * SRC2[63:0]
DEST[127:64] ← SRC1[127:64] * SRC2[127:64]
DEST[VLMAX-1:128] ← 0

**VMULPD (VEX.256 encoded version)**
DEST[63:0] ← SRC1[63:0] * SRC2[63:0]
DEST[127:64] ← SRC1[127:64] * SRC2[127:64]

**Intel C/C++ Compiler Intrinsic Equivalent**

MULPD: __m128d _mm_mul_pd (m128d a, m128d b)
VMULPD: __m256d _mm256_mul_pd (__m256d a, __m256d b);

**SIMD Floating-Point Exceptions**
Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**
See Exceptions Type 2
INSTRUCTION SET REFERENCE, M-Z

MULPS—Multiply Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 59 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Multiply packed single-precision floating-point values in xmm2/mem by xmm1.</td>
</tr>
<tr>
<td>MULPS xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 59 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply packed single-precision floating-point values from xmm3/mem to xmm2 and stores result in xmm1.</td>
</tr>
<tr>
<td>VMULPS xmm1,xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 59 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply packed single-precision floating-point values from ymm3/mem to ymm2 and stores result in ymm1.</td>
</tr>
<tr>
<td>VMULPS ymm1, ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD multiply of the four packed single-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the packed single-precision floating-point results in the destination operand. See Figure 10-5 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a SIMD single-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the destination YMM register destination are zeroed.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**MULPS (128-bit Legacy SSE version)**
DEST[31:0] ← SRC1[31:0] * SRC2[31:0]
DEST[95:64] ← SRC1[95:64] * SRC2[95:64]
DEST[VLMAX-1:128] (Unmodified)

**VMULPS (VEX.128 encoded version)**
DEST[31:0] ← SRC1[31:0] * SRC2[31:0]
DEST[95:64] ← SRC1[95:64] * SRC2[95:64]
DEST[VLMAX-1:128] ← 0

**VMULPS (VEX.256 encoded version)**
DEST[31:0] ← SRC1[31:0] * SRC2[31:0]
DEST[95:64] ← SRC1[95:64] * SRC2[95:64]

**Intel C/C++ Compiler Intrinsic Equivalent**
MULPS: __m128 _mm_mul_ps(__m128 a, __m128 b)
VMULPS: __m256 _mm256_mul_ps (__m256 a, __m256 b);

**SIMD Floating-Point Exceptions**
Overflow, Underflow, Invalid, Precision, Denormal.

**Other Exceptions**
See Exceptions Type 2
**MULSD—Multiply Scalar Double-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 59 /r MULSD xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Multiply the low double-precision floating-point value in xmm2/mem64 by low double-precision floating-point value in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F:WIG 59/r VMULSD xmm1,xmm2, xmm3/m64</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Multiply the low double-precision floating-point value in xmm3/mem64 by low double precision floating-point value in xmm2.</td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Multiplies the low double-precision floating-point value in the source operand (second operand) by the low double-precision floating-point value in the destination operand (first operand), and stores the double-precision floating-point result in the destination operand. The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. The high quadword of the destination operand remains unchanged. See Figure 11-4 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an illustration of a scalar double-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VMAXX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAXX-1:128) of the destination YMM register are zeroed.

**Operation**
MULSD (128-bit Legacy SSE version)
DEST[63:0] ← DEST[63:0] * SRC[63:0]
DEST[VLMAX-1:64] (Unmodified)

VMULSD (VEX.128 encoded version)
DEST[63:0] ← SRC1[63:0] * SRC2[63:0]
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
MULSD: _m128d _mm_mul_sd (m128d a, m128d b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Other Exceptions
See Exceptions Type 3
**MULSS—Multiply Scalar Single-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 59 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Multiply the low single-precision floating-point value in \texttt{xmm2/mem} by the low single-precision floating-point value in \texttt{xmm1}.</td>
</tr>
<tr>
<td>MULSS \texttt{xmm1, xmm2/m32}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.WIG 59 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply the low single-precision floating-point value in \texttt{xmm3/mem} by the low single-precision floating-point value in \texttt{xmm2}.</td>
</tr>
<tr>
<td>VMULSS \texttt{xmm1,xmm2, xmm3/m32}</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Multiplies the low single-precision floating-point value from the source operand (second operand) by the low single-precision floating-point value in the destination operand (first operand), and stores the single-precision floating-point result in the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The three high-order double-words of the destination operand remain unchanged. See Figure 10-6 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an illustration of a scalar single-precision floating-point operation.

In 64-bit mode, use of the REX.R prefix permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

**MULSS (128-bit Legacy SSE version)**
INSTRUCTION SET REFERENCE, M-Z

DEST[31:0] ← DEST[31:0] * SRC[31:0]
DEST[VLMAX-1:32] (Unmodified)

VMULSS (VEX.128 encoded version)
DEST[31:0] ← SRC1[31:0] * SRC2[31:0]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
MULSS: __m128 _mm_mul_ss(__m128 a, __m128 b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Other Exceptions
See Exceptions Type 3
MWAIT—Monitor Wait

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 C9</td>
<td>MWAIT</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>A hint that allow the processor to stop instruction execution and enter an implemenation-dependent optimized state until occurrence of a class of events.</td>
</tr>
</tbody>
</table>

**InstructionOperand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

MWAIT instruction provides hints to allow the processor to enter an implementation-dependent optimized state. There are two principal targeted usages: address-range monitor and advanced power management. Both usages of MWAIT require the use of the MONITOR instruction.

A CPUID feature flag (ECX bit 3; CPUID executed EAX = 1) indicates the availability of MONITOR and MWAIT in the processor. When set, MWAIT may be executed only at privilege level 0 (use at any other privilege level results in an invalid-opcode exception). The operating system or system BIOS may disable this instruction by using the IA32_MISC_ENABLE MSR; disabling MWAIT clears the CPUID feature flag and causes execution to generate an illegal opcode exception.

This instruction's operation is the same in non-64-bit modes and 64-bit mode.

**MWAIT for Address Range Monitoring**

For address-range monitoring, the MWAIT instruction operates with the MONITOR instruction. The two instructions allow the definition of an address at which to wait (MONITOR) and a implementation-dependent-optimized operation to commence at the wait address (MWAIT). The execution of MWAIT is a hint to the processor that it can enter an implementation-dependent-optimized state while waiting for an event or a store operation to the address range armed by MONITOR.

ECX specifies optional extensions for the MWAIT instruction. EAX may contain hints such as the preferred optimized state the processor should enter.

For Pentium 4 processors (CPUID signature family 15 and model 3), non-zero values for EAX and ECX are reserved. Later processors defined ECX=1 as a valid extension (see below).
The following cause the processor to exit the implementation-dependent-optimized state: a store to the address range armed by the MONITOR instruction, an NMI or SMI, a debug exception, a machine check exception, the BINIT# signal, the INIT# signal, and the RESET# signal. Other implementation-dependent events may also cause the processor to exit the implementation-dependent-optimized state.

In addition, an external interrupt causes the processor to exit the implementation-dependent-optimized state if either (1) the interrupt would be delivered to software (e.g., if HLT had been executed instead of MWAIT); or (2) ECX[0] = 1. Implementation-specific conditions may result in an interrupt causing the processor to exit the implementation-dependent-optimized state even if interrupts are masked and ECX[0] = 0.

Following exit from the implementation-dependent-optimized state, control passes to the instruction following the MWAIT instruction. A pending interrupt that is not masked (including an NMI or an SMI) may be delivered before execution of that instruction. Unlike the HLT instruction, the MWAIT instruction does not support a restart at the MWAIT instruction following the handling of an SMI.

If the preceding MONITOR instruction did not successfully arm an address range or if the MONITOR instruction has not been executed prior to executing MWAIT, then the processor will not enter the implementation-dependent-optimized state. Execution will resume at the instruction following the MWAIT.

**MWAIT for Power Management**

MWAIT accepts a hint and optional extension to the processor that it can enter a specified target C state while waiting for an event or a store operation to the address range armed by MONITOR. Support for MWAIT extensions for power management is indicated by CPUID.05H.ECX[0] reporting 1.

EAX and ECX will be used to communicate the additional information to the MWAIT instruction, such as the kind of optimized state the processor should enter. ECX specifies optional extensions for the MWAIT instruction. EAX may contain hints such as the preferred optimized state the processor should enter. Implementation-specific conditions may cause a processor to ignore the hint and enter a different optimized state. Future processor implementations may implement several optimized "waiting" states and will select among those states based on the hint argument.

Table 4-10 describes the meaning of ECX and EAX registers for MWAIT extensions.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Treat masked interrupts as break events (e.g., if EFLAGS.IF=0). May be set only if CPUID.01H.ECX.MONITOR[bit 3] = 1.</td>
</tr>
<tr>
<td>31: 1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Note that if MWAIT is used to enter any of the C-states that are numerically higher than C1, a store to the address range armed by the MONITOR instruction will cause the processor to exit MWAIT only if the store was originated by other processor agents. A store from non-processor agent might not cause the processor to exit MWAIT in such cases.

For additional details of MWAIT extensions, see Chapter 14, “Power and Thermal Management,” of *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A*.

**Operation**

(* MWAIT takes the argument in EAX as a hint extension and is architected to take the argument in ECX as an instruction extension MWAIT EAX, ECX *)

{  
  WHILE ("Monitor Hardware is in armed state") {  
    implementation_dependent_optimized_state(EAX, ECX);  
  }
  Set the state of Monitor Hardware as triggered;
}

**Intel C/C++ Compiler Intrinsic Equivalent**

MWAIT: void _mm_mwait(unsigned extensions, unsigned hints)

**Example**

MONITOR/MWAIT instruction pair must be coded in the same loop because execution of the MWAIT instruction will trigger the monitor hardware. It is not a proper usage to execute MONITOR once and then execute MWAIT in a loop. Setting up MONITOR without executing MWAIT has no adverse effects.

Typically the MONITOR/MWAIT pair is used in a sequence, such as:

EAX = Logical Address(Trigger)
ECX = 0 ("Hints *")

### Table 4-11. MWAIT Hints Register (EAX)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 : 0</td>
<td>Sub C-state within a C-state, indicated by bits [7:4]</td>
</tr>
</tbody>
</table>
| 7 : 4 | Target C-state*  
Value of 0 means C1; 1 means C2 and so on  
Value of 01111B means C0  
Note: Target C states for MWAIT extensions are processor-specific C-states, not ACPI C-states |
| 31: 8 | Reserved |
INSTRUCTION SET REFERENCE, M-Z

EDX = 0 (* Hints *)

IF (!trigger_store_happened) {
  MONITOR EAX, ECX, EDX
  IF (!trigger_store_happened) {
    MWAIT EAX, ECX
  }
}

The above code sequence makes sure that a triggering store does not happen between the first check of the trigger and the execution of the monitor instruction. Without the second check that triggering store would go un-noticed. Typical usage of MONITOR and MWAIT would have the above code sequence within a loop.

Numeric Exceptions
None

Protected Mode Exceptions
#GP(0) If ECX[31:1] ≠ 0.
  If ECX[0] = 1 and CPUID.05H:ECX[bit 3] = 0.
#UD If CPUID.01H:ECX.MONITOR[bit 3] = 0.
  If current privilege level is not 0.

Real Address Mode Exceptions
#GP If ECX[31:1] ≠ 0.
  If ECX[0] = 1 and CPUID.05H:ECX[bit 3] = 0.
#UD If CPUID.01H:ECX.MONITOR[bit 3] = 0.

Virtual 8086 Mode Exceptions
#UD The MWAIT instruction is not recognized in virtual-8086 mode (even if CPUID.01H:ECX.MONITOR[bit 3] = 1).

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If RCX[63:1] ≠ 0.
  If RCX[0] = 1 and CPUID.05H:ECX[bit 3] = 0.
#UD If the current privilege level is not 0.
  If CPUID.01H:ECX.MONITOR[bit 3] = 0.
NEG—Two’s Complement Negation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /3</td>
<td>NEG r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Two’s complement negate r/m8.</td>
</tr>
<tr>
<td>REX + F6 /3</td>
<td>NEG r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Two’s complement negate r/m8.</td>
</tr>
<tr>
<td>F7 /3</td>
<td>NEG r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Two’s complement negate r/m16.</td>
</tr>
<tr>
<td>F7 /3</td>
<td>NEG r/m32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Two’s complement negate r/m32.</td>
</tr>
<tr>
<td>REX.W + F7 /3</td>
<td>NEG r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Two’s complement negate r/m64.</td>
</tr>
</tbody>
</table>

NOTES:
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r, w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Replaces the value of operand (the destination operand) with its two’s complement. (This operation is equivalent to subtracting the operand from 0.) The destination operand is located in a general-purpose register or a memory location.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF DEST = 0
    THEN CF ← 0;
    ELSE CF ← 1;
FI;
DEST ← - (DEST)
Flags Affected
The CF flag set to 0 if the source operand is 0; otherwise it is set to 1. The OF, SF, ZF, AF, and PF flags are set according to the result.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same as for protected mode exceptions.
64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) For a page fault.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
**NOP—No Operation**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>NOP</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>One byte no-operation instruction.</td>
</tr>
<tr>
<td>0F 1F /0</td>
<td>NOP r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Multi-byte no-operation instruction.</td>
</tr>
<tr>
<td>0F 1F /0</td>
<td>NOP r/m32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Multi-byte no-operation instruction.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

This instruction performs no operation. It is a one-byte or multi-byte NOP that takes up space in the instruction stream but does not impact machine context, except for the EIP register.

The multi-byte form of NOP is available on processors with model encoding:

- CPUID.01H.EAX[Bytes 11:8] = 0110B or 1111B

The multi-byte NOP instruction does not alter the content of a register and will not issue a memory operation. The instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

The one-byte NOP instruction is an alias mnemonic for the XCHG (E)AX, (E)AX instruction.

The multi-byte NOP instruction performs no operation on supported processors and generates undefined opcode exception on processors that do not support the multi-byte NOP instruction.

The memory operand form of the instruction allows software to create a byte sequence of "no operation" as one instruction. For situations where multiple-byte NOPs are needed, the recommended operations (32-bit mode and 64-bit mode) are:
**Flags Affected**

None.

**Exceptions (All Operating Modes)**

#UD If the LOCK prefix is used.
NOT—One's Complement Negation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /2</td>
<td>NOT r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse each bit of r/m8.</td>
</tr>
<tr>
<td>REX + F6 /2</td>
<td>NOT r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Reverse each bit of r/m8.</td>
</tr>
<tr>
<td>F7 /2</td>
<td>NOT r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse each bit of r/m16.</td>
</tr>
<tr>
<td>F7 /2</td>
<td>NOT r/m32</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Reverse each bit of r/m32.</td>
</tr>
<tr>
<td>REX.W + F7 /2</td>
<td>NOT r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Reverse each bit of r/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM</td>
<td>r/m (r, w)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise NOT operation (each 1 is set to 0, and each 0 is set to 1) on the destination operand and stores the result in the destination operand location. The destination operand can be a register or a memory location.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

DEST ← NOT DEST;

**Flags Affected**

None.

**Protected Mode Exceptions**

#GP(0) If the destination operand points to a non-writable segment.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Compatibility Mode Exceptions**

Same as for protected mode exceptions.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
## OR—Logical Inclusive OR

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0C ib</td>
<td>OR AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>AL OR imm8.</td>
</tr>
<tr>
<td>0D iw</td>
<td>OR AX, imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>AX OR imm16.</td>
</tr>
<tr>
<td>0D id</td>
<td>OR EAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>EAX OR imm32.</td>
<td></td>
</tr>
<tr>
<td>REX.w + 0D id</td>
<td>OR RAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>N.E.</td>
<td>RAX OR imm32 (sign-extended).</td>
</tr>
<tr>
<td>80 /1 ib</td>
<td>OR r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m8 OR imm8.</td>
</tr>
<tr>
<td>REX + 80 /1 ib</td>
<td>OR r/m8*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m8 OR imm8.</td>
</tr>
<tr>
<td>81 /1 iw</td>
<td>OR r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 OR imm16.</td>
</tr>
<tr>
<td>81 /1 id</td>
<td>OR r/m32, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>r/m32 OR imm32.</td>
<td></td>
</tr>
<tr>
<td>REX.w + 81 /1 id</td>
<td>OR r/m64, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 OR imm32 (sign-extended).</td>
</tr>
<tr>
<td>83 /1 ib</td>
<td>OR r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 OR imm8 (sign-extended).</td>
</tr>
<tr>
<td>83 /1 ib</td>
<td>OR r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 OR imm8 (sign-extended).</td>
</tr>
<tr>
<td>REX.w + 83 /1 ib</td>
<td>OR r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 OR imm8 (sign-extended).</td>
</tr>
<tr>
<td>08 /r</td>
<td>OR r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m8 OR r8.</td>
</tr>
<tr>
<td>REX + 08 /r</td>
<td>OR r/m8*, r8*</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m8 OR r8.</td>
</tr>
<tr>
<td>09 /r</td>
<td>OR r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 OR r16.</td>
</tr>
<tr>
<td>09 /r</td>
<td>OR r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>r/m32 OR r32.</td>
<td></td>
</tr>
<tr>
<td>REX.w + 09 /r</td>
<td>OR r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 OR r64.</td>
</tr>
<tr>
<td>0A /r</td>
<td>OR r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>r8 OR r/m8.</td>
</tr>
<tr>
<td>REX + 0A /r</td>
<td>OR r8*, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>r8 OR r/m8.</td>
</tr>
<tr>
<td>0B /r</td>
<td>OR r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>r16 OR r/m16.</td>
</tr>
<tr>
<td>0B /r</td>
<td>OR r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>r32 OR r/m32.</td>
<td></td>
</tr>
<tr>
<td>REX.w + 0B /r</td>
<td>OR r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>r64 OR r/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
Description

Performs a bitwise inclusive OR operation between the destination (first) and source (second) operands and stores the result in the destination operand location. The source operand can be an immediate, a register, or a memory location; the destination operand can be a register or a memory location. (However, two memory operands cannot be used in one instruction.) Each bit of the result of the OR instruction is set to 0 if both corresponding bits of the first and second operands are 0; otherwise, each bit is set to 1.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

DEST ← DEST OR SRC;

Flags Affected

The OF and CF flags are cleared; the SF, ZF, and PF flags are set according to the result. The state of the AF flag is undefined.

Protected Mode Exceptions

#GP(0) If the destination operand points to a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

OR—Logical Inclusive OR
INSTRUCTION SET REFERENCE, M-Z

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same as for protected mode exceptions.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.
**ORPD—Bitwise Logical OR of Double-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 56 /r ORPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Bitwise OR of xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 56 /r VORPD xmm1,xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical OR of packed double-precision floating-point values in xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 56 /r VORPD ymm1, ymm2, ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical OR of packed double-precision floating-point values in ymm2 and ymm3/mem.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical OR of the two or four packed double-precision floating-point values from the first source operand and the second source operand, and stores the result in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the destination YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

If VORPD is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.
Operation

**ORPD (128-bit Legacy SSE version)**
DEST[63:0] ← DEST[63:0] BITWISE OR SRC[63:0]
DEST[127:64] ← DEST[127:64] BITWISE OR SRC[127:64]
DEST[VLMAX-1:128] (Unmodified)

**VORPD (VEX.128 encoded version)**
DEST[63:0] ← SRC1[63:0] BITWISE OR SRC2[63:0]
DEST[127:64] ← SRC1[127:64] BITWISE OR SRC2[127:64]
DEST[VLMAX-1:128] ← 0

**VORPD (VEX.256 encoded version)**
DEST[63:0] ← SRC1[63:0] BITWISE OR SRC2[63:0]
DEST[127:64] ← SRC1[127:64] BITWISE OR SRC2[127:64]

Intel® C/C++ Compiler Intrinsic Equivalent
ORPD: __m128d _mm_or_pd(__m128d a, __m128d b);
VORPD: __m256d _mm256_or_pd (__m256d a, __m256d b);

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
ORPS—Bitwise Logical OR of Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 56 /r ORPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Bitwise OR of xmm1 and xmm2/m128.</td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 56 /r VORPS xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical OR of packed single-precision floating-point values in xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 56 /r VORPS ymm1, ymm2, ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical OR of packed single-precision floating-point values in ymm2 and ymm3/mem.</td>
</tr>
</tbody>
</table>

**InstructionOperand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical OR of the four or eight packed single-precision floating-point values from the first source operand and the second source operand, and stores the result in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the destination YMM register destination are zeroed.

VEX.256 Encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

If VORPS is encoded with VEX.L= 1, an attempt to execute the instruction encoded with VEX.L= 1 will cause an #UD exception.
**INSTRUCTION SET REFERENCE, M-Z**

**Operation**

**ORPS (128-bit Legacy SSE version)**

DEST[31:0] ← SRC1[31:0] BITWISE OR SRC2[31:0]
DEST[95:64] ← SRC1[95:64] BITWISE OR SRC2[95:64]
DEST[VLMAX-1:128] (Unmodified)

**VORPS (VEX.128 encoded version)**

DEST[31:0] ← SRC1[31:0] BITWISE OR SRC2[31:0]
DEST[95:64] ← SRC1[95:64] BITWISE OR SRC2[95:64]
DEST[VLMAX-1:128] ← 0

**VORPS (VEX.256 encoded version)**

DEST[31:0] ← SRC1[31:0] BITWISE OR SRC2[31:0]
DEST[95:64] ← SRC1[95:64] BITWISE OR SRC2[95:64]

**Intel C/C++ Compiler Intrinsic Equivalent**

ORPS:  __m128 _mm_or_ps (__m128 a, __m128 b);
VORPS:  __m256 _mm256_or_ps (__m256 a, __m256 b);

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4.
OUT—Output to Port

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Copies the value from the second operand (source operand) to the I/O port specified with the destination operand (first operand). The source operand can be register AL, AX, or EAX, depending on the size of the port being accessed (8, 16, or 32 bits, respectively); the destination operand can be a byte-immediate or the DX register. Using a byte immediate allows I/O port addresses 0 to 255 to be accessed; using the DX register as a source operand allows I/O ports from 0 to 65,535 to be accessed.

The size of the I/O port being accessed is determined by the opcode for an 8-bit I/O port or by the operand-size attribute of the instruction for a 16- or 32-bit I/O port.

At the machine code level, I/O instructions are shorter when accessing 8-bit I/O ports. Here, the upper eight bits of the port address will be 0.

This instruction is only useful for accessing I/O ports located in the processor’s I/O address space. See Chapter 13, “Input/Output,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information on accessing I/O ports in the I/O address space.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

After executing an OUT instruction, the Pentium® processor ensures that the EWBE# pin has been sampled active before it begins to execute the next instruction. (Note that the instruction can be prefetched if EWBE# is not active, but it will not be executed until the EWBE# pin is sampled active.) Only the Pentium processor family has the EWBE# pin.

**Operation**

\[
\text{IF } ((\text{PE} = 1) \land ((\text{CPL} > \text{IOPL}) \lor (\text{VM} = 1))) \\
\text{THEN } (* \text{ Protected mode with CPL > IOPL or virtual-8086 mode } *) \\
\text{IF } (\text{Any I/O Permission Bit for I/O port being accessed } = 1) \\
\text{THEN } (* \text{ I/O operation is not allowed } *) \\
\#\text{GP}(0); \\
\text{ELSE } (* \text{ I/O operation is allowed } *) \\
\text{DEST } \leftarrow \text{SRC}; (* \text{ Writes to selected I/O port } *) \\
\text{FI}; \\
\text{ELSE (Real Mode or Protected Mode with CPL } \leq \text{ IOPL } *) \\
\text{DEST } \leftarrow \text{SRC}; (* \text{ Writes to selected I/O port } *) \\
\text{FI};
\]

**Flags Affected**

None.

**Protected Mode Exceptions**

\#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.

\#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

\#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

\#GP(0) If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.

\#PF(fault-code) If a page fault occurs.

\#UD If the LOCK prefix is used.
**Compatibility Mode Exceptions**  
Same as protected mode exceptions.

**64-Bit Mode Exceptions**  
Same as protected mode exceptions.
OUTS/OUTSB/OUTSW/OUTSD—Output String to Port

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6E</td>
<td>OUTS DX, m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output byte from memory location specified in DS:(E)SI or RSI to I/O port specified in DX**.</td>
</tr>
<tr>
<td>6F</td>
<td>OUTS DX, m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output word from memory location specified in DS:(E)SI or RSI to I/O port specified in DX**.</td>
</tr>
<tr>
<td>6F</td>
<td>OUTS DX, m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output doubleword from memory location specified in DS:(E)SI or RSI to I/O port specified in DX**.</td>
</tr>
<tr>
<td>6E</td>
<td>OUTSB</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output byte from memory location specified in DS:(E)SI or RSI to I/O port specified in DX**.</td>
</tr>
<tr>
<td>6F</td>
<td>OUTSW</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output word from memory location specified in DS:(E)SI or RSI to I/O port specified in DX**.</td>
</tr>
<tr>
<td>6F</td>
<td>OUTSD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output doubleword from memory location specified in DS:(E)SI or RSI to I/O port specified in DX**.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.
** In 64-bit mode, only 64-bit (RSI) and 32-bit (ESI) address sizes are supported. In non-64-bit mode, only 32-bit (ESI) and 16-bit (SI) address sizes are supported.

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Copies data from the source operand (second operand) to the I/O port specified with the destination operand (first operand). The source operand is a memory location, the address of which is read from either the DS:SI, DS:ESI or the RSI registers (depending on the address-size attribute of the instruction, 16, 32 or 64, respec-
OUTS/OUTSB/OUTSW/OUTSD—Output String to Port

At the assembly-code level, two forms of this instruction are allowed: the “explicit-operands” form and the “no-operands” form. The explicit-operands form (specified with the OUTS mnemonic) allows the source and destination operands to be specified explicitly. Here, the source operand should be a symbol that indicates the size of the I/O port and the source address, and the destination operand must be DX. This explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the source operand symbol must specify the correct type (size) of the operand (byte, word, or doubleword), but it does not have to specify the correct location. The location is always specified by the DS:(E)SI or RSI registers, which must be loaded correctly before the OUTS instruction is executed.

The no-operands form provides "short forms" of the byte, word, and doubleword versions of the OUTS instructions. Here also DS:(E)SI is assumed to be the source operand and DX is assumed to be the destination operand. The size of the I/O port is specified with the choice of mnemonic: OUTSB (byte), OUTSW (word), or OUTSD (doubleword).

After the byte, word, or doubleword is transferred from the memory location to the I/O port, the SI/ESI/RSI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the (E)SI register is incremented; if the DF flag is 1, the SI/ESI/RSI register is decremented.) The SI/ESI/RSI register is incremented or decremented by 1 for byte operations, by 2 for word operations, and by 4 for doubleword operations.

The OUTS, OUTSB, OUTSW, and OUTSD instructions can be preceded by the REP prefix for block input of ECX bytes, words, or doublewords. See “REP/REPE/REPZ /REPNE/REPNZ—Repeat String Operation Prefix” in this chapter for a description of the REP prefix. This instruction is only useful for accessing I/O ports located in the processor’s I/O address space. See Chapter 13, “Input/Output,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information on accessing I/O ports in the I/O address space.

In 64-bit mode, the default operand size is 32 bits; operand size is not promoted by the use of REX.W. In 64-bit mode, the default address size is 64 bits, and 64-bit address is specified using RSI by default. 32-bit address using ESI is support using the prefix 67H, but 16-bit address is not supported in 64-bit mode.

IA-32 Architecture Compatibility

After executing an OUTS, OUTSB, OUTSW, or OUTSD instruction, the Pentium processor ensures that the EWBE# pin has been sampled active before it begins to execute the next instruction. (Note that the instruction can be prefetched if EWBE#
is not active, but it will not be executed until the EWBE# pin is sampled active.) Only the Pentium processor family has the EWBE# pin.

For the Pentium 4, Intel® Xeon®, and P6 processor family, upon execution of an OUTS, OUTSB, OUTSW, or OUTSD instruction, the processor will not execute the next instruction until the data phase of the transaction is complete.

**Operation**

```
IF ((PE = 1) and ((CPL > IOPL) or (VM = 1)))
    THEN (* Protected mode with CPL > IOPL or virtual-8086 mode *)
        IF (Any I/O Permission Bit for I/O port being accessed = 1)
            THEN (* I/O operation is not allowed *)
                #GP(0);
            ELSE (* I/O operation is allowed *)
                DEST ← SRC; (* Writes to I/O port *)
        FI;
    ELSE (Real Mode or Protected Mode or 64-Bit Mode with CPL ≤ IOPL *)
        DEST ← SRC; (* Writes to I/O port *)
    FI;

Byte transfer:
    IF 64-bit mode
        Then
            IF 64-Bit Address Size
                THEN
                    IF DF = 0
                        THEN RSI ← RSI RSI + 1;
                        ELSE RSI ← RSI or – 1;
                    FI;
                    ELSE (* 32-Bit Address Size *)
                        IF DF = 0
                            THEN ESI ← ESI + 1;
                            ELSE ESI ← ESI – 1;
                        FI;
                FI;
            ELSE
                IF DF = 0
                    THEN (E)SI ← (E)SI + 1;
                    ELSE (E)SI ← (E)SI – 1;
                FI;
        FI;

Word transfer:
    IF 64-bit mode
        Then
```
OUTS/OUTSB/OUTSW/OUTSD—Output String to Port

IF 64-Bit Address Size
THEN
  IF DF = 0
    THEN RSI ← RSI RSI + 2;
    ELSE RSI ← RSI or − 2;
  FI;
ELSE (* 32-Bit Address Size *)
  IF DF = 0
    THEN ESI ← ESI + 2;
    ELSE ESI ← ESI − 2;
  FI;
FI;
ELSE
  IF DF = 0
    THEN (E)SI ← (E)SI + 2;
    ELSE (E)SI ← (E)SI − 2;
  FI;
FI;

Doubleword transfer:
IF 64-bit mode
Then
  IF 64-Bit Address Size
  THEN
    IF DF = 0
      THEN RSI ← RSI RSI + 4;
      ELSE RSI ← RSI or − 4;
    FI;
  ELSE (* 32-Bit Address Size *)
    IF DF = 0
      THEN ESI ← ESI + 4;
      ELSE ESI ← ESI − 4;
    FI;
  FI;
ELSE
  IF DF = 0
    THEN (E)SI ← (E)SI + 4;
    ELSE (E)SI ← (E)SI − 4;
  FI;
FI;

Flags Affected
None.
Protected Mode Exceptions

#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.
   If a memory operand effective address is outside the limit of the CS, DS, ES, FS, or GS segment.
   If the segment register contains a NULL segment selector.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same as for protected mode exceptions.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1.
   If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  
If the LOCK prefix is used.
## PABSB/PABSW/PABSD — Packed Absolute Value

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 1C /r¹</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Compute the absolute value of bytes in mm2/m64 and store UNSIGNED result in mm1.</td>
</tr>
<tr>
<td>PABSB mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 38 1C /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Compute the absolute value of bytes in xmm2/m128 and store UNSIGNED result in xmm1.</td>
</tr>
<tr>
<td>PABSB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 38 1D /r¹</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Compute the absolute value of 16-bit integers in mm2/m64 and store UNSIGNED result in mm1.</td>
</tr>
<tr>
<td>PABSW mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 38 1D /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Compute the absolute value of 16-bit integers in xmm2/m128 and store UNSIGNED result in xmm1.</td>
</tr>
<tr>
<td>PABSW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 38 1E /r¹</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Compute the absolute value of 32-bit integers in mm2/m64 and store UNSIGNED result in mm1.</td>
</tr>
<tr>
<td>PABSD mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 38 1E /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Compute the absolute value of 32-bit integers in xmm2/m128 and store UNSIGNED result in xmm1.</td>
</tr>
<tr>
<td>PABSD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 1C /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compute the absolute value of bytes in xmm2/m128 and store UNSIGNED result in xmm1.</td>
</tr>
<tr>
<td>VPABSB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 1D /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compute the absolute value of 16-bit integers in xmm2/m128 and store UNSIGNED result in xmm1.</td>
</tr>
<tr>
<td>VPABSW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**PABSB/PABSW/PABSD — Packed Absolute Value**

**Description**

PABSB/W/D computes the absolute value of each data element of the source operand (the second operand) and stores the UNSIGNED results in the destination operand (the first operand). PABSB operates on signed bytes, PABSW operates on 16-bit words, and PABSD operates on signed 32-bit integers. The source operand can be an MMX register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX or an XMM register. Both operands can be MMX register or XMM registers. When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0; otherwise instructions will #UD.

**Operation**

**PABSB (with 64 bit operands)**

- **Unsigned DEST[7:0] ← ABS(SRC[7:0])**
- Repeat operation for 2nd through 7th bytes
- **Unsigned DEST[63:56] ← ABS(SRC[63:56])**

**PABSB (with 128 bit operands)**

- **Unsigned DEST[7:0] ← ABS(SRC[7:0])**
- Repeat operation for 2nd through 15th bytes
UNSIGNED DEST[127:120] ← ABS(SRC[127:120])

PABSw (with 64 bit operands)
UNSIGNED DEST[15:0] ← ABS(SRC[15:0])
Repeat operation for 2nd through 3rd 16-bit words
UNSIGNED DEST[63:48] ← ABS(SRC[63:48])

PABSw (with 128 bit operands)
UNSIGNED DEST[15:0] ← ABS(SRC[15:0])
Repeat operation for 2nd through 7th 16-bit words
UNSIGNED DEST[127:112] ← ABS(SRC[127:112])

PABSD (with 64 bit operands)
UNSIGNED DEST[31:0] ← ABS(SRC[31:0])
UNSIGNED DEST[63:32] ← ABS(SRC[63:32])

PABSD (with 128 bit operands)
UNSIGNED DEST[31:0] ← ABS(SRC[31:0])
Repeat operation for 2nd through 3rd 32-bit double words
UNSIGNED DEST[127:96] ← ABS(SRC[127:96])

PABSB (128-bit Legacy SSE version)
DEST[127:0] ← BYTE_ABS(SRC)
DEST[VLMAX-1:128] (Unmodified)

VPABSB (VEX.128 encoded version)
DEST[127:0] ← BYTE_ABS(SRC)
DEST[VLMAX-1:128] ← 0

PABSw (128-bit Legacy SSE version)
DEST[127:0] ← WORD_ABS(SRC)
DEST[VLMAX-1:128] (Unmodified)

VPABSw (VEX.128 encoded version)
DEST[127:0] ← WORD_ABS(SRC)
DEST[VLMAX-1:128] ← 0

PABSD (128-bit Legacy SSE version)
DEST[127:0] ← DWORD_ABS(SRC)
DEST[VLMAX-1:128] (Unmodified)

VPABSD (VEX.128 encoded version)
DEST[127:0] ← DWORD_ABS(SRC)
DEST[VLMAX-1:128] ← 0
Intel C/C++ Compiler Intrinsic Equivalents

PABSB: __m64 _mm_abs_pi8 (__m64 a)
PABSB: __m128i _mm_abs_epi8 (__m128i a)
PABSW: __m64 _mm_abs_pi16 (__m64 a)
PABSW: __m128i _mm_abs_epi16 (__m128i a)
PABSD: __m64 _mm_abs_pi32 (__m64 a)
PABSD: __m128i _mm_abs_epi32 (__m128i a)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally

#UD If VEX.L = 1.
    If VEX.vvvv != 1111B.
## PACKSSwB/PACKSSdW—Pack with Signed Saturation

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
</table>
| **0F 63 /r**  
PACKSSwB mm1, mm2/m64 | RM V/V | MMX | Converts 4 packed signed word integers from mm1 and from mm2/m64 into 8 packed signed byte integers in mm1 using signed saturation. |
| **66 0F 63 /r**  
PACKSSwB xmm1, xmm2/m128 | RM V/V | SSE2 | Converts 8 packed signed word integers from xmm1 and from xmm2/m128 into 16 packed signed byte integers in xmm1 using signed saturation. |
| **0F 6B /r**  
PACKSSdW mm1, mm2/m64 | RM V/V | MMX | Converts 2 packed signed doubleword integers from mm1 and from mm2/m64 into 4 packed signed word integers in mm1 using signed saturation. |
| **66 0F 6B /r**  
PACKSSdW xmm1, xmm2/m128 | RM V/V | SSE2 | Converts 4 packed signed doubleword integers from xmm1 and from xmm2/m128 into 8 packed signed word integers in xmm1 using signed saturation. |
| **VEX.NDS.128.66.0F.WIG 63 /r**  
VPACKSSwB xmm1,xmm2, xmm3/m128 | RVM V/V | AVX | Converts 8 packed signed word integers from xmm2 and from xmm3/m128 into 16 packed signed byte integers in xmm1 using signed saturation. |
INSTRUCTION SET REFERENCE, M-Z

VEX.NDS.128.66.0F.WIG 6B /r
VPACKSSDW xmm1,xmm2, xmm3/m128

RVM V/V AVX

Converts 4 packed signed doubleword integers from xmm2 and from xmm3/m128 into 8 packed signed word integers in xmm1 using signed saturation.

NOTES:

Instruction Operand Encoding

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<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (w)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Converts packed signed word integers into packed signed byte integers (PACKSSWB) or converts packed signed doubleword integers into packed signed word integers (PACKSSDW), using saturation to handle overflow conditions. See Figure 4-5 for an example of the packing operation.

![Figure 4-5. Operation of the PACKSSDW Instruction Using 64-bit Operands](image)

The PACKSSWB instruction converts 4 or 8 signed word integers from the destination operand (first operand) and 4 or 8 signed word integers from the source operand (second operand) into 8 or 16 signed byte integers and stores the result in the destination operand. If a signed word integer value is beyond the range of a signed byte integer (that is, greater than 7FH for a positive integer or greater than 80H for a negative integer), the saturated signed byte integer value of 7FH or 80H, respectively, is stored in the destination.
The PACKSSDW instruction packs 2 or 4 signed doublewords from the destination operand (first operand) and 2 or 4 signed doublewords from the source operand (second operand) into 4 or 8 signed words in the destination operand (see Figure 4-5). If a signed doubleword integer value is beyond the range of a signed word (that is, greater than 7FFFH for a positive integer or greater than 8000H for a negative integer), the saturated signed word integer value of 7FFFH or 8000H, respectively, is stored into the destination.

The PACKSSWB and PACKSSDW instructions operate on either 64-bit or 128-bit operands. When operating on 64-bit operands, the destination operand must be an MMX technology register and the source operand can be either an MMX technology register or a 64-bit memory location. When operating on 128-bit operands, the destination operand must be an XMM register and the source operand can be either an XMM register or a 128-bit memory location.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PACKSSWB (with 64-bit operands)**

- \( \text{DEST}[7:0] \leftarrow \text{SaturateSignedWordToSignedByte} \text{DEST}[15:0] \)
- \( \text{DEST}[15:8] \leftarrow \text{SaturateSignedWordToSignedByte} \text{DEST}[31:16] \)
- \( \text{DEST}[23:16] \leftarrow \text{SaturateSignedWordToSignedByte} \text{DEST}[47:32] \)
- \( \text{DEST}[31:24] \leftarrow \text{SaturateSignedWordToSignedByte} \text{DEST}[63:48] \)
- \( \text{DEST}[39:32] \leftarrow \text{SaturateSignedWordToSignedByte} \text{SRC}[15:0] \)
- \( \text{DEST}[47:40] \leftarrow \text{SaturateSignedWordToSignedByte} \text{SRC}[31:16] \)
- \( \text{DEST}[55:48] \leftarrow \text{SaturateSignedWordToSignedByte} \text{SRC}[47:32] \)
- \( \text{DEST}[63:56] \leftarrow \text{SaturateSignedWordToSignedByte} \text{SRC}[63:48] \)

**PACKSSDW (with 64-bit operands)**

- \( \text{DEST}[15:0] \leftarrow \text{SaturateSignedDoublewordToSignedWord} \text{DEST}[31:0] \)
- \( \text{DEST}[31:16] \leftarrow \text{SaturateSignedDoublewordToSignedWord} \text{DEST}[63:32] \)
- \( \text{DEST}[47:32] \leftarrow \text{SaturateSignedDoublewordToSignedWord} \text{SRC}[31:0] \)
- \( \text{DEST}[63:48] \leftarrow \text{SaturateSignedDoublewordToSignedWord} \text{SRC}[63:32] \)

**PACKSSWB (with 128-bit operands)**

- \( \text{DEST}[7:0] \leftarrow \text{SaturateSignedWordToSignedByte} (\text{DEST}[15:0]) \)
- \( \text{DEST}[15:8] \leftarrow \text{SaturateSignedWordToSignedByte} (\text{DEST}[31:16]) \)
- \( \text{DEST}[23:16] \leftarrow \text{SaturateSignedWordToSignedByte} (\text{DEST}[47:32]) \)
- \( \text{DEST}[31:24] \leftarrow \text{SaturateSignedWordToSignedByte} (\text{DEST}[63:48]) \)
- \( \text{DEST}[39:32] \leftarrow \text{SaturateSignedWordToSignedByte} (\text{DEST}[79:64]) \)
INSTRUCTION SET REFERENCE, M-Z

PACKSSWB/PACKSSDW—Pack with Signed Saturation

DEST[47:40] ← SaturateSignedWordToSignedByte (DEST[95:80]);
DEST[63:56] ← SaturateSignedWordToSignedByte (DEST[127:112]);
DEST[71:64] ← SaturateSignedWordToSignedByte (SRC[15:0]);
DEST[79:72] ← SaturateSignedWordToSignedByte (SRC[31:16]);
DEST[87:80] ← SaturateSignedWordToSignedByte (SRC[47:32]);
DEST[103:96] ← SaturateSignedWordToSignedByte (SRC[79:64]);
DEST[111:104] ← SaturateSignedWordToSignedByte (SRC[95:80]);
DEST[119:112] ← SaturateSignedWordToSignedByte (SRC[111:96]);
DEST[127:120] ← SaturateSignedWordToSignedByte (SRC[127:112]);

PACKSSDW (with 128-bit operands)

DEST[15:0] ← SaturateSignedDwordToSignedWord (DEST[31:0]);
DEST[31:16] ← SaturateSignedDwordToSignedWord (DEST[63:32]);
DEST[47:32] ← SaturateSignedDwordToSignedWord (DEST[95:64]);
DEST[63:48] ← SaturateSignedDwordToSignedWord (DEST[127:96]);
DEST[79:64] ← SaturateSignedDwordToSignedWord (SRC[31:0]);
DEST[95:80] ← SaturateSignedDwordToSignedWord (SRC[63:32]);
DEST[111:96] ← SaturateSignedDwordToSignedWord (SRC[95:64]);
DEST[127:112] ← SaturateSignedDwordToSignedWord (SRC[127:96]);

PACKSSDW

DEST[127:0] ← SATURATING_PACK_DW(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

VPACKSSDW

DEST[127:0] ← SATURATING_PACK_DW(DEST, SRC)
DEST[VLMAX-1:128] ← 0

PACKSSWB

DEST[127:0] ← SATURATING_PACK_WB(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

VPACKSSWB

DEST[127:0] ← SATURATING_PACK_WB(DEST, SRC)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents

PACKSSWB:  __m64 _mm_packs_pi16(__m64 m1, __m64 m2)
PACKSSWB:  __m128i _mm_packs_epi16(__m128i m1, __m128i m2)
PACKSSDW:  __m64 _mm_packs_pi32 (__m64 m1, __m64 m2)
PACKSSDW:  __m128i _mm_packs_epi32(__m128i m1, __m128i m2)

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD          If VEX.L = 1.
**INSTRUCTION SET REFERENCE, M-Z**

**PACKUSDW — Pack with Unsigned Saturation**

<table>
<thead>
<tr>
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<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 OF 38 2B /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Convert 4 packed signed doubleword integers from xmm1 and 4 packed signed doubleword integers from xmm2/m128 into 8 packed unsigned word integers in xmm1 using unsigned saturation.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 2B /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Convert 4 packed signed doubleword integers from xmm2 and 4 packed signed doubleword integers from xmm3/m128 into 8 packed unsigned word integers in xmm1 using unsigned saturation.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
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<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Converts packed signed doubleword integers into packed unsigned word integers using unsigned saturation to handle overflow conditions. If the signed doubleword value is beyond the range of an unsigned word (that is, greater than FFFFH or less than 0000H), the saturated unsigned word integer value of FFFFH or 0000H, respectively, is stored in the destination.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

\[
\text{TMP}[15:0] \leftarrow (\text{DEST}[31:0] < 0) ? 0 : \text{DEST}[15:0]; \\
\text{DEST}[15:0] \leftarrow (\text{DEST}[31:0] > \text{FFFFH}) ? \text{FFFFH} : \text{TMP}[15:0];
\]
INSTRUCTION SET REFERENCE, M-Z

TMP[47:32] ← (DEST[95:64] < 0) ? 0 : DEST[79:64];
TMP[63:48] ← (DEST[127:96] < 0) ? 0 : DEST[111:96];
TMP[79:64] ← (SRC[31:0] < 0) ? 0 : SRC[15:0];
DEST[79:64] ← (SRC[31:0] > FFFFH) ? FFFFH : TMP[79:64];
TMP[111:96] ← (SRC[95:64] < 0) ? 0 : SRC[79:64];
DEST[111:96] ← (SRC[95:64] > FFFFH) ? FFFFH : TMP[111:96];
TMP[127:112] ← (SRC[127:96] < 0) ? 0 : SRC[111:96];

PACKUSDw (128-bit Legacy SSE version)
DEST[127:0] ← UNSIGNED_SATURATING_PACK_DW(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

VPACKUSDw (VEX.128 encoded version)
DEST[127:0] ← UNSIGNED_SATURATING_PACK_DW(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PACKUSDw: __m128i _mm_packus_epi32(__m128i m1, __m128i m2);

Flags Affected
None.

SIMD Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PACKUSWB—Pack with Unsigned Saturation

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
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<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0F 67 /r ( m )</td>
<td>RM V/V</td>
<td>MMX</td>
<td>Converts 4 signed word integers from ( m ) and 4 signed word integers from ( m/m64 ) into 8 unsigned byte integers in ( m ) using unsigned saturation.</td>
<td></td>
</tr>
<tr>
<td>66 0F 67 /r ( x ), ( x )</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Converts 8 signed word integers from ( x ) and 8 signed word integers from ( x/m64 ) into 16 unsigned byte integers in ( x ) using unsigned saturation.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 67 /r ( x ), ( x ), ( x )</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Converts 8 signed word integers from ( x ) and 8 signed word integers from ( x/m128 ) into 16 unsigned byte integers in ( x ) using unsigned saturation.</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:


Instruction Operand Encoding

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</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Converts 4 or 8 signed word integers from the destination operand (first operand) and 4 or 8 signed word integers from the source operand (second operand) into 8 or 16 unsigned byte integers and stores the result in the destination operand. (See Figure 4-5 for an example of the packing operation.) If a signed word integer value is beyond the range of an unsigned byte integer (that is, greater than FFH or less than
00H), the saturated unsigned byte integer value of FFH or 00H, respectively, is stored in the destination.

The PACKUSWB instruction operates on either 64-bit or 128-bit operands. When operating on 64-bit operands, the destination operand must be an MMX technology register and the source operand can be either an MMX technology register or a 64-bit memory location. When operating on 128-bit operands, the destination operand must be an XMM register and the source operand can be either an XMM register or a 128-bit memory location.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

Operation

**PACKUSWB (with 64-bit operands)**

- \( \text{DEST}[7:0] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[15:0]; \)
- \( \text{DEST}[15:8] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[31:16]; \)
- \( \text{DEST}[23:16] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[47:32]; \)
- \( \text{DEST}[31:24] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[63:48]; \)
- \( \text{DEST}[39:32] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[15:0]; \)
- \( \text{DEST}[47:40] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[31:16]; \)
- \( \text{DEST}[55:48] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[47:32]; \)
- \( \text{DEST}[63:56] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[63:48]; \)

**PACKUSWB (with 128-bit operands)**

- \( \text{DEST}[7:0] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[15:0]; \)
- \( \text{DEST}[15:8] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[31:16]; \)
- \( \text{DEST}[23:16] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[47:32]; \)
- \( \text{DEST}[31:24] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[63:48]; \)
- \( \text{DEST}[39:32] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[79:64]; \)
- \( \text{DEST}[47:40] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[95:80]; \)
- \( \text{DEST}[55:48] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[111:96]; \)
- \( \text{DEST}[63:56] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}[127:112]; \)
- \( \text{DEST}[71:64] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[15:0]; \)
- \( \text{DEST}[79:72] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[31:16]; \)
- \( \text{DEST}[87:80] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[47:32]; \)
- \( \text{DEST}[95:88] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[63:48]; \)
- \( \text{DEST}[103:96] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[79:64]; \)
- \( \text{DEST}[111:104] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[95:80]; \)
- \( \text{DEST}[119:112] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[111:96]; \)
- \( \text{DEST}[127:120] \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}[127:112]; \)

**PACKUSWB (128-bit Legacy SSE version)**

- \( \text{DEST}[127:0] \leftarrow \text{UNSIGNED_SATURATING_PACK_WB} \text{DEST, SRC} \)
- \( \text{DEST}[\text{VLMAX}-1:128] \text{(Unmodified)} \)
**VPACKUSWB (VEX.128 encoded version)**

DEST[127:0] ← UNSIGNED_SATURATING_PACK_WB(SRC1, SRC2)

DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

PACKUSWB: __m64 _mm_packs_pu16(__m64 m1, __m64 m2)

PACKUSWB: __m128i _mm_packus_epi16(__m128i m1, __m128i m2)

**Flags Affected**

None.

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.L = 1.
INSTRUCTION SET REFERENCE, M-Z

PADDB/PADDW/PADDD—Add Packed Integers

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F FC /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Add packed byte integers from mm/m64 and mm.</td>
</tr>
<tr>
<td>PADDB mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F FC /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed byte integers from xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>PADDB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F FD /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Add packed word integers from mm/m64 and mm.</td>
</tr>
<tr>
<td>PADDW mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F FD /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed word integers from xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>PADDW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F FE /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Add packed doubleword integers from mm/m64 and mm.</td>
</tr>
<tr>
<td>PADDD mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F FE /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed doubleword integers from xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>PADDD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG FC /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed byte integers from xmm3/m128 and xmm2.</td>
</tr>
<tr>
<td>VPADDB xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG FD /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed word integers from xmm3/m128 and xmm2.</td>
</tr>
<tr>
<td>VPADDW xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG FE /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed doubleword integers from xmm3/m128 and xmm2.</td>
</tr>
<tr>
<td>VPADDD xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

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PADDB/PADDW/PADDD—Add Packed Integers
Description
Performs a SIMD add of the packed integers from the source operand (second operand) and the destination operand (first operand), and stores the packed integer results in the destination operand. See Figure 9-4 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for an illustration of a SIMD operation. Overflow is handled with wraparound, as described in the following paragraphs.
These instructions can operate on either 64-bit or 128-bit operands. When operating on 64-bit operands, the destination operand must be an MMX technology register and the source operand can be either an MMX technology register or a 64-bit memory location. When operating on 128-bit operands, the destination operand must be an XMM register and the source operand can be either an XMM register or a 128-bit memory location.
Adds the packed byte, word, doubleword, or quadword integers in the first source operand to the second source operand and stores the result in the destination operand. When a result is too large to be represented in the 8/16/32 integer (overflow), the result is wrapped around and the low bits are written to the destination element (that is, the carry is ignored).
Note that these instructions can operate on either unsigned or signed (two’s complement notation) integers; however, it does not set bits in the EFLAGS register to indicate overflow and/or a carry. To prevent undetected overflow conditions, software must control the ranges of the values operated on.
In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.
VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation
**PADDB** (with 64-bit operands)

\[
\text{DEST}[7:0] \leftarrow \text{DEST}[7:0] + \text{SRC}[7:0];
\]
(* Repeat add operation for 2nd through 7th byte *)
\[
\text{DEST}[63:56] \leftarrow \text{DEST}[63:56] + \text{SRC}[63:56];
\]

**PADDW** (with 64-bit operands)

\[
\text{DEST}[15:0] \leftarrow \text{DEST}[15:0] + \text{SRC}[15:0];
\]
(* Repeat add operation for 2nd and 3th word *)
\[
\text{DEST}[63:48] \leftarrow \text{DEST}[63:48] + \text{SRC}[63:48];
\]
PADDW (with 128-bit operands)
DEST[15:0] ← DEST[15:0] + SRC[15:0];
(* Repeat add operation for 2nd through 7th word *)

PADD (with 64-bit operands)
DEST[31:0] ← DEST[31:0] + SRC[31:0];

PADD (with 128-bit operands)
DEST[31:0] ← DEST[31:0] + SRC[31:0];
(* Repeat add operation for 2nd and 3th doubleword *)

VPADDB (VEX.128 encoded version)
DEST[7:0] ← SRC1[7:0]+SRC2[7:0]
DEST[47:40] ← SRC1[47:40]+SRC2[47:40]
DEST[63:56] ← SRC1[63:56]+SRC2[63:56]
DEST[71:64] ← SRC1[71:64]+SRC2[71:64]
DEST[87:80] ← SRC1[87:80]+SRC2[87:80]
DEST[VLMAX-1:128] ← 0

VPADDW (VEX.128 encoded version)
DEST[15:0] ← SRC1[15:0]+SRC2[15:0]
DEST[79:64] ← SRC1[79:64]+SRC2[79:64]
DEST[VLMAX-1:128] ← 0
VPADDD (VEX.128 encoded version)
DEST[31:0] ← SRC1[31:0]+SRC2[31:0]
DEST[95:64] ← SRC1[95:64]+SRC2[95:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PADDB:  __m64 _mm_add_pi8(__m64 m1, __m64 m2)
PADDB:  __m128i _mm_add_epi8 (__m128ia,__m128ib)
PADDW:  __m64 _mm_add_pi16(__m64 m1, __m64 m2)
PADDW:  __m128i _mm_add_epi16 ( __m128i a, __m128i b)
PADDD:  __m64 _mm_add_pi32(__m64 m1, __m64 m2)
PADDD:  __m128i _mm_add_epi32 ( __m128i a, __m128i b)

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PADDQ—Add Packed Quadword Integers

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F D4 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add quadword integer mm2/m64 to mm1.</td>
</tr>
<tr>
<td>PADDQ mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F D4 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed quadword integers xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>PADDQ xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG D4 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed quadword integers xmm3/m128 and xmm2.</td>
</tr>
<tr>
<td>VPADDQ xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**


**Instruction Operand Encoding**

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<tr>
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</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:reg/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:reg/r (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Adds the first operand (destination operand) to the second operand (source operand) and stores the result in the destination operand. The source operand can be a quadword integer stored in an MMX technology register or a 64-bit memory location, or it can be two packed quadword integers stored in an XMM register or an 128-bit memory location. The destination operand can be a quadword integer stored in an MMX technology register or two packed quadword integers stored in an XMM register. When packed quadword operands are used, a SIMD add is performed. When a quadword result is too large to be represented in 64 bits (overflow), the result is wrapped around and the low 64 bits are written to the destination element (that is, the carry is ignored).

Note that the PADDQ instruction can operate on either unsigned or signed (two’s complement notation) integers; however, it does not set bits in the EFLAGS register to indicate overflow and/or a carry. To prevent undetected overflow conditions, software must control the ranges of the values operated on.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.
VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PADDQ (with 64-Bit operands)**
\[
\text{DEST}[63:0] \leftarrow \text{DEST}[63:0] + \text{SRC}[63:0];
\]

**PADDQ (with 128-Bit operands)**
\[
\begin{align*}
\text{DEST}[63:0] & \leftarrow \text{DEST}[63:0] + \text{SRC}[63:0]; \\
\text{DEST}[127:64] & \leftarrow \text{DEST}[127:64] + \text{SRC}[127:64];
\end{align*}
\]

**VPADDQ (VEX.128 encoded version)**
\[
\begin{align*}
\text{DEST}[63:0] & \leftarrow \text{SRC1}[63:0] + \text{SRC2}[63:0] \\
\text{DEST}[127:64] & \leftarrow \text{SRC1}[127:64] + \text{SRC2}[127:64] \\
\text{DEST}[VLMAX-1:128] & \leftarrow 0
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalents**

PADDQ: \[
\text{__m64 } \_\text{mm_add_si64 } (\text{__m64 a, __m64 b})
\]

PADDQ: \[
\text{__m128i } \_\text{mm_add_epi64 } (\text{__m128i a, __m128i b})
\]

**Flags Affected**
None.

**Numeric Exceptions**
None.

**Other Exceptions**
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
### PADDSB/PADDSW—Add Packed Signed Integers with Signed Saturation

<table>
<thead>
<tr>
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<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F EC /r&lt;sup&gt;1&lt;/sup&gt; PADDSB mm, mm/m64</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Add packed signed byte integers from mm/m64 and mm and saturate the results.</td>
</tr>
<tr>
<td>66 0F EC /r PADDSB xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed signed byte integers from xmm2/m128 and xmm1 saturate the results.</td>
</tr>
<tr>
<td>0F ED /r&lt;sup&gt;1&lt;/sup&gt; PADDSW mm, mm/m64</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Add packed signed word integers from mm/m64 and mm and saturate the results.</td>
</tr>
<tr>
<td>66 0F ED /r PADDSW xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed signed word integers from xmm2/m128 and xmm1 saturate the results.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG EC /r VPADDSB xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed signed byte integers from xmm3/m128 and xmm2 saturate the results.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG ED /r VPADDSW xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed signed word integers from xmm3/m128 and xmm2 saturate the results.</td>
</tr>
</tbody>
</table>

**NOTES:**
INSTRUCTION SET REFERENCE, M-Z

PADDSB/PADDSW—Add Packed Signed Integers with Signed Saturation

Description

Performs a SIMD add of the packed signed integers from the source operand (second operand) and the destination operand (first operand), and stores the packed integer results in the destination operand. See Figure 9-4 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a SIMD operation. Overflow is handled with signed saturation, as described in the following paragraphs.

These instructions can operate on either 64-bit or 128-bit operands. When operating on 64-bit operands, the destination operand must be an MMX technology register and the source operand can be either an MMX technology register or a 64-bit memory location. When operating on 128-bit operands, the destination operand must be an XMM register and the source operand can be either an XMM register or a 128-bit memory location.

The PADDSB instruction adds packed signed byte integers. When an individual byte result is beyond the range of a signed byte integer (that is, greater than 7FH or less than 80H), the saturated value of 7FH or 80H, respectively, is written to the destination operand.

The PADDSW instruction adds packed signed word integers. When an individual word result is beyond the range of a signed word integer (that is, greater than 7FFFH or less than 8000H), the saturated value of 7FFFH or 8000H, respectively, is written to the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

PADDSB (with 64-bit operands)

\[
\text{DEST}[7:0] \leftarrow \text{SaturateToSignedByte} (\text{DEST}[7:0] + \text{SRC}[7:0]);
\]

(* Repeat add operation for 2nd through 7th bytes * )

\[
\text{DEST}[63:56] \leftarrow \text{SaturateToSignedByte} (\text{DEST}[63:56] + \text{SRC}[63:56]);
\]

PADDSB (with 128-bit operands)

\[
\text{DEST}[7:0] \leftarrow \text{SaturateToSignedByte} (\text{DEST}[7:0] + \text{SRC}[7:0]);
\]
INSTRUCTION SET REFERENCE, M-Z

(* Repeat add operation for 2nd through 14th bytes *)
DEST[127:120] ← SaturateToSignedByte (DEST[111:120] + SRC[127:120])

VPADDSB
DEST[7:0] ← SaturateToSignedByte (SRC[7:0] + SRC2[7:0])
(* Repeat subtract operation for 2nd through 14th bytes *)
DEST[127:120] ← SaturateToSignedByte (SRC[111:120] + SRC2[127:120])
DEST[VLMAX-1:128] ← 0

PADDSW (with 64-bit operands)
DEST[15:0] ← SaturateToSignedWord(DEST[15:0] + SRC[15:0])
(* Repeat add operation for 2nd and 7th words *)

PADDSW (with 128-bit operands)
DEST[15:0] ← SaturateToSignedWord(DEST[15:0] + SRC[15:0])
(* Repeat add operation for 2nd through 7th words *)

VPADDSW
DEST[15:0] ← SaturateToSignedWord (SRC[15:0] + SRC2[15:0])
(* Repeat subtract operation for 2nd through 7th words *)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PADDSB: __m64 _mm_adds_pi8(__m64 m1, __m64 m2)
PADDSB: __m128i _mm_adds_epi8 ( __m128i a, __m128i b)
PADDSW: __m64 _mm_adds_pi16(__m64 m1, __m64 m2)
PADDSw: __m128i _mm_adds_epi16 ( __m128i a, __m128i b)

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PADDUSB/PADDUSW—Add Packed Unsigned Integers with Unsigned Saturation

<table>
<thead>
<tr>
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<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>0F DC /r¹</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Add packed unsigned byte integers from mm/m64 and mm and saturate the results.</td>
</tr>
<tr>
<td>PADDUSB mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F DC /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed unsigned byte integers from xmm2/m128 and xmm1 saturate the results.</td>
</tr>
<tr>
<td>PADDUSB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F DD /r¹</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Add packed unsigned word integers from mm/m64 and mm and saturate the results.</td>
</tr>
<tr>
<td>PADDUSW mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F DD /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Add packed unsigned word integers from xmm2/m128 to xmm1 and saturate the results.</td>
</tr>
<tr>
<td>PADDUSW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.660F:WIG DC /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed unsigned byte integers from xmm3/m128 to xmm2 and saturate the results.</td>
</tr>
<tr>
<td>VPADDUSB xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F:WIG DD /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add packed unsigned word integers from xmm3/m128 to xmm2 and saturate the results.</td>
</tr>
<tr>
<td>VPADDUSB xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

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<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX:vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>
**Description**

Performs a SIMD add of the packed unsigned integers from the source operand (second operand) and the destination operand (first operand), and stores the packed integer results in the destination operand. See Figure 9-4 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for an illustration of a SIMD operation. Overflow is handled with unsigned saturation, as described in the following paragraphs.

These instructions can operate on either 64-bit or 128-bit operands. When operating on 64-bit operands, the destination operand must be an MMX technology register and the source operand can be either an MMX technology register or a 64-bit memory location. When operating on 128-bit operands, the destination operand must be an XMM register and the source operand can be either an XMM register or a 128-bit memory location.

The PADDUSB instruction adds packed unsigned byte integers. When an individual byte result is beyond the range of an unsigned byte integer (that is, greater than FFH), the saturated value of FFH is written to the destination operand.

The PADDUSW instruction adds packed unsigned word integers. When an individual word result is beyond the range of an unsigned word integer (that is, greater than FFFFH), the saturated value of FFFFH is written to the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PADDUSB (with 64-bit operands)**

- \( \text{DEST}[7:0] \leftarrow \text{SaturateToUnsignedByte}(\text{DEST}[7:0] + \text{SRC}[7:0]) \);  
  (* Repeat add operation for 2nd through 7th bytes *)
- \( \text{DEST}[63:56] \leftarrow \text{SaturateToUnsignedByte}(\text{DEST}[63:56] + \text{SRC}[63:56]) \)

**PADDUSB (with 128-bit operands)**

- \( \text{DEST}[7:0] \leftarrow \text{SaturateToUnsignedByte}(\text{DEST}[7:0] + \text{SRC}[7:0]) \);  
  (* Repeat add operation for 2nd through 14th bytes *)
- \( \text{DEST}[127:120] \leftarrow \text{SaturateToUnsignedByte}(\text{DEST}[127:120] + \text{SRC}[127:120]) \)

**VPADDUSB**

- \( \text{DEST}[7:0] \leftarrow \text{SaturateToUnsignedByte}(\text{SRC1}[7:0] + \text{SRC2}[7:0]) \);  
  (* Repeat subtract operation for 2nd through 14th bytes *)
- \( \text{DEST}[127:120] \leftarrow \text{SaturateToUnsignedByte}(\text{SRC1}[111:120] + \text{SRC2}[127:120]) \)
- \( \text{DEST}[\text{VLMAX}-1:128] \leftarrow 0 \)
PADDUSW (with 64-bit operands)
DEST[15:0] ← SaturateToUnsignedWord(DEST[15:0] + SRC[15:0]);
(* Repeat add operation for 2nd and 3rd words *)

PADDUSw (with 128-bit operands)
DEST[15:0] ← SaturateToUnsignedWord (DEST[15:0] + SRC[15:0]);
(* Repeat add operation for 2nd through 7th words *)

VPADDUSW
DEST[15:0] ← SaturateToUnsignedWord (SRC1[15:0] + SRC2[15:0]);
(* Repeat subtract operation for 2nd through 7th words *)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PADDUSB: __m64 _mm_adds_pu8(__m64 m1, __m64 m2)
PADDUSw: __m64 _mm_adds_pu16(__m64 m1, __m64 m2)
PADDUSB: __m128i _mm_adds_epu8 (__m128i a, __m128i b)
PADDUSw: __m128i _mm_adds_epu16 ( __m128i a, __m128i b)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PALIGNR — Packed Align Right

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 3A 0F</td>
<td>RMI</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Concatenate destination and source operands, extract byte-aligned result shifted to the right by constant value in imm8 into mm1.</td>
</tr>
<tr>
<td>PALIGNR mm1, mm2/m64, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 3A 0F</td>
<td>RMI</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Concatenate destination and source operands, extract byte-aligned result shifted to the right by constant value in imm8 into xmm1.</td>
</tr>
<tr>
<td>PALIGNR xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.WIG 0F /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Concatenate xmm2 and xmm3/m128, extract byte aligned result shifted to the right by constant value in imm8 and result is stored in xmm1.</td>
</tr>
<tr>
<td>VPALIGNR xmm1, xmm2, xmm3/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
<thead>
<tr>
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<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMrm (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMrm (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

PALIGNR concatenates the destination operand (the first operand) and the source operand (the second operand) into an intermediate composite, shifts the composite at byte granularity to the right by a constant immediate, and extracts the right-aligned result into the destination. The first and the second operands can be an MMX or an XMM register. The immediate value is considered unsigned. Immediate shift counts larger than the 2L (i.e. 32 for 128-bit operands, or 16 for 64-bit operands) produce a zero result. Both operands can be MMX register or XMM registers. When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.
In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

**PALIGNR (with 64-bit operands)**

\[
\text{temp1}[127:0] = \text{CONCATENATE(DEST, SRC)} \gg (\text{imm8}\times 8) \\
\text{DEST}[63:0] = \text{temp1}[63:0]
\]

**PALIGNR (with 128-bit operands)**

\[
\text{temp1}[255:0] = \text{CONCATENATE(DEST, SRC)} \gg (\text{imm8}\times 8) \\
\text{DEST}[127:0] = \text{temp1}[127:0]
\]

**VPALIGNR**

\[
\text{temp1}[255:0] \leftarrow \text{CONCATENATE(SRC1, SRC2)} \gg (\text{imm8}\times 8) \\
\text{DEST}[127:0] \leftarrow \text{temp1}[127:0] \\
\text{DEST}[\text{VLMAX-1:128}] \leftarrow 0
\]

**Intel C/C++ Compiler Intrinsic Equivalents**

PALIGNR: \_m64 \_mm_alignr\_pi8 (\_m64 a, \_m64 b, int n)
PALIGNR: \_m128i \_mm_alignr\_epi8 (\_m128i a, \_m128i b, int n)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.L = 1.


**PAND—Logical AND**

<table>
<thead>
<tr>
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<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF DB /r(^1) PAND mm, mm/m64</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Bitwise AND mm/m64 and mm.</td>
</tr>
<tr>
<td>66 OF DB /r PAND xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Bitwise AND of xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG DB /r VPAND xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Bitwise AND of xmm3/m128 and xmm.</td>
</tr>
</tbody>
</table>

**NOTES:**

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**Instruction Operand Encoding**

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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMrm/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMrm/r (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical AND operation on the source operand (second operand) and the destination operand (first operand) and stores the result in the destination operand. The source operand can be an MMX technology register or a 64-bit memory location or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register. Each bit of the result is set to 1 if the corresponding bits of the first and second operands are 1; otherwise, it is set to 0.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PAND (128-bit Legacy SSE version)**
PAND—Logical AND

DEST ← DEST AND SRC
DEST[VLMAX-1:1288] (Unmodified)

VPAND (VEX.128 encoded version)
DEST ← SRC1 AND SRC2
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PAND: __m64 _mm_and_si64 (__m64 m1, __m64 m2)
PAND: __m128i _mm_and_si128 ( __m128i a, __m128i b)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PANDN—Logical AND NOT

Op/En Instruction Opcode/

<table>
<thead>
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<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0F DF /r1 PANDN mm, mm/m64</td>
<td>RM V/V</td>
<td>MMX</td>
<td>Bitwise AND NOT of mm/m64 and mm.</td>
<td></td>
</tr>
<tr>
<td>66 0F DF /r PANDN xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Bitwise AND NOT of xmm2/m128 and xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG DF /r VPANDN xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Bitwise AND NOT of xmm3/m128 and xmm2.</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
Performs a bitwise logical NOT of the destination operand (first operand), then performs a bitwise logical AND of the source operand (second operand) and the inverted destination operand. The result is stored in the destination operand. The source operand can be an MMX technology register or a 64-bit memory location or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register. Each bit of the result is set to 1 if the corresponding bit in the first operand is 0 and the corresponding bit in the second operand is 1; otherwise, it is set to 0.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:1288) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.
**Operation**

**PANDN (128-bit Legacy SSE version)**

\[ \text{DEST} \leftarrow \text{NOT(DEST)} \text{ AND SRC} \]

\[ \text{DEST}[\text{VLMAX}-1:128] \text{ (Unmodified)} \]

**VPANDN (VEX.128 encoded version)**

\[ \text{DEST} \leftarrow \text{NOT(SRC1)} \text{ AND SRC2} \]

\[ \text{DEST}[\text{VLMAX}-1:128] \leftarrow 0 \]

**Intel C/C++ Compiler Intrinsic Equivalent**

PANDN: \_m64 \_mm_andnotsi64 (\_m64 m1, \_m64 m2)

PANDN: \_m128i \_mm_andnotsi128 (\_m128i a, \_m128i b)

**Flags Affected**

None.

**Numeric Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

\#UD \quad \text{If VEX.L = 1.}
PAUSE—Spin Loop Hint

**Description**

Improves the performance of spin-wait loops. When executing a "spin-wait loop," a Pentium 4 or Intel Xeon processor suffers a severe performance penalty when exiting the loop because it detects a possible memory order violation. The PAUSE instruction provides a hint to the processor that the code sequence is a spin-wait loop. The processor uses this hint to avoid the memory order violation in most situations, which greatly improves processor performance. For this reason, it is recommended that a PAUSE instruction be placed in all spin-wait loops.

An additional function of the PAUSE instruction is to reduce the power consumed by a Pentium 4 processor while executing a spin loop. The Pentium 4 processor can execute a spin-wait loop extremely quickly, causing the processor to consume a lot of power while it waits for the resource it is spinning on to become available. Inserting a pause instruction in a spin-wait loop greatly reduces the processor’s power consumption.

This instruction was introduced in the Pentium 4 processors, but is backward compatible with all IA-32 processors. In earlier IA-32 processors, the PAUSE instruction operates like a NOP instruction. The Pentium 4 and Intel Xeon processors implement the PAUSE instruction as a pre-defined delay. The delay is finite and can be zero for some processors. This instruction does not change the architectural state of the processor (that is, it performs essentially a delaying no-op operation).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

Execute_Next Instruction(DELAY);

**Numeric Exceptions**

None.
Exceptions (All Operating Modes)

#UD        If the LOCK prefix is used.
PAVGB/PAVGW—Average Packed Integers

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF E0 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Average packed unsigned byte integers from mm2/m64 and mm1 with rounding.</td>
</tr>
<tr>
<td>PAVGB mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF E0, /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Average packed unsigned byte integers from xmm2/m128 and xmm1 with rounding.</td>
</tr>
<tr>
<td>PAVGB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF E3 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Average packed unsigned word integers from mm2/m64 and mm1 with rounding.</td>
</tr>
<tr>
<td>PAVGW mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF E3 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Average packed unsigned word integers from xmm2/m128 and xmm1 with rounding.</td>
</tr>
<tr>
<td>PAVGW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG E0 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Average packed unsigned byte integers from xmm3/m128 and xmm2 with rounding.</td>
</tr>
<tr>
<td>VPAVGB xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG E3 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Average packed unsigned word integers from xmm3/m128 and xmm2 with rounding.</td>
</tr>
<tr>
<td>VPAVGW xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
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<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
Performs a SIMD average of the packed unsigned integers from the source operand.
(second operand) and the destination operand (first operand), and stores the results in the destination operand. For each corresponding pair of data elements in the first and second operands, the elements are added together, a 1 is added to the temporary sum, and that result is shifted right one bit position. The source operand can be an MMX technology register or a 64-bit memory location or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

The PAVGB instruction operates on packed unsigned bytes and the PAVGW instruction operates on packed unsigned words.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PAVGB (with 64-bit operands)**

\[
\text{DEST}[7:0] \leftarrow (\text{SRC}[7:0] + \text{DEST}[7:0] + 1) >> 1; \quad (\text{Temp sum before shifting is 9 bits})
\]

(*) Repeat operation performed for bytes 2 through 6 *)

\[
\text{DEST}[63:56] \leftarrow (\text{SRC}[63:56] + \text{DEST}[63:56] + 1) >> 1;
\]

**PAVGW (with 64-bit operands)**

\[
\text{DEST}[15:0] \leftarrow (\text{SRC}[15:0] + \text{DEST}[15:0] + 1) >> 1; \quad (\text{Temp sum before shifting is 17 bits})
\]

(*) Repeat operation performed for words 2 and 3 *)

\[
\text{DEST}[63:48] \leftarrow (\text{SRC}[63:48] + \text{DEST}[63:48] + 1) >> 1;
\]

**PAVGB (with 128-bit operands)**

\[
\text{DEST}[7:0] \leftarrow (\text{SRC}[7:0] + \text{DEST}[7:0] + 1) >> 1; \quad (\text{Temp sum before shifting is 9 bits})
\]

(*) Repeat operation performed for bytes 2 through 14 *)

\[
\text{DEST}[127:120] \leftarrow (\text{SRC}[127:120] + \text{DEST}[127:120] + 1) >> 1;
\]

**PAVGW (with 128-bit operands)**

\[
\text{DEST}[15:0] \leftarrow (\text{SRC}[15:0] + \text{DEST}[15:0] + 1) >> 1; \quad (\text{Temp sum before shifting is 17 bits})
\]

(*) Repeat operation performed for words 2 through 6 *)

\[
\text{DEST}[127:112] \leftarrow (\text{SRC}[127:112] + \text{DEST}[127:112] + 1) >> 1;
\]

**VPAVGB (VEX.128 encoded version)**

\[
\text{DEST}[7:0] \leftarrow (\text{SRC1}[7:0] + \text{SRC2}[7:0] + 1) >> 1;
\]

(*) Repeat operation performed for bytes 2 through 15 *)

\[
\text{DEST}[127:120] \leftarrow (\text{SRC1}[127:120] + \text{SRC2}[127:120] + 1) >> 1
\]

\[
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0
\]
VPAVGW (VEX.128 encoded version)
DEST[15:0] ← (SRC1[15:0] + SRC2[15:0] + 1) >> 1;
(* Repeat operation performed for 16-bit words 2 through 7 *)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PAVGB:  __m64 _mm_avg_pu8 (__m64 a, __m64 b)
PAVGw:  __m64 _mm_avg_pu16 (__m64 a, __m64 b)
PAVGB:  __m128i _mm_avg_epu8 ( __m128i a, __m128i b)
PAVGw:  __m128i _mm_avg_epu16 ( __m128i a, __m128i b)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD             If VEX.L = 1.
PBLENDVB — Variable Blend Packed Bytes

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 10 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Select byte values from xmm1 and xmm2/m128 from mask specified in the high bit of each byte in XMM0 and store the values into xmm1.</td>
</tr>
<tr>
<td>PBLENDVB xmm1, xmm2/m128, &lt;XMM0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.W0 4C /r /is4</td>
<td>RVMR</td>
<td>V/V</td>
<td>AVX</td>
<td>Select byte values from xmm2 and xmm3/m128 using mask bits in the specified mask register, xmm4, and store the values into xmm1.</td>
</tr>
<tr>
<td>VPBLENDVB xmm1, xmm2, xmm3/m128, xmm4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>&lt;XMM0&gt;</td>
<td>NA</td>
</tr>
<tr>
<td>RVMR</td>
<td>ModRM:reg (w)</td>
<td>VEX:vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>ModRM:reg (r)</td>
</tr>
</tbody>
</table>

**Description**

Conditionally copies byte elements from the source operand (second operand) to the destination operand (first operand) depending on mask bits defined in the implicit third register argument, XMM0. The mask bits are the most significant bit in each byte element of the XMM0 register.

If a mask bit is "1", then the corresponding byte element in the source operand is copied to the destination, else the byte element in the destination operand is left unchanged.

The register assignment of the implicit third operand is defined to be the architectural register XMM0.

128-bit Legacy SSE version: The first source operand and the destination operand is the same. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged. The mask register operand is implicitly defined to be the architectural register XMM0. An attempt to execute PBLENDVB with a VEX prefix will cause #UD.

VEX.128 encoded version: The first source operand and the destination operand are XMM registers. The second source operand is an XMM register or 128-bit memory location. The mask operand is the third source register, and encoded in bits[7:4] of the immediate byte (imm8). The bits[3:0] of imm8 are ignored. In 32-bit mode, imm8[7] is ignored. The upper bits (VLMAX-1:128) of the corresponding YMM
register (destination register) are zeroed. VEX.L must be 0, otherwise the instruction will #UD. VEX.W must be 0, otherwise, the instruction will #UD.

VPBLENDVB permits the mask to be any XMM or YMM register. In contrast, PBLENDVB treats XMM0 implicitly as the mask and do not support non-destructive destination operation. An attempt to execute PBLENDVB encoded with a VEX prefix will cause a #UD exception.

**Operation**

**PBLENDVB (128-bit Legacy SSE version)**

\[
\text{MASK} \leftarrow \text{XMM0} \\
\text{IF (MASK}[7] = 1) \text{ THEN } \text{DEST}[7:0] \leftarrow \text{SRC}[7:0]; \\
\text{ELSE } \text{DEST}[7:0] \leftarrow \text{DEST}[7:0]; \\
\text{IF (MASK}[15] = 1) \text{ THEN } \text{DEST}[15:8] \leftarrow \text{SRC}[15:8]; \\
\text{ELSE } \text{DEST}[15:8] \leftarrow \text{DEST}[15:8]; \\
\text{IF (MASK}[23] = 1) \text{ THEN } \text{DEST}[23:16] \leftarrow \text{SRC}[23:16]; \\
\text{ELSE } \text{DEST}[23:16] \leftarrow \text{DEST}[23:16]; \\
\text{IF (MASK}[31] = 1) \text{ THEN } \text{DEST}[31:24] \leftarrow \text{SRC}[31:24]; \\
\text{ELSE } \text{DEST}[31:24] \leftarrow \text{DEST}[31:24]; \\
\text{IF (MASK}[39] = 1) \text{ THEN } \text{DEST}[39:32] \leftarrow \text{SRC}[39:32]; \\
\text{ELSE } \text{DEST}[39:32] \leftarrow \text{DEST}[39:32]; \\
\text{IF (MASK}[47] = 1) \text{ THEN } \text{DEST}[47:40] \leftarrow \text{SRC}[47:40]; \\
\text{ELSE } \text{DEST}[47:40] \leftarrow \text{DEST}[47:40]; \\
\text{IF (MASK}[55] = 1) \text{ THEN } \text{DEST}[55:48] \leftarrow \text{SRC}[55:48]; \\
\text{ELSE } \text{DEST}[55:48] \leftarrow \text{DEST}[55:48]; \\
\text{IF (MASK}[63] = 1) \text{ THEN } \text{DEST}[63:56] \leftarrow \text{SRC}[63:56]; \\
\text{ELSE } \text{DEST}[63:56] \leftarrow \text{DEST}[63:56]; \\
\text{IF (MASK}[71] = 1) \text{ THEN } \text{DEST}[71:64] \leftarrow \text{SRC}[71:64]; \\
\text{ELSE } \text{DEST}[71:64] \leftarrow \text{DEST}[71:64]; \\
\text{IF (MASK}[79] = 1) \text{ THEN } \text{DEST}[79:72] \leftarrow \text{SRC}[79:72]; \\
\text{ELSE } \text{DEST}[79:72] \leftarrow \text{DEST}[79:72]; \\
\text{IF (MASK}[87] = 1) \text{ THEN } \text{DEST}[87:80] \leftarrow \text{SRC}[87:80]; \\
\text{ELSE } \text{DEST}[87:80] \leftarrow \text{DEST}[87:80]; \\
\text{IF (MASK}[95] = 1) \text{ THEN } \text{DEST}[95:88] \leftarrow \text{SRC}[95:88]; \\
\text{ELSE } \text{DEST}[95:88] \leftarrow \text{DEST}[95:88]; \\
\text{IF (MASK}[103] = 1) \text{ THEN } \text{DEST}[103:96] \leftarrow \text{SRC}[103:96]; \\
\text{ELSE } \text{DEST}[103:96] \leftarrow \text{DEST}[103:96]; \\
\text{IF (MASK}[111] = 1) \text{ THEN } \text{DEST}[111:104] \leftarrow \text{SRC}[111:104]; \\
\text{ELSE } \text{DEST}[111:104] \leftarrow \text{DEST}[111:104]; \\
\text{IF (MASK}[119] = 1) \text{ THEN } \text{DEST}[119:112] \leftarrow \text{SRC}[119:112]; \\
\text{ELSE } \text{DEST}[119:112] \leftarrow \text{DEST}[119:112]; \\
\text{IF (MASK}[127] = 1) \text{ THEN } \text{DEST}[127:120] \leftarrow \text{SRC}[127:120]; \\
\text{ELSE } \text{DEST}[127:120] \leftarrow \text{DEST}[127:120]);
VPBLENDVB (VEX.128 encoded version)

```plaintext
DEST[VLMAX-1:128] (Unmodified)

VPBLENDVB (VEX.128 encoded version)

DEST[VLMAX-1:128] (Unmodified)

VPBLENDVB

```
INSTRUCTION SET REFERENCE, M-Z

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD       If VEX.L = 1.
          If VEX.W = 1.
**PBLENDW — Blend Packed Words**

**Op/En** | **Operand 1** | **Operand 2** | **Operand 3** | **Operand 4**
---|---|---|---|---
RMI | ModRM:reg (r, w) | ModRM:r/m (r) | imm8 | NA
RVMI | ModRM:reg (w) | VEX.vvvv (r) | ModRM:r/m (r) | imm8

**Opcode/Instruction**

| 66 0F 3A 0E /r ib | PBLENDW xmm1, xmm2/m128, imm8 |
| 6F 6.0F3A.WIG 0E /r ib | VPBLENDW xmm1, xmm2, xmm3/m128, imm8 |

**Description**

Conditionally copies word elements from the source operand (second operand) to the destination operand (first operand) depending on the immediate byte (third operand). Each bit of Imm8 correspond to a word element.

If a bit is "1", then the corresponding word element in the source operand is copied to the destination, else the word element in the destination operand is left unchanged.

128-bit Legacy SSE version: Bits (VLMAX-1:1288) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PBLENDW (128-bit Legacy SSE version)**

IF (imm8[0] = 1) THEN DEST[15:0] ← SRC[15:0]
ELSE DEST[15:0] ← DEST[15:0]
ELSE DEST[31:16] ← DEST[31:16]
ELSE DEST[63:48] ← DEST[63:48]
ELSE DEST[79:64] ← DEST[79:64]
ELSE DEST[95:80] ← DEST[95:80]
ELSE DEST[111:96] ← DEST[111:96]
ELSE DEST[127:112] ← DEST[127:112]

VPBLENDW (VEX.128 encoded version)
IF (imm8[0] = 1) THEN DEST[15:0] ← SRC2[15:0]
ELSE DEST[15:0] ← SRC1[15:0]
ELSE DEST[31:16] ← SRC1[31:16]
ELSE DEST[63:48] ← SRC1[63:48]
ELSE DEST[79:64] ← SRC1[79:64]
ELSE DEST[95:80] ← SRC1[95:80]
ELSE DEST[111:96] ← SRC1[111:96]
ELSE DEST[127:112] ← SRC1[127:112]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PBLENDW: __m128i _mm_blend_epi16 (__m128i v1, __m128i v2, const int mask);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PCLMULQDQ - Carry-Less Multiplication Quadword

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 44 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>CLMUL</td>
<td>Carry-less multiplication of one quadword of xmm1 by one quadword of xmm2/m128, stores the 128-bit result in xmm1. The immediate is used to determine which quadwords of xmm1 and xmm2/m128 should be used.</td>
</tr>
<tr>
<td>PCLMULQDQ xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.WIG 44 /r ib VPCLMULQDQ xmm1, xmm2, xmm3/m128, imm8</td>
<td>RVI</td>
<td>V/V</td>
<td>Both CLMUL and AVX flags</td>
<td>Carry-less multiplication of one quadword of xmm2 by one quadword of xmm3/m128, stores the 128-bit result in xmm1. The immediate is used to determine which quadwords of xmm2 and xmm3/m128 should be used.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand2</th>
<th>Operand3</th>
<th>Operand4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Performs a carry-less multiplication of two quadwords, selected from the first source and second source operand according to the value of the immediate byte. Bits 4 and 0 are used to select which 64-bit half of each operand to use according to Table 4-13, other bits of the immediate byte are ignored.

Table 4-13. PCLMULQDQ Quadword Selection of Immediate Byte

<table>
<thead>
<tr>
<th>Imm[4]</th>
<th>Imm[0]</th>
<th>PCLMULQDQ Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>CL_MUL( SRC2[63:0], SRC1[63:0] )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>CL_MUL( SRC2[63:0], SRC1[127:64] )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>CL_MUL( SRC2[127:64], SRC1[63:0] )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>CL_MUL( SRC2[127:64], SRC1[127:64] )</td>
</tr>
</tbody>
</table>
NOTES:
1. SRC2 denotes the second source operand, which can be a register or memory; SRC1
denotes the first source and destination operand.

The first source operand and the destination operand are the same and must be an
XMM register. The second source operand can be an XMM register or a 128-bit
memory location. Bits (VLMAX-1:128) of the corresponding YMM destination register
remain unchanged.

Compilers and assemblers may implement the following pseudo-op syntax to simply
programming and emit the required encoding for Imm8.

Table 4-14. Pseudo-Op and PCLMULQDQ Implementation

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>Imm8 Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCLMULLQLQDQ xmm1, xmm2</td>
<td>0000_0000B</td>
</tr>
<tr>
<td>PCLMULHQLQDQ xmm1, xmm2</td>
<td>0000_0001B</td>
</tr>
<tr>
<td>PCLMULLQHDQ xmm1, xmm2</td>
<td>0001_0000B</td>
</tr>
<tr>
<td>PCLMULHQHDQ xmm1, xmm2</td>
<td>0001_0001B</td>
</tr>
</tbody>
</table>

Operation

PCLMULQDQ
IF (Imm8[0] = 0 )
    THEN
        TEMP1 ← SRC1 [63:0];
    ELSE
        TEMP1 ← SRC1 [127:64];
    FI
IF (Imm8[4] = 0 )
    THEN
        TEMP2 ← SRC2 [63:0];
    ELSE
        TEMP2 ← SRC2 [127:64];
    FI
For i = 0 to 63 {
    TmpB [i] ← (TEMP1[0] and TEMP2[i]);
    For j = 1 to i {
        TmpB [i] ← TmpB [i] xor (TEMP1[j] and TEMP2[i-j])
    }
    DEST[i] ← TmpB [i];
}
INSTRUCTION SET REFERENCE, M-Z

PCLMULQDQ - Carry-Less Multiplication Quadword

```
TmpB[i] ← 0;
For j = i - 63 to 63 {
    TmpB[i] ← TmpB[i] xor (TEMP1[j] and TEMP2[i - j])
}
DEST[i] ← TmpB[i];
}
DEST[127] ← 0;
DEST[VLMAX-1:128] (Unmodified)

VPCLMULQDQ
IF (Imm8[0] = 0 )
    THEN
        TEMP1 ← SRC1 [63:0];
    ELSE
        TEMP1 ← SRC1 [127:64];
    FI
IF (Imm8[4] = 0 )
    THEN
        TEMP2 ← SRC2 [63:0];
    ELSE
        TEMP2 ← SRC2 [127:64];
    FI
For i = 0 to 63 {
    TmpB[i] ← (TEMP1[0] and TEMP2[i]);
    For j = 1 to i{
        TmpB[i] ← TmpB[i] xor (TEMP1[j] and TEMP2[i - j])
    }
    DEST[i] ← TmpB[i];
}
For i = 64 to 126 {
    TmpB[i] ← 0;
    For j = i - 63 to 63 {
        TmpB[i] ← TmpB[i] xor (TEMP1[j] and TEMP2[i - j])
    }
    DEST[i] ← TmpB[i];
}
DEST[VLMAX-1:127] ← 0;
```

Intel C/C++ Compiler Intrinsic Equivalent

```
(V)PCLMULQDQ: __m128i __mm_clmulepi64_si128 (__m128i, __m128i, const int)
```
SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4.
## PCMPEQB/PCMPEQW/PCMPEQD— Compare Packed Data for Equal

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 74 /r&lt;sup&gt;1&lt;/sup&gt; PCMPEQB mm, mm/m64</td>
<td>RM V/V</td>
<td>MMX</td>
<td>Compare packed bytes in mm/m64 and mm for equality.</td>
<td></td>
</tr>
<tr>
<td>66 0F 74 /r PCMPEQB xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Compare packed bytes in xmm2/m128 and xmm1 for equality.</td>
<td></td>
</tr>
<tr>
<td>0F 75 /r&lt;sup&gt;1&lt;/sup&gt; PCMPEQW mm, mm/m64</td>
<td>RM V/V</td>
<td>MMX</td>
<td>Compare packed words in mm/m64 and mm for equality.</td>
<td></td>
</tr>
<tr>
<td>66 0F 75 /r PCMPEQW xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Compare packed words in xmm2/m128 and xmm1 for equality.</td>
<td></td>
</tr>
<tr>
<td>0F 76 /r&lt;sup&gt;1&lt;/sup&gt; PCMPEQD mm, mm/m64</td>
<td>RM V/V</td>
<td>MMX</td>
<td>Compare packed doublewords in mm/m64 and mm for equality.</td>
<td></td>
</tr>
<tr>
<td>66 0F 76 /r PCMPEQD xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Compare packed doublewords in xmm2/m128 and xmm1 for equality.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 74 /r VPCMPEQB xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Compare packed bytes in xmm3/m128 and xmm2 for equality.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 75 /r VPCMPEQW xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Compare packed words in xmm3/m128 and xmm2 for equality.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 76 /r VPCMPEQD xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Compare packed doublewords in xmm3/m128 and xmm2 for equality.</td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:
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**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD compare for equality of the packed bytes, words, or doublewords in the destination operand (first operand) and the source operand (second operand). If a pair of data elements is equal, the corresponding data element in the destination operand is set to all 1s; otherwise, it is set to all 0s. The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

The PCMPEQB instruction compares the corresponding bytes in the destination and source operands; the PCMPEQW instruction compares the corresponding words in the destination and source operands; and the PCMPEQD instruction compares the corresponding doublewords in the destination and source operands.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PCMPEQB (with 64-bit operands)**

1. IF DEST[7:0] = SRC[7:0] THEN DEST[7:0] ← FFH; ELSE DEST[7:0] ← 0; Fl;
2. (* Continue comparison of 2nd through 7th bytes in DEST and SRC *)
   ELSE DEST[63:56] ← 0; Fl;

**PCMPEQB (with 128-bit operands)**

1. IF DEST[7:0] = SRC[7:0] THEN DEST[7:0] ← FFH; ELSE DEST[7:0] ← 0; Fl;
   (* Continue comparison of 2nd through 15th bytes in DEST and SRC *)
ELSE DEST[127:120] ← 0; Fl;

**PCMPEQw (with 64-bit operands)**

IF DEST[15:0] = SRC[15:0]
  THEN DEST[15:0] ← FFFFH;
  ELSE DEST[15:0] ← 0; Fl;

(* Continue comparison of 2nd and 3rd words in DEST and SRC *)

IF DEST[63:48] = SRC[63:48]
  THEN DEST[63:48] ← FFFFH;
  ELSE DEST[63:48] ← 0; Fl;

**PCMPEQw (with 128-bit operands)**

IF DEST[15:0] = SRC[15:0]
  THEN DEST[15:0] ← FFFFH;
  ELSE DEST[15:0] ← 0; Fl;

(* Continue comparison of 2nd through 7th words in DEST and SRC *)

  THEN DEST[127:112] ← FFFFH;
  ELSE DEST[127:112] ← 0; Fl;

**PCMPEQD (with 64-bit operands)**

IF DEST[31:0] = SRC[31:0]
  THEN DEST[31:0] ←FFFFFFFFH;
  ELSE DEST[31:0] ← 0; Fl;

  THEN DEST[63:32] ← FFFFFFFFFH;
  ELSE DEST[63:32] ← 0; Fl;

**PCMPEQD (with 128-bit operands)**

IF DEST[31:0] = SRC[31:0]
  THEN DEST[31:0] ←FFFFFFFFH;
  ELSE DEST[31:0] ← 0; Fl;

(* Continue comparison of 2nd and 3rd doublewords in DEST and SRC *)

IF DEST[127:96] = SRC[127:96]
  THEN DEST[127:96] ← FFFFFFFFFH;
  ELSE DEST[127:96] ← 0; Fl;

**VPCMPEQB (VEX.128 encoded version)**

DEST[127:0] ← COMPARE_BYTES_EQUAL(SRC1,SRC2)
DEST[VLMAX-1:128] ← 0

**VPCMPEQW (VEX.128 encoded version)**

DEST[127:0] ← COMPARE_WORDS_EQUAL(SRC1,SRC2)
DEST[VLMAX-1:128] ← 0
VPCMPEQD (VEX.128 encoded version)
DEST[127:0] ← COMPARE_DWORDS_EQUAL(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PCMPEQB:  __m64 _mm_cmpeq_pi8 (__m64 m1, __m64 m2)
PCMPEQW:  __m64 _mm_cmpeq_pi16 (__m64 m1, __m64 m2)
PCMPEQD:  __m64 _mm_cmpeq_pi32 (__m64 m1, __m64 m2)
PCMPEQB:  __m128i _mm_cmpeq_epi8 ( __m128i a, __m128i b)
PCMPEQW:  __m128i _mm_cmpeq_epi16 ( __m128i a, __m128i b)
PCMPEQD:  __m128i _mm_cmpeq_epi32 ( __m128i a, __m128i b)

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
**PCMPEQQ — Compare Packed Qword Data for Equal**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 29 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4.1</td>
<td>Compare packed qwords in xmm2/m128 and xmm1 for equality.</td>
</tr>
<tr>
<td>PCMPEQQ xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 29 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed quadwords in xmm3/m128 and xmm2 for equality.</td>
</tr>
<tr>
<td>VPCMPEQQ xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an SIMD compare for equality of the packed quadwords in the destination operand (first operand) and the source operand (second operand). If a pair of data elements is equal, the corresponding data element in the destination is set to all 1s; otherwise, it is set to 0s.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

IF (DEST[63:0] = SRC[63:0])
THEN DEST[63:0] ← FFFFFFFFFFFFFFFFH;
ELSE DEST[63:0] ← 0; FI;

IF (DEST[127:64] = SRC[127:64])
THEN DEST[127:64] ← FFFFFFFFFFFFFFFFH;
ELSE DEST[127:64] ← 0; FI;

**VPCMPEQQ (VEX.128 encoded version)**

DEST[127:0] ← COMPARE_QWORDS_EQUAL(SRC1,SRC2)
DEST[VLMAX-1:128] ← 0
Intel C/C++ Compiler Intrinsic Equivalent

PCMPEQQ: __m128i _mm_cmpeq_epi64(__m128i a, __m128i b);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
**Description**

The instruction compares and processes data from two string fragments based on the encoded value in the Imm8 Control Byte (see Section 4.1, “Imm8 Control Byte Operation for PCMPESTRI / PCMPESTRM / PCMPISTRI / PCMPISTRM”), and generates an index stored to the count register (ECX/RCX).

Each string fragment is represented by two values. The first value is an xmm (or possibly m128 for the second operand) which contains the data elements of the string (byte or word data). The second value is stored in an input length register. The input length register is EAX/RAX (for xmm1) or EDX/RDX (for xmm2/m128). The length represents the number of bytes/words which are valid for the respective xmm/m128 data.

The length of each input is interpreted as being the absolute-value of the value in the length register. The absolute-value computation saturates to 16 (for bytes) and 8 (for words), based on the value of imm8[bit3] when the value in the length register is greater than 16 (8) or less than -16 (-8).

The comparison and aggregation operations are performed according to the encoded value of Imm8 bit fields (see Section 4.1). The index of the first (or last, according to imm8[6]) set bit of IntRes2 (see Section 4.1.4) is returned in ECX. If no bits are set in IntRes2, ECX is set to 16 (8).

Note that the Arithmetic Flags are written in a non-standard manner in order to supply the most relevant information:

- **CFlag** – Reset if IntRes2 is equal to zero, set otherwise

---

PCPPESTRI — Packed Compare Explicit Length Strings, Return Index

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode</th>
<th>CPUID Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 61 /r imm8 PCMPESTRI xmm1, xmm2/m128, imm8</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4.2</td>
<td>Perform a packed comparison of string data with explicit lengths, generating an index, and storing the result in ECX.</td>
</tr>
<tr>
<td>VEX.128.66.0F3A.W1 61 /r ib VPCMPESTRI xmm1, xmm2/m128, imm8</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Perform a packed comparison of string data with explicit lengths, generating an index, and storing the result in ECX.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRMreg (r)</td>
<td>ModRMreg (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, M-Z

ZFlag – Set if absolute-value of EDX is < 16 (8), reset otherwise
SFlag – Set if absolute-value of EAX is < 16 (8), reset otherwise
OFlag – IntRes2[0]
AFlag – Reset
PFlag – Reset

Effective Operand Size

<table>
<thead>
<tr>
<th>Operating mode/size</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Length 1</th>
<th>Length 2</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>EAX</td>
<td>EDX</td>
<td>ECX</td>
</tr>
<tr>
<td>32 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>EAX</td>
<td>EDX</td>
<td>ECX</td>
</tr>
<tr>
<td>64 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>EAX</td>
<td>EDX</td>
<td>ECX</td>
</tr>
<tr>
<td>64 bit + REX.W</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>RAX</td>
<td>RDX</td>
<td>RCX</td>
</tr>
</tbody>
</table>

Intel C/C++ Compiler Intrinsic Equivalent For Returning Index

int _mm_cmpestri (__m128i a, int la, __m128i b, int lb, const int mode);

Intel C/C++ Compiler Intrinsics For Reading EFlag Results

int _mm_cmpestra (__m128i a, int la, __m128i b, int lb, const int mode);
int _mm_cmpestrc (__m128i a, int la, __m128i b, int lb, const int mode);
int _mm_cmpestro (__m128i a, int la, __m128i b, int lb, const int mode);
int _mm_cmpestrs (__m128i a, int la, __m128i b, int lb, const int mode);
int _mm_cmpestrz (__m128i a, int la, __m128i b, int lb, const int mode);

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 4; additionally

#UD If VEX.L = 1.
    If VEX.vvv != 1111B.
PCMPESTRM — Packed Compare Explicit Length Strings, Return Mask

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 60 /r imm8</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_2</td>
<td>Perform a packed comparison of string data with explicit lengths, generating a mask, and storing the result in XMM0.</td>
</tr>
<tr>
<td>PCMPESTRM xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66,0F3A.WIG 60 / r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Perform a packed comparison of string data with explicit lengths, generating a mask, and storing the result in XMM0.</td>
</tr>
<tr>
<td>VPCMPESTRM xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

The instruction compares data from two string fragments based on the encoded value in the imm8 control byte (see Section 4.1, “Imm8 Control Byte Operation for PCMPESTR1 / PCMPESTRM / PCMPISTRI / PCMPISTRM”), and generates a mask stored to XMM0.

Each string fragment is represented by two values. The first value is an xmm (or possibly m128 for the second operand) which contains the data elements of the string (byte or word data). The second value is stored in an input length register. The input length register is EAX/RAX (for xmm1) or EDX/RDX (for xmm2/m128). The length represents the number of bytes/words which are valid for the respective xmm/m128 data.

The length of each input is interpreted as being the absolute-value of the value in the length register. The absolute-value computation saturates to 16 (for bytes) and 8 (for words), based on the value of imm8[bit3] when the value in the length register is greater than 16 (8) or less than -16 (-8).

The comparison and aggregation operations are performed according to the encoded value of Imm8 bit fields (see Section 4.1). As defined by imm8[6], IntRes2 is then either stored to the least significant bits of XMM0 (zero extended to 128 bits) or expanded into a byte/word-mask and then stored to XMM0.

Note that the Arithmetic Flags are written in a non-standard manner in order to supply the most relevant information:

- CFlag - Reset if IntRes2 is equal to zero, set otherwise
**INSTRUCTION SET REFERENCE, M-Z**

ZFlag – Set if absolute-value of EDX is < 16 (8), reset otherwise
SFlag – Set if absolute-value of EAX is < 16 (8), reset otherwise
OFlag – IntRes2[0]
AFlag – Reset
PFlag – Reset

Note: In VEX.128 encoded versions, bits (VLMAX-1:128) of XMM0 are zeroed.
VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.

**Effective Operand Size**

<table>
<thead>
<tr>
<th>Operating mode/size</th>
<th>Operand1</th>
<th>Operand 2</th>
<th>Length1</th>
<th>Length2</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>EAX</td>
<td>EDX</td>
<td>XMM0</td>
</tr>
<tr>
<td>32 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>EAX</td>
<td>EDX</td>
<td>XMM0</td>
</tr>
<tr>
<td>64 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>EAX</td>
<td>EDX</td>
<td>XMM0</td>
</tr>
<tr>
<td>64 bit + REX.W</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>RAX</td>
<td>RDX</td>
<td>XMM0</td>
</tr>
</tbody>
</table>

**Intel C/C++ Compiler Intrinsic Equivalent For Returning Mask**

__m128i _mm_cmpestrm (__m128i a, int la, __m128i b, int lb, const int mode);

**Intel C/C++ Compiler Intrinsics For Reading EFlag Results**

int _mm_cmpestra (__m128i a, int la, __m128i b, int lb, const int mode);
int _mm_cmpestrc (__m128i a, int la, __m128i b, int lb, const int mode);
int _mm_cmpestro (__m128i a, int la, __m128i b, int lb, const int mode);
int _mm_cmpestrs (__m128i a, int la, __m128i b, int lb, const int mode);
int _mm_cmpestrz (__m128i a, int la, __m128i b, int lb, const int mode);

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally
#UD

If VEX.L = 1.

If VEX.vvvv != 1111B.
### PCMPGTB/PCMPGTW/PCMPGTD—Compare Packed Signed Integers for Greater Than

<table>
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<tr>
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<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 64 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Compare packed signed byte integers in mm and mm/m64 for greater than.</td>
</tr>
<tr>
<td>PCMPGTB mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF 64 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compare packed signed byte integers in xmm1 and xmm2/m128 for greater than.</td>
</tr>
<tr>
<td>PCMPGTB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF 65 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Compare packed signed word integers in mm and mm/m64 for greater than.</td>
</tr>
<tr>
<td>PCMPGTW mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF 65 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compare packed signed word integers in xmm1 and xmm2/m128 for greater than.</td>
</tr>
<tr>
<td>PCMPGTW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF 66 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Compare packed signed doubleword integers in mm and mm/m64 for greater than.</td>
</tr>
<tr>
<td>PCMPGTD mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF 66 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compare packed signed doubleword integers in xmm1 and xmm2/m128 for greater than.</td>
</tr>
<tr>
<td>PCMPGTD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 64 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed signed byte integers in xmm2 and xmm3/m128 for greater than.</td>
</tr>
<tr>
<td>VPCMPGTB xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 65 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed signed word integers in xmm2 and xmm3/m128 for greater than.</td>
</tr>
<tr>
<td>VPCMPGTW xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, M-Z

VEX.NDS.128.66.0F.WIG 66 /r
VPCMPGTD xmm1, xmm2, xmm3/m128

RVM V/V AVX

Compare packed signed doubleword integers in xmm2 and xmm3/m128 for greater than.

NOTES:

Instruction Operand Encoding

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<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs an SIMD signed compare for the greater value of the packed byte, word, or doubleword integers in the destination operand (first operand) and the source operand (second operand). If a data element in the destination operand is greater than the corresponding date element in the source operand, the corresponding data element in the destination operand is set to all 1s; otherwise, it is set to all 0s. The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

The PCMPGTB instruction compares the corresponding signed byte integers in the destination and source operands; the PCMPGTW instruction compares the corresponding signed word integers in the destination and source operands; and the PCMPGTD instruction compares the corresponding signed doubleword integers in the destination and source operands.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

PCMPGTB (with 64-bit operands)

IF DEST[7:0] > SRC[7:0]
THEN DEST[7:0] ← FFH;

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PCMPGTB/PCMPGTW/PCMPGTD—Compare Packed Signed Integers for Greater Than
ELSE DEST[7:0] ← 0; FI;
(* Continue comparison of 2nd through 7th bytes in DEST and SRC *)
IF DEST[63:56] > SRC[63:56]
    THEN DEST[63:56] ← FFH;
    ELSE DEST[63:56] ← 0; FI;

PCMPGTB (with 128-bit operands)
IF DEST[7:0] > SRC[7:0]
    THEN DEST[7:0] ← FFH;
    ELSE DEST[7:0] ← 0; FI;
(* Continue comparison of 2nd through 15th bytes in DEST and SRC *)
IF DEST[127:120] > SRC[127:120]
    THEN DEST[127:120] ← FFH;
    ELSE DEST[127:120] ← 0; FI;

PCMPGTW (with 64-bit operands)
IF DEST[15:0] > SRC[15:0]
    THEN DEST[15:0] ← FFFFH;
    ELSE DEST[15:0] ← 0; FI;
(* Continue comparison of 2nd and 3rd words in DEST and SRC *)
IF DEST[63:48] > SRC[63:48]
    THEN DEST[63:48] ← FFFFH;
    ELSE DEST[63:48] ← 0; FI;

PCMPGTW (with 128-bit operands)
IF DEST[15:0] > SRC[15:0]
    THEN DEST[15:0] ← FFFFH;
    ELSE DEST[15:0] ← 0; FI;
(* Continue comparison of 2nd through 7th words in DEST and SRC *)
IF DEST[63:48] > SRC[127:112]
    THEN DEST[127:112] ← FFFFH;
    ELSE DEST[127:112] ← 0; FI;

PCMPGTD (with 64-bit operands)
IF DEST[31:0] > SRC[31:0]
    THEN DEST[31:0] ← FFFFFFFFH;
    ELSE DEST[31:0] ← 0; FI;
    THEN DEST[63:32] ← FFFFFFFFH;
    ELSE DEST[63:32] ← 0; FI;

PCMPGTD (with 128-bit operands)
IF DEST[31:0] > SRC[31:0]
    THEN DEST[31:0] ← FFFFFFFFH;
    ELSE DEST[31:0] ← 0; FI;
PCMPGTB/PCMPGTW/PCMPGTD—Compare Packed Signed Integers for Greater Than

(* Continue comparison of 2nd and 3rd doublewords in DEST and SRC *)

IF DEST[127:96] > SRC[127:96]
    THEN DEST[127:96] ← FFFFFFFFH;
ELSE DEST[127:96] ← 0; FI;

VPCMPGTB (VEX.128 encoded version)
DEST[127:0] ← COMPARE_BYTES_GREATER(SRC1,SRC2)
DEST[VLMAX-1:128] ← 0

VPCMPGTW (VEX.128 encoded version)
DEST[127:0] ← COMPARE_WORDS_GREATER(SRC1,SRC2)
DEST[VLMAX-1:128] ← 0

VPCMPGTD (VEX.128 encoded version)
DEST[127:0] ← COMPARE_DWORDS_GREATER(SRC1,SRC2)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents

PCMPGTB: __m64 _mm_cmpgt_pi8 (__m64 m1, __m64 m2)
PCMPGTW: __m64 _mm_pcmpgt_pi16 (__m64 m1, __m64 m2)
DCMPGTD: __m64 _mm_pcmpgt_pi32 (__m64 m1, __m64 m2)
PCMPGTB: __m128i _mm_cmpgt_epi8 ( __m128i a, __m128i b)
PCMPGTW: __m128i _mm_pcmpgt_epi16 ( __m128i a, __m128i b)
DCMPGTD: __m128i _mm_pcmpgt_epi32 ( __m128i a, __m128i b)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PCMPGTQ — Compare Packed Data for Greater Than

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 37 /r PCMPGTQ xmm1,xmm2/m128</td>
<td>RM V/V</td>
<td>SSE4_2</td>
<td>Compare packed signed qwords in xmm2/m128 and xmm1 for greater than.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 37 /r VPCMPGTQ xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Compare packed signed qwords in xmm2 and xmm3/m128 for greater than.</td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an SIMD signed compare for the packed quadwords in the destination operand (first operand) and the source operand (second operand). If the data element in the first (destination) operand is greater than the corresponding element in the second (source) operand, the corresponding data element in the destination is set to all 1s; otherwise, it is set to 0s.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

IF (DEST[63-0] > SRC[63-0])
    THEN DEST[63-0] ← FFFFFFFFHH;
    ELSE DEST[63-0] ← 0; FI

IF (DEST[127-64] > SRC[127-64])
    THEN DEST[127-64] ← FFFFFFFFHH;
    ELSE DEST[127-64] ← 0; FI

**VPCMPGTQ (VEX.128 encoded version)**

DEST[127:0] ← COMPARE_QWORDS_GREATER(SRC1,SRC2)
DEST[VLMAX-1:128] ← 0
INSTRUCTION SET REFERENCE, M-Z

Intel C/C++ Compiler Intrinsic Equivalent

PCMPGTQ: __m128i _mm_cmpgt_epi64(__m128i a, __m128i b)

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
INSTRUCTION SET REFERENCE, M-Z

PCMPISTRI — Packed Compare Implicit Length Strings, Return Index

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 63 /r imm8 PCMPISTRI xmm1, xmm2/m128, imm8</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_2</td>
<td>Perform a packed comparison of string data with implicit lengths, generating an index, and storing the result in ECX.</td>
</tr>
<tr>
<td>VEX.128.66,0F3A.WIG 63 /r ib VPCMPISTRI xmm1, xmm2/m128, imm8</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Perform a packed comparison of string data with implicit lengths, generating an index, and storing the result in ECX.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r)</td>
<td>ModRMreg (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

The instruction compares data from two strings based on the encoded value in the Imm8 Control Byte (see Section 4.1, “Imm8 Control Byte Operation for PCMPESTRI / PCMPESTRM / PCMPISTRI / PCMPISTRM”), and generates an index stored to ECX.

Each string is represented by a single value. The value is an xmm (or possibly m128 for the second operand) which contains the data elements of the string (byte or word data). Each input byte/word is augmented with a valid/invalid tag. A byte/word is considered valid only if it has a lower index than the least significant null byte/word. (The least significant null byte/word is also considered invalid.)

The comparison and aggregation operations are performed according to the encoded value of Imm8 bit fields (see Section 4.1). The index of the first (or last, according to imm8[6]) set bit of IntRes2 is returned in ECX. If no bits are set in IntRes2, ECX is set to 16 (8).

Note that the Arithmetic Flags are written in a non-standard manner in order to supply the most relevant information:

- CFlag – Reset if IntRes2 is equal to zero, set otherwise
- ZFlag – Set if any byte/word of xmm2/mem128 is null, reset otherwise
- SFlag – Set if any byte/word of xmm1 is null, reset otherwise
- OFlag – IntRes2[0]
- AFlag – Reset
- PFlag – Reset
INSTRUCTION SET REFERENCE, M-Z

Note: In VEX.128 encoded version, VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.

Effective Operand Size

<table>
<thead>
<tr>
<th>Operating mode/size</th>
<th>Operand1</th>
<th>Operand 2</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>ECX</td>
</tr>
<tr>
<td>32 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>ECX</td>
</tr>
<tr>
<td>64 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>ECX</td>
</tr>
<tr>
<td>64 bit + REX.W</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>RCX</td>
</tr>
</tbody>
</table>

Intel C/C++ Compiler Intrinsic Equivalent For Returning Index

int _mm_cmpistri (__m128i a, __m128i b, const int mode);

Intel C/C++ Compiler Intrinsics For Reading EFlag Results

int _mm_cmpistra (__m128i a, __m128i b, const int mode);
int _mm_cmpistrc (__m128i a, __m128i b, const int mode);
int _mm_cmpistro (__m128i a, __m128i b, const int mode);
int _mm_cmpistrs (__m128i a, __m128i b, const int mode);
int _mm_cmpistrz (__m128i a, __m128i b, const int mode);

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 4; additionally
#UD If VEX.L = 1.
    If VEX.vvvv != 1111B.
PCMPISTRM — Packed Compare Implicit Length Strings, Return Mask

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 62 /r imm8</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_2</td>
<td>Perform a packed comparison of string data with implicit lengths, generating a mask, and storing the result in XMM0.</td>
</tr>
<tr>
<td>PCMPISTRM xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F3A.WIG 62 /r ib</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Perform a packed comparison of string data with implicit lengths, generating a Mask, and storing the result in XMM0.</td>
</tr>
<tr>
<td>VPCMPISTRM xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r)</td>
<td>ModRMreg/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

The instruction compares data from two strings based on the encoded value in the imm8 byte (see Section 4.1, “Imm8 Control Byte Operation for PCMPESTRI / PCMPESTRM / PCMPISTRI / PCMPISTRM”) generating a mask stored to XMM0.

Each string is represented by a single value. The value is an xmm (or possibly m128 for the second operand) which contains the data elements of the string (byte or word data). Each input byte/word is augmented with a valid/invalid tag. A byte/word is considered valid only if it has a lower index than the least significant null byte/word. (The least significant null byte/word is also considered invalid.)

The comparison and aggregation operation are performed according to the encoded value of Imm8 bit fields (see Section 4.1). As defined by imm8[6], IntRes2 is then either stored to the least significant bits of XMM0 (zero extended to 128 bits) or expanded into a byte/word-mask and then stored to XMM0.

Note that the Arithmetic Flags are written in a non-standard manner in order to supply the most relevant information:

- CFlag – Reset if IntRes2 is equal to zero, set otherwise
- ZFlag – Set if any byte/word of xmm2/mem128 is null, reset otherwise
- SFlag – Set if any byte/word of xmm1 is null, reset otherwise
- OFlag – IntRes2[0]
- AFlag – Reset
- PFlag – Reset
Note: In VEX.128 encoded versions, bits (VLMAX-1:128) of XMM0 are zeroed. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.

Effective Operand Size

<table>
<thead>
<tr>
<th>Operating mode/size</th>
<th>Operand1</th>
<th>Operand 2</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>XMM0</td>
</tr>
<tr>
<td>32 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>XMM0</td>
</tr>
<tr>
<td>64 bit</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>XMM0</td>
</tr>
<tr>
<td>64 bit + REX.W</td>
<td>xmm</td>
<td>xmm/m128</td>
<td>XMM0</td>
</tr>
</tbody>
</table>

Intel C/C++ Compiler Intrinsic Equivalent For Returning Mask

__m128i _mm_cmpistrm (__m128i a, __m128i b, const int mode);

Intel C/C++ Compiler Intrinsics For Reading EFlag Results

int _mm_cmpistra (__m128i a, __m128i b, const int mode);
int _mm_cmpistrc (__m128i a, __m128i b, const int mode);
int _mm_cmpistro (__m128i a, __m128i b, const int mode);
int _mm_cmpistrs (__m128i a, __m128i b, const int mode);
int _mm_cmpistrz (__m128i a, __m128i b, const int mode);

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 4; additionally
#UD If VEX.L = 1.
    If VEX.vvvv != 1111B.
### PEXTRB/PEXTRD/PEXTRQ — Extract Byte/Dword/Qword

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 14 /r ib</td>
<td>MRI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Extract a byte integer value from xmm2 at the source byte offset specified by imm8 into rreg or m8. The upper bits of r32 or r64 are zeroed.</td>
</tr>
<tr>
<td>66 0F 3A 16 /r ib</td>
<td>MRI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Extract a dword integer value from xmm2 at the source dword offset specified by imm8 into r/m32.</td>
</tr>
<tr>
<td>66 REX.W 0F 3A 16 /r ib</td>
<td>MRI</td>
<td>V/N.E.</td>
<td>SSE4_1</td>
<td>Extract a qword integer value from xmm2 at the source qword offset specified by imm8 into r/m64.</td>
</tr>
<tr>
<td>VEX.128.66.0F3A.W0 14 /r ib</td>
<td>MRI</td>
<td>V/V</td>
<td>AVX</td>
<td>Extract a byte integer value from xmm2 at the source byte offset specified by imm8 into reg or m8. The upper bits of r64/r32 is filled with zeros.</td>
</tr>
<tr>
<td>VEX.128.66.0F3A.W0 16 /r ib</td>
<td>MRI</td>
<td>V/V</td>
<td>AVX</td>
<td>Extract a dword integer value from xmm2 at the source dword offset specified by imm8 into r32/m32.</td>
</tr>
<tr>
<td>VEX.128.66.0F3A.W1 16 /r ib</td>
<td>MRI</td>
<td>V/i</td>
<td>AVX</td>
<td>Extract a qword integer value from xmm2 at the source dword offset specified by imm8 into r64/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**
1. In 64-bit mode, VEX.W1 is ignored for VPEXTRB (similar to legacy REX.W=1 prefix in PEXTRB).

#### Instruction Operand Encoding

<table>
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<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MRI</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, M-Z

Description

Extract a byte/dword/qword integer value from the source XMM register at a byte/dword/qword offset determined from imm8[3:0]. The destination can be a register or byte/dword/qword memory location. If the destination is a register, the upper bits of the register are zero extended.

In legacy non-VEX encoded version and if the destination operand is a register, the default operand size in 64-bit mode for PEXTRB/PEXTRD is 64 bits, the bits above the least significant byte/dword data are filled with zeros. PEXTRQ is not encodable in non-64-bit modes and requires REX.W in 64-bit mode.

Note: In VEX.128 encoded versions, VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD. If the destination operand is a register, the default operand size in 64-bit mode for VPEXTRB/VPEXTRD is 64 bits, the bits above the least significant byte/word/dword data are filled with zeros. Attempt to execute VPEXTRQ in non-64-bit mode will cause #UD.

Operation

CASE of

PEXTRB: SEL ← COUNT[3:0];
    TEMP ← (Src >> SEL*8) AND FFH;
    IF (DEST = Mem8)
        THEN
            Mem8 ← TEMP[7:0];
        ELSE IF (64-Bit Mode and 64-bit register selected)
            THEN
                R64[7:0] ← TEMP[7:0];
                r64[63:8] ← ZERO_FILL;
            ELSE
                R32[7:0] ← TEMP[7:0];
                r32[31:8] ← ZERO_FILL;
        FI;
    PEXTRD:SEL ← COUNT[1:0];
    TEMP ← (Src >> SEL*32) AND FFFF_FFFFH;
    DEST ← TEMP;
    PEXTRQ: SEL ← COUNT[0];
    TEMP ← (Src >> SEL*64);
    DEST ← TEMP;

EASC:

(V)PEXTRTD/(V)PEXTRQ

IF (64-Bit Mode and 64-bit dest operand)
THEN
    Src_Offset ← Imm8[0]
r64/m64 ← (Src >> Src_Offset * 64)
ELSE
    Src_Offset ← Imm8[1:0]
    r32/m32 ← ((Src >> Src_Offset *32) AND 0FFFFFFFFh);
FI

(V)PEXTRB (dest=m8)
SRC_Offset ← Imm8[3:0]
Mem8 ← (Src >> Src_Offset*8)

(V)PEXTRB (dest=reg)
IF (64-Bit Mode)
THEN
    SRC_Offset ← Imm8[3:0]
    DEST[7:0] ← ((Src >> Src_Offset*8) AND 0FFh)
    DEST[63:8] ← ZERO_FILL;
ELSE
    SRC_Offset ← Imm8[3:0];
    DEST[7:0] ← ((Src >> Src_Offset*8) AND 0FFh);
    DEST[31:8] ← ZERO_FILL;
FI

Intel C/C++ Compiler Intrinsic Equivalent
PEXTRB: int _mm_extract_epi8 (__m128i src, const int ndx);
PEXTRD: int _mm_extract_epi32 (__m128i src, const int ndx);
PEXTRQ: __int64 _mm_extract_epi64 (__m128i src, const int ndx);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD
    If VEX.L = 1.
    If VEX.vvvv != 1111B.
    If VPEXTRQ in non-64-bit mode, VEX.W=1.
PEXTRW—Extract Word

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C5 /r ib¹</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE</td>
<td>Extract the word specified by imm8 from mm and move it to reg, bits 15-0. The upper bits of r32 or r64 is zeroed.</td>
</tr>
<tr>
<td>PEXTRW reg, mm, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F C5 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Extract the word specified by imm8 from xmm and move it to reg, bits 15-0. The upper bits of r32 or r64 is zeroed.</td>
</tr>
<tr>
<td>PEXTRW reg, xmm, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 3A 15 /r ib</td>
<td>MRI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Extract the word specified by imm8 from xmm and copy it to lowest 16 bits of reg or m16. Zero-extend the result in the destination, r32 or r64.</td>
</tr>
<tr>
<td>PEXTRW reg/m16, xmm, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:W0 C5 /r ib</td>
<td>RMI</td>
<td>V²/V</td>
<td>AVX</td>
<td>Extract the word specified by imm8 from xmm1 and move it to reg, bits 15:0. Zero-extend the result. The upper bits of r64/r32 is filled with zeros.</td>
</tr>
<tr>
<td>VPEXTRW reg, xmm1, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F3A:W0 15 /r ib</td>
<td>MRI</td>
<td>V/V</td>
<td>AVX</td>
<td>Extract a word integer value from xmm2 at the source word offset specified by imm8 into reg or m16. The upper bits of r64/r32 is filled with zeros.</td>
</tr>
<tr>
<td>VPEXTRW reg/m16, xmm2, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
2. In 64-bit mode, VEX.W1 is ignored for VPEXTRW (similar to legacy REX.W=1 prefix in PEXTRW).

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, M-Z

Description
Copies the word in the source operand (second operand) specified by the count operand (third operand) to the destination operand (first operand). The source operand can be an MMX technology register or an XMM register. The destination operand can be the low word of a general-purpose register or a 16-bit memory address. The count operand is an 8-bit immediate. When specifying a word location in an MMX technology register, the 2 least-significant bits of the count operand specify the location; for an XMM register, the 3 least-significant bits specify the location. The content of the destination register above bit 16 is cleared (set to all 0s).

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15, R8-15). If the destination operand is a general-purpose register, the default operand size is 64-bits in 64-bit mode.

Note: In VEX.128 encoded versions, VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD. If the destination operand is a register, the default operand size in 64-bit mode for VPEXTRW is 64 bits, the bits above the least significant byte/word/dword data are filled with zeros.

Operation
IF (DEST = Mem16)
THEN
SEL ← COUNT[2:0];
TEMP ← (Src >> SEL*16) AND FFFFH;
Mem16 ← TEMP[15:0];
ELSE IF (64-Bit Mode and destination is a general-purpose register)
THEN
FOR (PEXTRW instruction with 64-bit source operand)
{ SEL ← COUNT[1:0];
  TEMP ← (SRC >> (SEL + 16)) AND FFFFH;
  r64[15:0] ← TEMP[15:0];
  r64[63:16] ← ZERO_FILL; }
FOR (PEXTRW instruction with 128-bit source operand)
{ SEL ← COUNT[2:0];
  TEMP ← (SRC >> (SEL + 16)) AND FFFFH;
  r64[15:0] ← TEMP[15:0];
  r64[63:16] ← ZERO_FILL; }
ELSE
FOR (PEXTRW instruction with 64-bit source operand)
{ SEL ← COUNT[1:0];
  TEMP ← (SRC >> (SEL + 16)) AND FFFFH;

PEXTRW—Extract Word
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INSTRUCTION SET REFERENCE, M-Z

r32[15:0] ← TEMP[15:0];
r32[31:16] ← ZERO_FILL;
FOR (PEXTRW instruction with 128-bit source operand)
{ SEL ← COUNT[2:0];
  TEMP ← (SRC >> (SEL * 16)) AND FFFFH;
  r32[15:0] ← TEMP[15:0];
  r32[31:16] ← ZERO_FILL;
}  
FI;
FI;

(V)PEXTRW (dest=m16)
SRC_Offset ← Imm8[2:0]
Mem16 ← (Src >> SRC_Offset*16)

(V)PEXTRW (dest=reg)
IF (64-Bit Mode)
THEN
  SRC_Offset ← Imm8[2:0]
  DEST[15:0] ← (Src >> SRC_Offset*16) AND 0FFFFh
  DEST[63:16] ← ZERO_FILL;
ELSE
  SRC_Offset ← Imm8[2:0]
  DEST[15:0] ← (Src >> SRC_Offset*16) AND 0FFFFh
  DEST[31:16] ← ZERO_FILL;
FI

Intel C/C++ Compiler Intrinsic Equivalent
PEXTRw: int _mm_extract_pi16 (__m64 a, int n)
PEXTRw: int _mm_extract_epi16 ( __m128i a, int imm)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD If VEX.L = 1.
If VEX.vvvv != 1111B.
### PHADDW/PHADDD — Packed Horizontal Add

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 01 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Add 16-bit integers horizontally, pack to MM1.</td>
</tr>
<tr>
<td>66 0F 38 01 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Add 16-bit integers horizontally, pack to XMM1.</td>
</tr>
<tr>
<td>0F 38 02 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Add 32-bit integers horizontally, pack to MM1.</td>
</tr>
<tr>
<td>66 0F 38 02 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Add 32-bit integers horizontally, pack to XMM1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 01 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add 16-bit integers horizontally, pack to xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 02 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Add 32-bit integers horizontally, pack to xmm1.</td>
</tr>
</tbody>
</table>

**NOTES:**


<table>
<thead>
<tr>
<th>Instruction Operand Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Op/En</td>
</tr>
<tr>
<td>RM</td>
</tr>
<tr>
<td>RVM</td>
</tr>
</tbody>
</table>

### Description

PHADDW adds two adjacent 16-bit signed integers horizontally from the source and destination operands and packs the 16-bit signed results to the destination operand (first operand). PHADDD adds two adjacent 32-bit signed integers horizontally from the source and destination operands and packs the 32-bit signed results to the destination operand (first operand). Both operands can be MMX or XMM registers. When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

Note that these instructions can operate on either unsigned or signed (two’s complement notation) integers; however, it does not set bits in the EFLAGS register to indi-
cate overflow and/or a carry. To prevent undetected overflow conditions, software must control the ranges of the values operated on.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PHADDW (with 64-bit operands)**

{\[
\begin{align*}
\text{mm1}[15-0] &= \text{mm1}[31-16] + \text{mm1}[15-0]; \\
\text{mm1}[31-16] &= \text{mm1}[63-48] + \text{mm1}[47-32]; \\
\text{mm1}[47-32] &= \text{mm2}/\text{m64}[31-16] + \text{mm2}/\text{m64}[15-0]; \\
\text{mm1}[63-48] &= \text{mm2}/\text{m64}[63-48] + \text{mm2}/\text{m64}[47-32];
\end{align*}
\]}

**PHADDW (with 128-bit operands)**

{\[
\begin{align*}
\text{xmm1}[15-0] &= \text{xmm1}[31-16] + \text{xmm1}[15-0]; \\
\text{xmm1}[31-16] &= \text{xmm1}[63-48] + \text{xmm1}[47-32]; \\
\text{xmm1}[47-32] &= \text{xmm1}[95-80] + \text{xmm1}[79-64]; \\
\text{xmm1}[63-48] &= \text{xmm2}/\text{m128}[31-16] + \text{xmm2}/\text{m128}[15-0]; \\
\text{xmm1}[79-64] &= \text{xmm2}/\text{m128}[63-48] + \text{xmm2}/\text{m128}[47-32]; \\
\text{xmm1}[95-80] &= \text{xmm2}/\text{m128}[95-80] + \text{xmm2}/\text{m128}[79-64]; \\
\text{xmm1}[111-96] &= \text{xmm2}/\text{m128}[127-112] + \text{xmm2}/\text{m128}[111-96];
\end{align*}
\]}

**PHADDD (with 64-bit operands)**

{\[
\begin{align*}
\text{mm1}[31-0] &= \text{mm1}[63-32] + \text{mm1}[31-0]; \\
\text{mm1}[63-32] &= \text{mm2}/\text{m64}[63-32] + \text{mm2}/\text{m64}[31-0];
\end{align*}
\]}

**PHADDD (with 128-bit operands)**

{\[
\begin{align*}
\text{xmm1}[31-0] &= \text{xmm1}[63-32] + \text{xmm1}[31-0]; \\
\text{xmm1}[63-32] &= \text{xmm1}[127-96] + \text{xmm1}[95-64]; \\
\text{xmm1}[95-64] &= \text{xmm2}/\text{m128}[63-32] + \text{xmm2}/\text{m128}[31-0]; \\
\text{xmm1}[127-96] &= \text{xmm2}/\text{m128}[127-96] + \text{xmm2}/\text{m128}[95-64];
\end{align*}
\]}

**VPHADDW (VEX.128 encoded version)**

{\[
\begin{align*}
\text{DEST}[15:0] &= \text{SRC1}[31:16] + \text{SRC1}[15:0]; \\
\text{DEST}[31:16] &= \text{SRC1}[63:48] + \text{SRC1}[47:32]; \\
\text{DEST}[47:32] &= \text{SRC1}[95:80] + \text{SRC1}[79:64]; \\
\text{DEST}[63:48] &= \text{SRC1}[127:112] + \text{SRC1}[111:96]; \\
\text{DEST}[79:64] &= \text{SRC2}[31:16] + \text{SRC2}[15:0]; \\
\text{DEST}[95:80] &= \text{SRC2}[63:48] + \text{SRC2}[47:32];
\end{align*}
\]}

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PHADDW/PHADDD — Packed Horizontal Add

**DEST[111:96]** ← **SRC2[95:80] + SRC2[79:64]**
**DEST[127:112]** ← **SRC2[127:112] + SRC2[111:96]**
**DEST[VLMAX-1:128]** ← 0

**VPHADDD (VEX.128 encoded version)**
**DEST[31-0]** ← **SRC1[63-32] + SRC1[31-0]**
**DEST[63-32]** ← **SRC1[127-96] + SRC1[95-64]**
**DEST[95-64]** ← **SRC2[63-32] + SRC2[31-0]**
**DEST[127-96]** ← **SRC2[127-96] + SRC2[95-64]**
**DEST[VLMAX-1:128]** ← 0

**Intel C/C++ Compiler Intrinsic Equivalents**

**PHADDW:** __m64 _mm_hadd_pi16 (__m64 a, __m64 b)
**PHADDW:** __m128i _mm_hadd_epi16 (__m128i a, __m128i b)
**PHADDD:** __m64 _mm_hadd_pi32 (__m64 a, __m64 b)
**PHADDD:** __m128i _mm_hadd_epi32 (__m128i a, __m128i b)

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 4; additionally

#UD If VEX.L = 1.
INSTRUCTION SET REFERENCE, M-Z

PHADDSW — Packed Horizontal Add and Saturate

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 03 /r&lt;sup&gt;1&lt;/sup&gt; PHADDSW mm1, mm2/m64</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Add 16-bit signed integers horizontally, pack saturated integers to MM1.</td>
<td></td>
</tr>
<tr>
<td>66 0F 38 03 /r PHADDSW xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Add 16-bit signed integers horizontally, pack saturated integers to XMM1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 03 /r VPHADDSW xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Add 16-bit signed integers horizontally, pack saturated integers to xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>RVM ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

Description

PHADDSW adds two adjacent signed 16-bit integers horizontally from the source and destination operands and saturates the signed results; packs the signed, saturated 16-bit results to the destination operand (first operand) Both operands can be MMX or XMM registers. When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

PHADDSW (with 64-bit operands)
**PHADDSW** (with 128-bit operands)

\[
\begin{align*}
\text{mm1}[15:0] &= \text{SaturateToSignedWord}(\text{mm1}[31:16] + \text{mm1}[15:0]); \\
\text{mm1}[31:16] &= \text{SaturateToSignedWord}(\text{mm1}[63:48] + \text{mm1}[47:32]); \\
\text{mm1}[47:32] &= \text{SaturateToSignedWord}(\text{mm2/m64}[31:16] + \text{mm2/m64}[15:0]); \\
\text{mm1}[63:48] &= \text{SaturateToSignedWord}(\text{mm2/m64}[63:48] + \text{mm2/m64}[47:32]); \\
\end{align*}
\]

**VPHADDSW** (VEX.128 encoded version)

\[
\begin{align*}
\text{DEST}[15:0] &= \text{SaturateTo SignedWord}(\text{SRC1}[31:16] + \text{SRC1}[15:0]); \\
\text{DEST}[31:16] &= \text{SaturateTo SignedWord}(\text{SRC1}[63:48] + \text{SRC1}[47:32]); \\
\text{DEST}[47:32] &= \text{SaturateTo SignedWord}(\text{SRC1}[95:80] + \text{SRC1}[79:64]); \\
\text{DEST}[63:48] &= \text{SaturateTo SignedWord}(\text{SRC2/m128}[31:16] + \text{SRC2/m128}[15:0]); \\
\text{DEST}[79:64] &= \text{SaturateTo SignedWord}(\text{SRC2/m128}[63:48] + \text{SRC2/m128}[47:32]); \\
\text{DEST}[95:80] &= \text{SaturateTo SignedWord}(\text{SRC2/m128}[95:80] + \text{SRC2/m128}[79:64]); \\
\text{DEST}[111:96] &= \text{SaturateTo SignedWord}(\text{SRC2/m128}[127:112] + \text{SRC2/m128}[111:96]); \\
\text{DEST}[127:112] &= \text{SaturateToSignedWord}(\text{mm2/m128}[127:112] + \text{mm2/m128}[111:96]); \\
\text{DEST}[\text{VLMAX}-1:128] &\leftarrow 0
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

\[
\begin{align*}
\text{PHADDSW:} & \quad \text{__m64 } \_\text{mm_hadds_pi16 }(_\text{__m64 } a, _\text{__m64 } b) \\
\text{PHADDSW:} & \quad \text{__m128i } \_\text{mm_hadds_epi16 }(_\text{__m128i } a, _\text{__m128i } b)
\end{align*}
\]

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

\#UD If VEX.L = 1.
INSTRUCTION SET REFERENCE, M-Z

PHMINPOSUW — Packed Horizontal Word Minimum

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 41 /r PHMINPOSUW xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Find the minimum unsigned word in xmm2/m128 and place its value in the low word of xmm1 and its index in the second-lowest word of xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 41 /r VPPHMINPOSUW xmm1, xmm2/m128</td>
<td>RM V/V AVX</td>
<td></td>
<td>Find the minimum unsigned word in xmm2/m128 and place its value in the low word of xmm1 and its index in the second-lowest word of xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction Operand Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Op/En Operand 1 Operand 2 Operand 3 Operand 4</td>
</tr>
<tr>
<td>RM ModRM:reg (w) ModRM:r/m (r) NA NA</td>
</tr>
</tbody>
</table>

**Description**

Determine the minimum unsigned word value in the source operand (second operand) and place the unsigned word in the low word (bits 0-15) of the destination operand (first operand). The word index of the minimum value is stored in bits 16-18 of the destination operand. The remaining upper bits of the destination are set to zero.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

PHMINPOSUW (128-bit Legacy SSE version)

INDEX ← 0;
MIN ← SRC[15:0];
IF (SRC[31:16] < MIN)
    THEN INDEX ← 1; MIN ← SRC[31:16]; FI;
IF (SRC[47:32] < MIN)
THEN INDEX ← 2; MIN ← SRC[47:32]; Fl;
* Repeat operation for words 3 through 6
IF (SRC[127:112] < MIN)
   THEN INDEX ← 7; MIN ← SRC[127:112]; Fl;
DEST[15:0] ← MIN;
DEST[18:16] ← INDEX;
DEST[127:19] ← 0000000000000000000000000000H;

VPHMINPOSUw (VEX.128 encoded version)
INDEX ← 0
MIN ← SRC[15:0]
IF (SRC[31:16] < MIN) THEN INDEX ← 1; MIN ← SRC[31:16]
IF (SRC[47:32] < MIN) THEN INDEX ← 2; MIN ← SRC[47:32]
* Repeat operation for words 3 through 6
IF (SRC[127:112] < MIN) THEN INDEX ← 7; MIN ← SRC[127:112]
DEST[15:0] ← MIN
DEST[18:16] ← INDEX
DEST[127:19] ← 0000000000000000000000000000H
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent

PHMINPOSUw: __m128i _mm_minpos_epu16(__m128i packed_words);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
   If VEX.vvvv != 111B.
PHSUBW/PHSUBD — Packed Horizontal Subtract

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 05 /r&lt;sup&gt;1&lt;/sup&gt; PHSUBW mm1, mm2/m64</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Subtract 16-bit signed integers horizontally, pack to MM1.</td>
<td></td>
</tr>
<tr>
<td>66 0F 38 05 /r PHSUBW xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Subtract 16-bit signed integers horizontally, pack to XMM1.</td>
<td></td>
</tr>
<tr>
<td>0F 38 06 /r PHSUBD mm1, mm2/m64</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Subtract 32-bit signed integers horizontally, pack to MM1.</td>
<td></td>
</tr>
<tr>
<td>66 0F 38 06 /r PHSUBD xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Subtract 32-bit signed integers horizontally, pack to XMM1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 05 /r VPHSUBW xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Subtract 16-bit signed integers horizontally, pack to xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 06 /r VPHSUBD xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Subtract 32-bit signed integers horizontally, pack to xmm1.</td>
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NOTES:

Instruction Operand Encoding

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<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (r, w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

PHSUBW performs horizontal subtraction on each adjacent pair of 16-bit signed integers by subtracting the most significant word from the least significant word of each pair in the source and destination operands, and packs the signed 16-bit results to the destination operand (first operand). PHSUBD performs horizontal subtraction on each adjacent pair of 32-bit signed integers by subtracting the most significant doubleword from the least significant doubleword of each pair, and packs the signed...
32-bit result to the destination operand. Both operands can be MMX or XMM registers. When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

**PHSUBW (with 64-bit operands)**

\[
\begin{align*}
\text{mm1}[15-0] &= \text{mm1}[15-0] - \text{mm1}[31-16]; \\
\text{mm1}[31-16] &= \text{mm1}[47-32] - \text{mm1}[63-48]; \\
\text{mm1}[47-32] &= \text{mm2}/\text{m64}[15-0] - \text{mm2}/\text{m64}[31-16]; \\
\text{mm1}[63-48] &= \text{mm2}/\text{m64}[47-32] - \text{mm2}/\text{m64}[63-48];
\end{align*}
\]

**PHSUBW (with 128-bit operands)**

\[
\begin{align*}
\text{xmm1}[15-0] &= \text{xmm1}[15-0] - \text{xmm1}[31-16]; \\
\text{xmm1}[31-16] &= \text{xmm1}[47-32] - \text{xmm1}[63-48]; \\
\text{xmm1}[47-32] &= \text{xmm1}[79-64] - \text{xmm1}[95-80]; \\
\text{xmm1}[63-48] &= \text{ xmm1}[111-96] - \text{xmm1}[127-112]; \\
\text{xmm1}[79-64] &= \text{ xmm2}/\text{m128}[15-0] - \text{xmm2}/\text{m128}[31-16]; \\
\text{xmm1}[95-80] &= \text{ xmm2}/\text{m128}[47-32] - \text{xmm2}/\text{m128}[63-48]; \\
\text{xmm1}[111-96] &= \text{ xmm2}/\text{m128}[79-64] - \text{xmm2}/\text{m128}[95-80]; \\
\text{xmm1}[127-112] &= \text{ xmm2}/\text{m128}[111-96] - \text{ xmm2}/\text{m128}[127-112];
\end{align*}
\]

**PHSUBD (with 64-bit operands)**

\[
\begin{align*}
\text{mm1}[31-0] &= \text{mm1}[31-0] - \text{mm1}[63-32]; \\
\text{mm1}[63-32] &= \text{mm2}/\text{m64}[31-0] - \text{mm2}/\text{m64}[63-32];
\end{align*}
\]

**PHSUBD (with 128-bit operands)**

\[
\begin{align*}
\text{xmm1}[31-0] &= \text{xmm1}[31-0] - \text{xmm1}[63-32]; \\
\text{xmm1}[63-32] &= \text{xmm1}[95-64] - \text{ xmm1}[127-96]; \\
\text{xmm1}[95-64] &= \text{ xmm2}/\text{m128}[31-0] - \text{xmm2}/\text{m128}[63-32]; \\
\text{xmm1}[127-96] &= \text{ xmm2}/\text{m128}[95-64] - \text{ xmm2}/\text{m128}[127-96];
\end{align*}
\]

**VPHSUBW (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[15:0] &\leftarrow \text{SRC1}[15:0] - \text{SRC1}[31:16] \\
\text{DEST}[31:16] &\leftarrow \text{SRC1}[47:32] - \text{SRC1}[63:48] \\
\text{DEST}[47:32] &\leftarrow \text{SRC1}[79:64] - \text{SRC1}[95:80] \\
\text{DEST}[63:48] &\leftarrow \text{SRC1}[111:96] - \text{SRC1}[127:112]
\end{align*}
\]
DEST[79:64] ← SRC2[15:0] - SRC2[31:16]
DEST[111:96] ← SRC2[79:64] - SRC2[95:80]
DEST[VLMAX-1:128] ← 0

VPHSUBD (VEX.128 encoded version)
DEST[31-0] ← SRC1[31-0] - SRC1[63-32]
DEST[63-32] ← SRC1[95-64] - SRC1[127-96]
DEST[95-64] ← SRC2[31-0] - SRC2[63-32]
DEST[127-96] ← SRC2[95-64] - SRC2[127-96]
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalents**

PHSUBW:  __m64 _mm_hsub_pi16 (__m64 a, __m64 b)
PHSUBW:  __m128i _mm_hsub_epi16 (__m128i a, __m128i b)
PHSUBD:  __m64 _mm_hsub_pi32 (__m64 a, __m64 b)
PHSUBD:  __m128i _mm_hsub_epi32 (__m128i a, __m128i b)

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PHSUBSW — Packed Horizontal Subtract and Saturate

**Opcode/Instruction**

<table>
<thead>
<tr>
<th>Opcode/En</th>
<th>ModRM:reg (r, w)</th>
<th>ModRM:r/m (r)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 38 07 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM</td>
<td>V/V</td>
</tr>
<tr>
<td>66 OF 38 07 /r</td>
<td>RM</td>
<td>V/V</td>
</tr>
<tr>
<td>VEX.NDS.128:66.0F38.WIG 07 /r</td>
<td>RVM</td>
<td>V/V</td>
</tr>
<tr>
<td>VPUSHUBSW xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
</tr>
</tbody>
</table>

**Description**

PHSUBSW performs horizontal subtraction on each adjacent pair of 16-bit signed integers by subtracting the most significant word from the least significant word of each pair in the source and destination operands. The signed, saturated 16-bit results are packed to the destination operand (first operand). Both operands can be MMX or XMM register. When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**NOTES:**


**Instruction Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (r, w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

PHSUBSW performs horizontal subtraction on each adjacent pair of 16-bit signed integers by subtracting the most significant word from the least significant word of each pair in the source and destination operands. The signed, saturated 16-bit results are packed to the destination operand (first operand). Both operands can be MMX or XMM register. When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.
INSTRUCTION SET REFERENCE, M-Z

Operation

**PHSUBSW (with 64-bit operands)**

- \( mm1[15-0] = \text{SaturateToSignedWord}(mm1[15-0] - mm1[31-16]); \)
- \( mm1[31-16] = \text{SaturateToSignedWord}(mm1[47-32] - mm1[63-48]); \)
- \( mm1[47-32] = \text{SaturateToSignedWord}(mm2/m64[15-0] - mm2/m64[31-16]); \)
- \( mm1[63-48] = \text{SaturateToSignedWord}(mm2/m64[47-32] - mm2/m64[63-48]); \)

**PHSUBSW (with 128-bit operands)**

- \( xmm1[15-0] = \text{SaturateToSignedWord}(xmm1[15-0] - xmm1[31-16]); \)
- \( xmm1[31-16] = \text{SaturateToSignedWord}(xmm1[47-32] - xmm1[63-48]); \)
- \( xmm1[47-32] = \text{SaturateToSignedWord}(xmm1[79-64] - xmm1[95-80]); \)
- \( xmm1[63-48] = \text{SaturateToSignedWord}(xmm1[111-96] - xmm1[127-112]); \)
- \( xmm1[79-64] = \text{SaturateToSignedWord}(xmm2/m128[15-0] - xmm2/m128[31-16]); \)
- \( xmm1[95-80] = \text{SaturateToSignedWord}(xmm2/m128[47-32] - xmm2/m128[63-48]); \)
- \( xmm1[111-96] = \text{SaturateToSignedWord}(xmm2/m128[79-64] - xmm2/m128[95-80]); \)
- \( xmm1[127-112] = \text{SaturateToSignedWord}(xmm2/m128[111-96] - xmm2/m128[127-112]); \)

**VPHSUBSW (VEX.128 encoded version)**

- \( \text{DEST}[15:0] = \text{SaturateToSignedWord}(\text{SRC1}[15:0] - \text{SRC1}[31:16]); \)
- \( \text{DEST}[31:16] = \text{SaturateToSignedWord}(\text{SRC1}[47:32] - \text{SRC1}[63:48]); \)
- \( \text{DEST}[47:32] = \text{SaturateToSignedWord}(\text{SRC1}[79:64] - \text{SRC1}[95:80]); \)
- \( \text{DEST}[63:48] = \text{SaturateToSignedWord}(\text{SRC1}[111:96] - \text{SRC1}[127:112]); \)
- \( \text{DEST}[79:64] = \text{SaturateToSignedWord}(\text{SRC2}[15:0] - \text{SRC2}[31:16]); \)
- \( \text{DEST}[95:80] = \text{SaturateToSignedWord}(\text{SRC2}[47:32] - \text{SRC2}[63:48]); \)
- \( \text{DEST}[111:96] = \text{SaturateToSignedWord}(\text{SRC2}[79:64] - \text{SRC2}[95:80]); \)
- \( \text{DEST}[127:112] = \text{SaturateToSignedWord}(\text{SRC2}[111:96] - \text{SRC2}[127:112]); \)

- \( \text{DEST}[\text{VLMAX}-1:128] \leftarrow 0 \)

**Intel C/C++ Compiler Intrinsic Equivalent**

- \( \text{PHSUBSW: } _\text{__m64 } \_\text{mm_hsubs_pi16}(\_\text{m64 } a, \_\text{m64 } b) \)
- \( \text{PHSUBSW: } _\text{__m128i } \_\text{mm_hsubs_epi16}(\_\text{m128i } a, \_\text{m128i } b) \)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

- \#UD If \( \text{VEX.L} = 1 \).
**INSTRUCTION SET REFERENCE, M-Z**

**PINSRB/PINSRD/PINSRQ — Insert Byte/Dword/Qword**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 20 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Insert a byte integer value from r32/m8 into xmm1 at the destination element in xmm1 specified by imm8.</td>
</tr>
<tr>
<td>PINSRB xmm1, r32/m8, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 3A 22 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Insert a dword integer value from r/m32 into the xmm1 at the destination element specified by imm8.</td>
</tr>
<tr>
<td>PINSRD xmm1, r/m32, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 REX.W 0F 3A 22 /r ib</td>
<td>RMI</td>
<td>N. E./V</td>
<td>SSE4_1</td>
<td>Insert a qword integer value from r/m32 into the xmm1 at the destination element specified by imm8.</td>
</tr>
<tr>
<td>PINSRQ xmm1, r/m64, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.W0 20 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Merge a byte integer value from r32/m8 and rest from xmm2 into xmm1 at the byte offset in imm8.</td>
</tr>
<tr>
<td>VPINSRB xmm1, xmm2, r32/m8, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.W0 22 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Insert a dword integer value from r32/m32 and rest from xmm2 into xmm1 at the dword offset in imm8.</td>
</tr>
<tr>
<td>VPINSRD xmm1, xmm2, r32/m32, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F3A.W1 22 /r ib</td>
<td>RVMI</td>
<td>V/I</td>
<td>AVX</td>
<td>Insert a qword integer value from r64/m64 and rest from xmm2 into xmm1 at the qword offset in imm8.</td>
</tr>
<tr>
<td>VPINSRQ xmm1, xmm2, r64/m64, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. In 64-bit mode, VEX.W1 is ignored for VPINSRB (similar to legacy REX.W=1 prefix with PINSRB).

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRMreg (w)</td>
<td>ModRMtr/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMtr/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

**Description**

Copies a byte/dword/qword from the source operand (second operand) and inserts it in the destination operand (first operand) at the location specified with the count operand (third operand). (The other elements in the destination register are left untouched.) The source operand can be a general-purpose register or a memory.
location. (When the source operand is a general-purpose register, PINSRB copies the low byte of the register.) The destination operand is an XMM register. The count operand is an 8-bit immediate. When specifying a qword[dword, byte] location in an XMM register, the [2, 4] least-significant bit(s) of the count operand specify the location.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15, R8-15). Use of REX.W permits the use of 64 bit general purpose registers.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD. Attempt to execute VPINSRQ in non-64-bit mode will cause #UD.

**Operation**

CASE OF

PINSRB: SEL ← COUNT[3:0];
MASK ← (0FH << (SEL * 8));
TEMP ← ((SRC[7:0] << (SEL * 8)) AND MASK);

PINSRD: SEL ← COUNT[1:0];
MASK ← (0FFFFFFFH << (SEL * 32));
TEMP ← ((SRC << (SEL * 32)) AND MASK);

PINSRQ: SEL ← COUNT[0]
MASK ← (0FFFFFFFFFFFFFFFFH << (SEL * 64));
TEMP ← ((SRC << (SEL * 32)) AND MASK);

ESAC;
DEST ← ((DEST AND NOT MASK) OR TEMP);

**VPINSRB (VEX.128 encoded version)**

SEL ← imm8[3:0]
DEST[127:0] ← write_b_element(SEL, SRC2, SRC1)
DEST[VLMAX-1:128] ← 0

**VPINSRD (VEX.128 encoded version)**

SEL ← imm8[1:0]
DEST[127:0] ← write_d_element(SEL, SRC2, SRC1)
DEST[VLMAX-1:128] ← 0

**VPINSRQ (VEX.128 encoded version)**

SEL ← imm8[0]
DEST[127:0] ← write_q_element(SEL, SRC2, SRC1)
DEST[VLMAX-1:128] ← 0
Intel C/C++ Compiler Intrinsic Equivalent

PINSRB: __m128i _mm_insert_epi8 (__m128i s1, int s2, const int ndx);
PINSRD: __m128i _mm_insert_epi32 (__m128i s2, int s, const int ndx);
PINSRQ: __m128i _mm_insert_epi64(__m128i s2, __int64 s, const int ndx);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD If VEX.L = 1.
    If VPINSRQ in non-64-bit mode with VEX.W=1.
PINSRW—Insert Word

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C4 /r ib&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE</td>
<td>Insert the low word from r32 or from m16 into mm at the word position specified by imm8.</td>
</tr>
<tr>
<td>PINSRW mm, r32/m16, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F C4 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move the low word of r32 or from m16 into xmm at the word position specified by imm8.</td>
</tr>
<tr>
<td>PINSRW xmm, r32/m16, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.W0 C4 /r ib</td>
<td>RVMI</td>
<td>V2/V</td>
<td>AVX</td>
<td>Insert a word integer value from r32/m16 and rest from xmm2 into xmm1 at the word offset in imm8.</td>
</tr>
<tr>
<td>VPINSRW xmm1, xmm2, r32/m16, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:


2. In 64-bit mode, VEX.W1 is ignored for VPINSRW (similar to legacy REX.W=1 prefix in PINSRW).

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Copies a word from the source operand (second operand) and inserts it in the destination operand (first operand) at the location specified with the count operand (third operand). (The other words in the destination register are left untouched.) The source operand can be a general-purpose register or a 16-bit memory location. (When the source operand is a general-purpose register, the low word of the register is copied.) The destination operand can be an MMX technology register or an XMM register. The count operand is an 8-bit immediate. When specifying a word location in an MMX technology register, the 2 least-significant bits of the count operand specify the location; for an XMM register, the 3 least-significant bits specify the location.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15, R8-15).
128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

PINSRW (with 64-bit source operand)

\[
\text{SEL} \leftarrow \text{COUNT \ AND \ 3H}; \\
\text{CASE (Determine word position) OF} \\
\text{SEL} \leftarrow 0: \ \text{MASK} \leftarrow 000000000000FFFFH; \\
\text{SEL} \leftarrow 1: \ \text{MASK} \leftarrow 0000000000000000FFFFH; \\
\text{SEL} \leftarrow 2: \ \text{MASK} \leftarrow 00000000000000000000FFFFH; \\
\text{SEL} \leftarrow 3: \ \text{MASK} \leftarrow FFF00000000000000000000000000H; \\
\text{DEST} \leftarrow (\text{DEST \ AND \ NOT \ MASK}) \ \text{OR} \ ((\text{SRC} << (\text{SEL} \ \ast \ 16)) \ \text{AND} \ \text{MASK}); \\
\]

PINSRW (with 128-bit source operand)

\[
\text{SEL} \leftarrow \text{COUNT \ AND \ 7H}; \\
\text{CASE (Determine word position) OF} \\
\text{SEL} \leftarrow 0: \ \text{MASK} \leftarrow 0000000000000000000000000000FFFFH; \\
\text{SEL} \leftarrow 1: \ \text{MASK} \leftarrow 000000000000000000000000FFFF0000H; \\
\text{SEL} \leftarrow 2: \ \text{MASK} \leftarrow 00000000000000000000FFFF00000000H; \\
\text{SEL} \leftarrow 3: \ \text{MASK} \leftarrow 000000000000000000FFFF0000000000H; \\
\text{SEL} \leftarrow 4: \ \text{MASK} \leftarrow 000000000000FFFF0000000000000000H; \\
\text{SEL} \leftarrow 5: \ \text{MASK} \leftarrow 00000000FFFF0000000000000000000H; \\
\text{SEL} \leftarrow 6: \ \text{MASK} \leftarrow 000FFFF000000000000000000000000H; \\
\text{SEL} \leftarrow 7: \ \text{MASK} \leftarrow FFFF000000000000000000000000000H; \\
\text{DEST} \leftarrow (\text{DEST \ AND \ NOT \ MASK}) \ \text{OR} \ ((\text{SRC} << (\text{SEL} \ \ast \ 16)) \ \text{AND} \ \text{MASK}); \\
\]

VPINSRW (VEX.128 encoded version)

\[
\text{SEL} \leftarrow \text{imm8}[2:0] \\
\text{DEST}[127:0] \leftarrow \text{write}_w\text{element}(\text{SEL}, \text{SRC2, SRC1}) \\
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0 \\
\]

Intel C/C++ Compiler Intrinsic Equivalent

PINSRW: \_m64 \_mm\_insert\_pi16 (\_m64 a, int d, int n)
PINSRW: \_m128i \_mm\_insert\_epi16 (\_m128i a, int b, int imm)

Flags Affected

None.
Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD If VEX.L = 1.
   If VPINSRW in non-64-bit mode with VEX.W=1.
**PMADDUBSW — Multiply and Add Packed Signed and Unsigned Bytes**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 04 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Multiply signed and unsigned bytes, add horizontal pair of signed words, pack saturated signed-words to MM1.</td>
</tr>
<tr>
<td>PMADDUBSW mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 38 04 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Multiply signed and unsigned bytes, add horizontal pair of signed words, pack saturated signed-words to XMM1.</td>
</tr>
<tr>
<td>PMADDUBSW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 04 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply signed and unsigned bytes, add horizontal pair of signed words, pack saturated signed-words to xmm1.</td>
</tr>
<tr>
<td>VPMADDUBSW xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMreg/r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

PMADDUBSW multiplies vertically each unsigned byte of the destination operand (first operand) with the corresponding signed byte of the source operand (second operand), producing intermediate signed 16-bit integers. Each adjacent pair of signed words is added and the saturated result is packed to the destination operand. For example, the lowest-order bytes (bits 7-0) in the source and destination operands are multiplied and the intermediate signed word result is added with the corresponding intermediate result from the 2nd lowest-order bytes (bits 15-8) of the operands; the sign-saturated result is stored in the lowest word of the destination register (15-0). The same operation is performed on the other pairs of adjacent bytes. Both operands can be MMX register or XMM registers. When the source
operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PMADDUBSW (with 64 bit operands)**

\[
\begin{align*}
\text{DEST}[15-0] &= \text{SaturateToSignedWord} (\text{SRC}[15-8] \times \text{DEST}[15-8] + \text{SRC}[7-0] \times \text{DEST}[7-0]); \\
\text{DEST}[31-16] &= \text{SaturateToSignedWord} (\text{SRC}[31-24] \times \text{DEST}[31-24] + \text{SRC}[23-16] \times \text{DEST}[23-16]); \\
\text{DEST}[47-32] &= \text{SaturateToSignedWord} (\text{SRC}[47-40] \times \text{DEST}[47-40] + \text{SRC}[39-32] \times \text{DEST}[39-32]); \\
\text{DEST}[63-48] &= \text{SaturateToSignedWord} (\text{SRC}[63-56] \times \text{DEST}[63-56] + \text{SRC}[55-48] \times \text{DEST}[55-48]); \\
\end{align*}
\]

**PMADDUBSW (with 128 bit operands)**

\[
\begin{align*}
\text{DEST}[15-0] &= \text{SaturateToSignedWord} (\text{SRC}[15-8] \times \text{DEST}[15-8] + \text{SRC}[7-0] \times \text{DEST}[7-0]); \\
&\text{ Repeat operation for 2nd through 7th word} \\
\text{SRC1/DEST}[127-112] &= \text{SaturateToSignedWord} (\text{SRC}[127-120] \times \text{SRC1}[127-120] + \text{SRC}[119-112] \times \text{DEST}[119-112]); \\
\end{align*}
\]

**VPMADDUBSW (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[15:0] &\leftarrow \text{SaturateToSignedWord} (\text{SRC2}[15:8] \times \text{SRC1}[15:8] + \text{SRC2}[7:0] \times \text{SRC1}[7:0]) \\
&\text{ Repeat operation for 2nd through 7th word} \\
\text{DEST}[127:112] &\leftarrow \text{SaturateToSignedWord} (\text{SRC2}[127:120] \times \text{SRC1}[127:120] + \text{SRC2}[119:112] \times \\
&\text{SRC1}[119:112]); \\
\text{DEST}[VLMAX-1:128] &\leftarrow 0
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalents**

\[
\begin{align*}
\text{PMADDUBSW: } &\_m64\_\text{mm}_maddubs\_pi16 (\_m64\ a, \_m64\ b) \\
\text{PMADDUBSW: } &\_m128\_\text{mm}_maddubs\_epi16 (\_m128i\ a, \_m128i\ b)
\end{align*}
\]

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

\[#UD\] If VEX.L = 1.
PMADDWD—Multiply and Add Packed Integers

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit</th>
<th>Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF F5 /r(^3)</td>
<td>RM</td>
<td>V/V</td>
<td>V/V</td>
<td>MMX</td>
<td>Multiply the packed words in \textit{mm} by the packed words in \textit{mm/m64}, add adjacent doubleword results, and store in \textit{mm}.</td>
</tr>
<tr>
<td>PMADDWD mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF F5 /r</td>
<td>RM</td>
<td>V/V</td>
<td>V/V</td>
<td>SSE2</td>
<td>Multiply the packed word integers in \textit{xmm1} by the packed word integers in \textit{xmm2/m128}, add adjacent doubleword results, and store in \textit{xmm1}.</td>
</tr>
<tr>
<td>PMADDWD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG F5 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply the packed word integers in \textit{xmm2} by the packed word integers in \textit{xmm3/m128}, add adjacent doubleword results, and store in \textit{xmm1}.</td>
</tr>
<tr>
<td>VPMADDWD xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

### Instruction Operand Encoding

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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Multiplies the individual signed words of the destination operand (first operand) by the corresponding signed words of the source operand (second operand), producing temporary signed, doubleword results. The adjacent doubleword results are then summed and stored in the destination operand. For example, the corresponding low-order words (15-0) and (31-16) in the source and destination operands are multiplied by one another and the doubleword results are added together and stored in the low doubleword of the destination register (31-0). The same operation is performed on the other pairs of adjacent words. (Figure 4-6 shows this operation when using 64-bit operands.) The source operand can be an MMX technology register.
or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

The PMADDWD instruction wraps around only in one situation: when the 2 pairs of words being operated on in a group are all 8000H. In this case, the result wraps around to 80000000H.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Figure 4-6. PMADDWD Execution Model Using 64-bit Operands**

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>TEMP</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>X3</td>
<td>Y3</td>
<td>X3 * Y3</td>
<td>(X3<em>Y3) + (X2</em>Y2)</td>
</tr>
<tr>
<td>X2</td>
<td>Y2</td>
<td>X2 * Y2</td>
<td>(X1<em>Y1) + (X0</em>Y0)</td>
</tr>
<tr>
<td>X1</td>
<td>Y1</td>
<td>X1 * Y1</td>
<td></td>
</tr>
<tr>
<td>X0</td>
<td>Y0</td>
<td>X0 * Y0</td>
<td></td>
</tr>
</tbody>
</table>

**Operation**

**PMADDWD (with 64-bit operands)**

\[
\text{DEST}[31:0] \leftarrow (\text{DEST}[15:0] \times \text{SRC}[15:0]) + (\text{DEST}[31:16] \times \text{SRC}[31:16]); \\
\text{DEST}[63:32] \leftarrow (\text{DEST}[47:32] \times \text{SRC}[47:32]) + (\text{DEST}[63:48] \times \text{SRC}[63:48]);
\]

**PMADDWD (with 128-bit operands)**

\[
\text{DEST}[31:0] \leftarrow (\text{DEST}[15:0] \times \text{SRC}[15:0]) + (\text{DEST}[31:16] \times \text{SRC}[31:16]); \\
\text{DEST}[63:32] \leftarrow (\text{DEST}[47:32] \times \text{SRC}[47:32]) + (\text{DEST}[63:48] \times \text{SRC}[63:48]); \\
\text{DEST}[95:64] \leftarrow (\text{DEST}[79:64] \times \text{SRC}[79:64]) + (\text{DEST}[95:80] \times \text{SRC}[95:80]); \\
\text{DEST}[127:96] \leftarrow (\text{DEST}[111:96] \times \text{SRC}[111:96]) + (\text{DEST}[127:112] \times \text{SRC}[127:112]);
\]

**VPMADDWD (VEX.128 encoded version)**

\[
\text{DEST}[31:0] \leftarrow (\text{SRC}[15:0] \times \text{SRC2}[15:0]) + (\text{SRC}[31:16] \times \text{SRC2}[31:16]) \\
\text{DEST}[63:32] \leftarrow (\text{SRC}[47:32] \times \text{SRC2}[47:32]) + (\text{SRC}[63:48] \times \text{SRC2}[63:48]) \\
\text{DEST}[95:64] \leftarrow (\text{SRC}[79:64] \times \text{SRC2}[79:64]) + (\text{SRC}[95:80] \times \text{SRC2}[95:80]) \\
\text{DEST}[127:96] \leftarrow (\text{SRC}[111:96] \times \text{SRC2}[111:96]) + (\text{SRC}[127:112] \times \text{SRC2}[127:112]) \\
\text{DEST}[VLMAX-1:128] \leftarrow 0
\]
PMADDWD—Multiply and Add Packed Integers

**Intel C/C++ Compiler Intrinsic Equivalent**

PMADDWD:  

```
__m64 _mm_madd_pi16(__m64 m1, __m64 m2)
```

PMADDWD:  

```
__m128i _mm_madd_epi16 ( __m128i a, __m128i b)
```

**Flags Affected**

None.

**Numeric Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

```
#UD              If VEX.L = 1.
```
INSTRUCTION SET REFERENCE, M-Z

PMAXSB — Maximum of Packed Signed Byte Integers

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 3C /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Compare packed signed byte integers in xmm1 and xmm2/m128 and store packed maximum values in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 3C /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed signed byte integers in xmm2 and xmm3/m128 and store packed maximum values in xmm1.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Compares packed signed byte integers in the destination operand (first operand) and the source operand (second operand), and returns the maximum for each packed value in the destination operand.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

IF (DEST[7:0] > SRC[7:0])
THEN DEST[7:0] ← DEST[7:0];
ELSE DEST[7:0] ← SRC[7:0]; Flt;
IF (DEST[15:8] > SRC[15:8])
THEN DEST[15:8] ← DEST[15:8];
ELSE DEST[15:8] ← SRC[15:8]; Flt;
IF (DEST[23:16] > SRC[23:16])
THEN DEST[23:16] ← DEST[23:16];
ELSE DEST[23:16] ← SRC[23:16]; Flt;
IF (DEST[31:24] > SRC[31:24])
THEN DEST[31:24] ← DEST[31:24];
ELSE DEST[31:24] ← SRC[31:24]; Flt;
THEN DEST[31:24] ← DEST[31:24];
ELSE DEST[31:24] ← SRC[31:24]; FI;


IF (DEST[47:40] > SRC[47:40])
    THEN DEST[47:40] ← DEST[47:40];
    ELSE DEST[47:40] ← SRC[47:40]; FI;

IF (DEST[55:48] > SRC[55:48])
    ELSE DEST[55:48] ← SRC[55:48]; FI;

IF (DEST[63:56] > SRC[63:56])
    THEN DEST[63:56] ← DEST[63:56];
    ELSE DEST[63:56] ← SRC[63:56]; FI;

IF (DEST[71:64] > SRC[71:64])
    THEN DEST[71:64] ← DEST[71:64];
    ELSE DEST[71:64] ← SRC[71:64]; FI;

IF (DEST[79:72] > SRC[79:72])
    THEN DEST[79:72] ← DEST[79:72];
    ELSE DEST[79:72] ← SRC[79:72]; FI;

IF (DEST[87:80] > SRC[87:80])
    THEN DEST[87:80] ← DEST[87:80];
    ELSE DEST[87:80] ← SRC[87:80]; FI;

IF (DEST[95:88] > SRC[95:88])
    THEN DEST[95:88] ← DEST[95:88];
    ELSE DEST[95:88] ← SRC[95:88]; FI;

IF (DEST[103:96] > SRC[103:96])
    THEN DEST[103:96] ← DEST[103:96];
    ELSE DEST[103:96] ← SRC[103:96]; FI;

IF (DEST[111:104] > SRC[111:104])
    THEN DEST[111:104] ← DEST[111:104];
    ELSE DEST[111:104] ← SRC[111:104]; FI;

IF (DEST[119:112] > SRC[119:112])
    THEN DEST[119:112] ← DEST[119:112];
    ELSE DEST[119:112] ← SRC[119:112]; FI;

IF (DEST[127:120] > SRC[127:120])
    THEN DEST[127:120] ← DEST[127:120];
    ELSE DEST[127:120] ← SRC[127:120]; FI;

**VPMAXSB (VEX.128 encoded version)**

IF SRC[1:0] > SRC[1:0] THEN
    DEST[7:0] ← SRC[7:0];
ELSE
INSTRUCTION SET REFERENCE, M-Z

DEST[7:0] ← SRC2[7:0]; Fi;
(* Repeat operation for 2nd through 15th bytes in source and destination operands *)
IF SRC1[127:120] > SRC2[127:120] THEN
    DEST[127:120] ← SRC1[127:120];
ELSE
    DEST[127:120] ← SRC2[127:120]; Fi;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent

PMAXSB: __m128i _mm_max_epi8 (__m128i a, __m128i b);

Flags Affected

None.

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 4; additionally

#UD If VEX.L = 1.
PMAXSD — Maximum of Packed Signed Dword Integers

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 3D /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Compare packed signed dword integers in xmm1 and xmm2/m128 and store packed maximum values in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 3D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed signed dword integers in xmm2 and xmm3/m128 and store packed maximum values in xmm1.</td>
</tr>
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<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
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<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Comparates packed signed dword integers in the destination operand (first operand) and the source operand (second operand), and returns the maximum for each packed value in the destination operand.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:1288) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

### Operation

\[
\begin{align*}
&\text{IF} (\text{DEST}[31:0] > \text{SRC}[31:0]) \\
&\quad \text{THEN} \text{DEST}[31:0] \leftarrow \text{DEST}[31:0]; \\
&\quad \text{ELSE} \text{DEST}[31:0] \leftarrow \text{SRC}[31:0]; \text{Fl}; \\
&\text{IF} (\text{DEST}[63:32] > \text{SRC}[63:32]) \\
&\quad \text{THEN} \text{DEST}[63:32] \leftarrow \text{DEST}[63:32]; \\
&\quad \text{ELSE} \text{DEST}[63:32] \leftarrow \text{SRC}[63:32]; \text{Fl}; \\
&\text{IF} (\text{DEST}[95:64] > \text{SRC}[95:64]) \\
&\quad \text{THEN} \text{DEST}[95:64] \leftarrow \text{DEST}[95:64]; \\
&\quad \text{ELSE} \text{DEST}[95:64] \leftarrow \text{SRC}[95:64]; \text{Fl}; \\
&\text{IF} (\text{DEST}[127:96] > \text{SRC}[127:96]) \\
&\quad \text{THEN} \text{DEST}[127:96] \leftarrow \text{DEST}[127:96]; \\
&\quad \text{ELSE} \text{DEST}[127:96] \leftarrow \text{SRC}[127:96]; \text{Fl}; \\
\end{align*}
\]
THEN DEST[127:96] ← DEST[127:96];
ELSE DEST[127:96] ← SRC[127:96]; FI;

VP MAXSD (VEX.128 encoded version)
IF SRC[31:0] > SRC2[31:0] THEN
   DEST[31:0] ← SRC1[31:0];
ELSE
   DEST[31:0] ← SRC2[31:0]; FI;
(* Repeat operation for 2nd through 3rd dwords in source and destination operands *)
IF SRC[127:95] > SRC2[127:95] THEN
   DEST[127:95] ← SRC1[127:95];
ELSE
   DEST[127:95] ← SRC2[127:95]; FI;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMAXSD: __m128i _mm_max_epi32 (__m128i a, __m128i b);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PMAXSW—Maximum of Packed Signed Word Integers

<table>
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<tr>
<th>Opcode/Instruction</th>
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<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F EE /r(^1) PMAXSW mm1, mm2/m64</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Compare signed word integers in mm2/m64 and mm1 and return maximum values.</td>
</tr>
<tr>
<td>66 0F EE /r PMAXSW xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compare signed word integers in xmm2/m128 and xmm1 and return maximum values.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG EE /r VPMAXSW xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed signed word integers in xmm3/m128 and xmm2 and store packed maximum values in xmm1.</td>
</tr>
</tbody>
</table>

**NOTES:**

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<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD compare of the packed signed word integers in the destination operand (first operand) and the source operand (second operand), and returns the maximum value for each pair of word integers to the destination operand. The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.
INSTRUCTION SET REFERENCE, M-Z

Operation

PMAXSW (64-bit operands)

IF DEST[15:0] > SRC[15:0] THEN
   DEST[15:0] ← DEST[15:0];
ELSE
   DEST[15:0] ← SRC[15:0]; FI;

(* Repeat operation for 2nd and 3rd words in source and destination operands *)

   DEST[63:48] ← DEST[63:48];
ELSE
   DEST[63:48] ← SRC[63:48]; FI;

PMAXSW (128-bit operands)

IF DEST[15:0] > SRC[15:0] THEN
   DEST[15:0] ← DEST[15:0];
ELSE
   DEST[15:0] ← SRC[15:0]; FI;

(* Repeat operation for 2nd through 7th words in source and destination operands *)

   DEST[127:112] ← DEST[127:112];
ELSE
   DEST[127:112] ← SRC[127:112]; FI;

VPMAXSW (VEX.128 encoded version)

IF SRC1[15:0] > SRC2[15:0] THEN
   DEST[15:0] ← SRC1[15:0];
ELSE
   DEST[15:0] ← SRC2[15:0]; FI;

(* Repeat operation for 2nd through 7th words in source and destination operands *)

   DEST[127:112] ← SRC1[127:112];
ELSE
   DEST[127:112] ← SRC2[127:112]; FI;

DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent

PMAXSW: __m64 _mm_max_pi16(__m64 a, __m64 b)
PMAXSW: __m128i _mm_max_epi16(__m128i a, __m128i b)

Flags Affected

None.
Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
### PMAXUB—Maximum of Packed Unsigned Byte Integers

<table>
<thead>
<tr>
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<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
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<th>Description</th>
</tr>
</thead>
</table>
| 0F DE /r\(^1\)  
PMAXUB mm1, mm2/m64 | RM V/V | SSE | Compare unsigned byte integers in mm2/m64 and mm1 and returns maximum values. |
| 66 0F DE /r  
PMAXUB xmm1, xmm2/m128 | RM V/V | SSE2 | Compare unsigned byte integers in xmm2/m128 and xmm1 and returns maximum values. |
| VEX.NDS.128.66.0F.WIG DE /r  
VPMAXUB xmm1, xmm2, xmm3/m128 | RVM V/V | AVX | Compare packed unsigned byte integers in xmm2 and xmm3/m128 and store packed maximum values in xmm1. |

**NOTES:**


### Instruction Operand Encoding

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<th>Op/En</th>
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<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Performs a SIMD compare of the packed unsigned byte integers in the destination operand (first operand) and the source operand (second operand), and returns the maximum value for each pair of byte integers to the destination operand. The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.
INSTRUCTION SET REFERENCE, M-Z

Operation

**PMAXUB (64-bit operands)**

IF DEST[7:0] > SRC[17:0] THEN
  DEST[7:0] ← DEST[7:0];
ELSE
  DEST[7:0] ← SRC[7:0]; FI;

(* Repeat operation for 2nd through 7th bytes in source and destination operands *)

IF DEST[63:56] > SRC[63:56] THEN
  DEST[63:56] ← DEST[63:56];
ELSE
  DEST[63:56] ← SRC[63:56]; FI;

**PMAXUB (128-bit operands)**

IF DEST[7:0] > SRC[17:0] THEN
  DEST[7:0] ← DEST[7:0];
ELSE
  DEST[7:0] ← SRC[7:0]; FI;

(* Repeat operation for 2nd through 15th bytes in source and destination operands *)

IF DEST[127:120] > SRC[127:120] THEN
  DEST[127:120] ← DEST[127:120];
ELSE
  DEST[127:120] ← SRC[127:120]; FI;

**VPMAXUB (VEX.128 encoded version)**

IF SRC1[7:0] > SRC2[7:0] THEN
  DEST[7:0] ← SRC1[7:0];
ELSE
  DEST[7:0] ← SRC2[7:0]; FI;

(* Repeat operation for 2nd through 15th bytes in source and destination operands *)

IF SRC1[127:120] > SRC2[127:120] THEN
  DEST[127:120] ← SRC1[127:120];
ELSE
  DEST[127:120] ← SRC2[127:120]; FI;

DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

PMAXUB:  __m64 _mm_max_pu8(__m64 a, __m64 b)
PMAXUB:  __m128i _mm_max_epu8 ( __m128i a, __m128i b)

**Flags Affected**

None.
Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
**PMAXUD — Maximum of Packed Unsigned Dword Integers**

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<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Compare packed unsigned dword integers in xmm1 and xmm2/m128 and store packed maximum values in xmm1.</td>
</tr>
<tr>
<td>PMAXUD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 3F /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed unsigned dword integers in xmm2 and xmm3/m128 and store packed maximum values in xmm1.</td>
</tr>
<tr>
<td>VPMAXUD xmm1, xmm2, xmm3/m128</td>
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**Instruction Operands Encoding**

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<td>ModRMreg (r, w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Compares packed unsigned dword integers in the destination operand (first operand) and the source operand (second operand), and returns the maximum for each packed value in the destination operand.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

\[
\begin{align*}
\text{IF } & (\text{DEST}[31:0] > \text{SRC}[31:0]) \\
\text{THEN } & \text{DEST}[31:0] \leftarrow \text{DEST}[31:0]; \\
\text{ELSE} & \text{DEST}[31:0] \leftarrow \text{SRC}[31:0]; \text{FI}; \\
\text{IF } & (\text{DEST}[63:32] > \text{SRC}[63:32]) \\
\text{THEN } & \text{DEST}[63:32] \leftarrow \text{DEST}[63:32]; \\
\text{ELSE} & \text{DEST}[63:32] \leftarrow \text{SRC}[63:32]; \text{FI}; \\
\text{IF } & (\text{DEST}[95:64] > \text{SRC}[95:64]) \\
\text{THEN } & \text{DEST}[95:64] \leftarrow \text{DEST}[95:64]; \\
\text{ELSE} & \text{DEST}[95:64] \leftarrow \text{SRC}[95:64]; \text{FI}; \\
\text{IF } & (\text{DEST}[127:96] > \text{SRC}[127:96]) \\
\end{align*}
\]

PMAXUD — Maximum of Packed Unsigned Dword Integers
THEN DEST[127:96] ← DEST[127:96];
ELSE DEST[127:96] ← SRC[127:96]; FI;

VPMAXUD (VEX.128 encoded version)
IF SRC1[31:0] > SRC2[31:0] THEN
   DEST[31:0] ← SRC1[31:0];
ELSE
   DEST[31:0] ← SRC2[31:0]; FI;
(* Repeat operation for 2nd through 3rd dwords in source and destination operands *)
IF SRC1[127:95] > SRC2[127:95] THEN
   DEST[127:95] ← SRC1[127:95];
ELSE
   DEST[127:95] ← SRC2[127:95]; FI;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMAXUD: __m128i _mm_max_epu32 (__m128i a, __m128i b);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PMAXUW — Maximum of Packed Word Integers

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<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Compare packed unsigned word integers in xmm1 and xmm2/m128 and store packed maximum values in xmm1.</td>
</tr>
<tr>
<td>PMAXUW xmm1, xmm2/m128</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66,0F38.WIG 3E/r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed unsigned word integers in xmm3/m128 and xmm2 and store maximum packed values in xmm1.</td>
</tr>
<tr>
<td>VPMAXUW xmm1, xmm2, xmm3/m128</td>
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**Instruction Operand Encoding**

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<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Compares packed unsigned word integers in the destination operand (first operand) and the source operand (second operand), and returns the maximum for each packed value in the destination operand.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

\[
\begin{align*}
&\text{IF (DEST}[15:0] > \text{SRC}[15:0]) \\
&\quad \text{THEN DEST}[15:0] \leftarrow \text{DEST}[15:0]; \\
&\quad \text{ELSE DEST}[15:0] \leftarrow \text{SRC}[15:0]; \text{FI}; \\
&\text{IF (DEST}[31:16] > \text{SRC}[31:16]) \\
&\quad \text{THEN DEST}[31:16] \leftarrow \text{DEST}[31:16]; \\
&\quad \text{ELSE DEST}[31:16] \leftarrow \text{SRC}[31:16]; \text{FI}; \\
&\text{IF (DEST}[47:32] > \text{SRC}[47:32]) \\
&\quad \text{THEN DEST}[47:32] \leftarrow \text{DEST}[47:32]; \\
&\quad \text{ELSE DEST}[47:32] \leftarrow \text{SRC}[47:32]; \text{FI}; \\
&\text{IF (DEST}[63:48] > \text{SRC}[63:48])
\end{align*}
\]
INSTRUCTION SET REFERENCE, M-Z

THEN DEST[63:48] ← DEST[63:48];
ELSE DEST[63:48] ← SRC[63:48]; FI;
IF (DEST[79:64] > SRC[79:64])
THEN DEST[79:64] ← DEST[79:64];
ELSE DEST[79:64] ← SRC[79:64]; FI;
IF (DEST[95:80] > SRC[95:80])
THEN DEST[95:80] ← DEST[95:80];
ELSE DEST[95:80] ← SRC[95:80]; FI;
IF (DEST[111:96] > SRC[111:96])
THEN DEST[111:96] ← DEST[111:96];
ELSE DEST[111:96] ← SRC[111:96]; FI;
IF (DEST[127:112] > SRC[127:112])
THEN DEST[127:112] ← DEST[127:112];
ELSE DEST[127:112] ← SRC[127:112]; FI;

VPMAXUW (VEX.128 encoded version)
IF SRC1[15:0] > SRC2[15:0] THEN
   DEST[15:0] ← SRC1[15:0];
ELSE
   DEST[15:0] ← SRC2[15:0]; FI;
(* Repeat operation for 2nd through 7th words in source and destination operands *)
   DEST[127:112] ← SRC1[127:112];
ELSE
   DEST[127:112] ← SRC2[127:112]; FI;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMAXUW: __m128i _mm_max_epu16 (__m128i a, __m128i b);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PMINSB — Minimum of Packed Signed Byte Integers

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<tr>
<td>66 0F 38 3B /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Compare packed signed byte integers in xmm1 and xmm2/m128 and store packed minimum values in xmm1.</td>
</tr>
<tr>
<td>PMINSB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 3B /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed signed byte integers in xmm2 and xmm3/m128 and store packed minimum values in xmm1.</td>
</tr>
<tr>
<td>VPMINSB xmm1, xmm2, xmm3/m128</td>
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Instruction Operand Encoding

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<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMrm (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMrm (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Compares packed signed byte integers in the destination operand (first operand) and the source operand (second operand), and returns the minimum for each packed value in the destination operand.

128-bit Legacy SSE version: Bits (VLMAX-1:1288) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

\[
\begin{align*}
\text{IF } & (\text{DEST}[7:0] < \text{SRC}[7:0]) \\
& \text{THEN } \text{DEST}[7:0] \leftarrow \text{DEST}[7:0]; \\
\text{ELSE } & \text{DEST}[7:0] \leftarrow \text{SRC}[7:0]; \text{FI}; \\
\text{IF } & (\text{DEST}[15:8] < \text{SRC}[15:8]) \\
& \text{THEN } \text{DEST}[15:8] \leftarrow \text{DEST}[15:8]; \\
\text{ELSE } & \text{DEST}[15:8] \leftarrow \text{SRC}[15:8]; \text{FI}; \\
\text{IF } & (\text{DEST}[23:16] < \text{SRC}[23:16]) \\
& \text{THEN } \text{DEST}[23:16] \leftarrow \text{DEST}[23:16]; \\
\text{ELSE } & \text{DEST}[23:16] \leftarrow \text{SRC}[23:16]; \text{FI}; \\
\text{IF } & (\text{DEST}[31:24] < \text{SRC}[31:24]) \\
& \text{THEN } \text{DEST}[31:24] \leftarrow \text{DEST}[31:24]; \\
\text{ELSE } & \text{DEST}[31:24] \leftarrow \text{SRC}[31:24]; \text{FI}; \\
\end{align*}
\]
THEN DEST[31:24] ← DEST[31:24];
ELSE DEST[31:24] ← SRC[31:24]; Fl;
IF (DEST[47:40] < SRC[47:40])
THEN DEST[47:40] ← DEST[47:40];
ELSE DEST[47:40] ← SRC[47:40]; Fl;
IF (DEST[55:48] < SRC[55:48])
ELSE DEST[55:48] ← SRC[55:48]; Fl;
IF (DEST[63:56] < SRC[63:56])
THEN DEST[63:56] ← DEST[63:56];
ELSE DEST[63:56] ← SRC[63:56]; Fl;
IF (DEST[71:64] < SRC[71:64])
THEN DEST[71:64] ← DEST[71:64];
ELSE DEST[71:64] ← SRC[71:64]; Fl;
IF (DEST[79:72] < SRC[79:72])
THEN DEST[79:72] ← DEST[79:72];
ELSE DEST[79:72] ← SRC[79:72]; Fl;
IF (DEST[87:80] < SRC[87:80])
THEN DEST[87:80] ← DEST[87:80];
ELSE DEST[87:80] ← SRC[87:80]; Fl;
IF (DEST[95:88] < SRC[95:88])
THEN DEST[95:88] ← DEST[95:88];
ELSE DEST[95:88] ← SRC[95:88]; Fl;
IF (DEST[103:96] < SRC[103:96])
THEN DEST[103:96] ← DEST[103:96];
ELSE DEST[103:96] ← SRC[103:96]; Fl;
IF (DEST[111:104] < SRC[111:104])
THEN DEST[111:104] ← DEST[111:104];
ELSE DEST[111:104] ← SRC[111:104]; Fl;
IF (DEST[119:112] < SRC[119:112])
THEN DEST[119:112] ← DEST[119:112];
ELSE DEST[119:112] ← SRC[119:112]; Fl;
IF (DEST[127:120] < SRC[127:120])
THEN DEST[127:120] ← DEST[127:120];
ELSE DEST[127:120] ← SRC[127:120]; Fl;

VPMINSB (VEX.128 encoded version)
IF SRC1[7:0] < SRC2[7:0] THEN
    DEST[7:0] ← SRC1[7:0];
ELSE
PMINSB — Minimum of Packed Signed Byte Integers

```
DEST[7:0] ← SRC2[7:0]; Fl;
(* Repeat operation for 2nd through 15th bytes in source and destination operands *)
IF SRC1[127:120] < SRC2[127:120] THEN
  DEST[127:120] ← SRC1[127:120];
ELSE
  DEST[127:120] ← SRC2[127:120]; Fl;
DEST[VLMAX-1:128] ← 0
```

**Intel C/C++ Compiler Intrinsic Equivalent**

PMINSB: `__m128i _mm_min_epi8 ( __m128i a, __m128i b);`

**Flags Affected**

None.

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.L = 1.
PMINSD — Minimum of Packed Dword Integers

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<td>66 0F 38 39 /r PMINSD xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Compare packed signed dword integers in xmm1 and xmm2/m128 and store packed minimum values in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66H.0F38.WIG 39 /r VPMINSD xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Compare packed signed dword integers in xmm2 and xmm3/m128 and store packed minimum values in xmm1.</td>
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Instruction Operand Encoding

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<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
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</tr>
</tbody>
</table>

Description

Compares packed signed dword integers in the destination operand (first operand) and the source operand (second operand), and returns the minimum for each packed value in the destination operand.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

IF (DEST[31:0] < SRC[31:0])
    THEN DEST[31:0] ← DEST[31:0];
ELSE DEST[31:0] ← SRC[31:0]; Flt;
IF (DEST[63:32] < SRC[63:32])
    THEN DEST[63:32] ← DEST[63:32];
ELSE DEST[63:32] ← SRC[63:32]; Flt;
IF (DEST[95:64] < SRC[95:64])
    THEN DEST[95:64] ← DEST[95:64];
ELSE DEST[95:64] ← SRC[95:64]; Flt;
IF (DEST[127:96] < SRC[127:96])
    THEN DEST[127:96] ← DEST[127:96];
ELSE DEST[127:96] ← SRC[127:96]; Flt;

THEN DEST[127:96] ← DEST[127:96];
ELSE DEST[127:96] ← SRC[127:96]; FI;

VPMINSND (VEX.128 encoded version)
    IF SRC1[31:0] < SRC2[31:0] THEN
        DEST[31:0] ← SRC1[31:0];
    ELSE
        DEST[31:0] ← SRC2[31:0]; FI;
    (* Repeat operation for 2nd through 3rd dwords in source and destination operands *)
    IF SRC1[127:95] < SRC2[127:95] THEN
        DEST[127:95] ← SRC1[127:95];
    ELSE
        DEST[127:95] ← SRC2[127:95]; FI;
    DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMINSND:  __m128i _mm_min_epi32 ( __m128i a, __m128i b);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD                  If VEX.L = 1.
PMINSW—Minimum of Packed Signed Word Integers

<table>
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<tr>
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<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0F EA /r(^1) PMINSW mm1, mm2/m64</td>
<td>RM V/V</td>
<td>SSE</td>
<td>Compare signed word integers in mm2/m64 and mm1 and return minimum values.</td>
<td></td>
</tr>
<tr>
<td>66 0F EA /r PMINSW xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Compare signed word integers in xmm2/m128 and xmm1 and return minimum values.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG EA /r VPMINSW xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Compare packed signed word integers in xmm3/m128 and xmm2 and return packed minimum values in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMrmr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMrmr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD compare of the packed signed word integers in the destination operand (first operand) and the source operand (second operand), and returns the minimum value for each pair of word integers to the destination operand. The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.
Operation

**PMINSW (64-bit operands)**
IF DEST[15:0] < SRC[15:0] THEN
  DEST[15:0] ← DEST[15:0];
ELSE
  DEST[15:0] ← SRC[15:0]; Fl;
(* Repeat operation for 2nd and 3rd words in source and destination operands *)
  DEST[63:48] ← DEST[63:48];
ELSE
  DEST[63:48] ← SRC[63:48]; Fl;

**PMINSW (128-bit operands)**
IF DEST[15:0] < SRC[15:0] THEN
  DEST[15:0] ← DEST[15:0];
ELSE
  DEST[15:0] ← SRC[15:0]; Fl;
(* Repeat operation for 2nd through 7th words in source and destination operands *)
IF DEST[127:112] < SRC/m64[127:112] THEN
  DEST[127:112] ← DEST[127:112];
ELSE
  DEST[127:112] ← SRC[127:112]; Fl;

**VPMINSW (VEX.128 encoded version)**
IF SRC1[15:0] < SRC2[15:0] THEN
  DEST[15:0] ← SRC1[15:0];
ELSE
  DEST[15:0] ← SRC2[15:0]; Fl;
(* Repeat operation for 2nd through 7th words in source and destination operands *)
  DEST[127:112] ← SRC1[127:112];
ELSE
  DEST[127:112] ← SRC2[127:112]; Fl;
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**
PMINSW: __m64 _mm_min_pi16 (__m64 a, __m64 b)
PMINSW: __m128i _mm_min_epi16 (__m128i a, __m128i b)

**Flags Affected**
None.
Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
#MF (64-bit operations only) If there is a pending x87 FPU exception.
PMINUB—Minimum of Packed Unsigned Byte Integers

<table>
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<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF DA /r^1</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Compare unsigned byte integers in mm2/m64 and mm1 and returns minimum values.</td>
</tr>
<tr>
<td>PMINUB mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF DA /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compare unsigned byte integers in xmm2/m128 and xmm1 and returns minimum values.</td>
</tr>
<tr>
<td>PMINUB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG DA /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed unsigned byte integers in xmm2 and xmm3/m128 and store packed minimum values in xmm1.</td>
</tr>
<tr>
<td>VPMINUB xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

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<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD compare of the packed unsigned byte integers in the destination operand (first operand) and the source operand (second operand), and returns the minimum value for each pair of byte integers to the destination operand. The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.
INSTRUCTION SET REFERENCE, M-Z

Operation

PMINUB (for 64-bit operands)
IF DEST[7:0] < SRC[17:0] THEN
DEST[7:0] ← DEST[7:0];
ELSE
DEST[7:0] ← SRC[7:0]; Fl;
(* Repeat operation for 2nd through 7th bytes in source and destination operands *)
IF DEST[63:56] < SRC[63:56] THEN
DEST[63:56] ← DEST[63:56];
ELSE
DEST[63:56] ← SRC[63:56]; Fl;

PMINUB (for 128-bit operands)
IF DEST[7:0] < SRC[17:0] THEN
DEST[7:0] ← DEST[7:0];
ELSE
DEST[7:0] ← SRC[7:0]; Fl;
(* Repeat operation for 2nd through 15th bytes in source and destination operands *)
IF DEST[127:120] < SRC[127:120] THEN
DEST[127:120] ← DEST[127:120];
ELSE
DEST[127:120] ← SRC[127:120]; Fl;

VPMINUB (VEX.128 encoded version)
VPMINUB instruction for 128-bit operands:
IF SRC1[7:0] < SRC2[7:0] THEN
DEST[7:0] ← SRC1[7:0];
ELSE
DEST[7:0] ← SRC2[7:0]; Fl;
(* Repeat operation for 2nd through 15th bytes in source and destination operands *)
IF SRC1[127:120] < SRC2[127:120] THEN
DEST[127:120] ← SRC1[127:120];
ELSE
DEST[127:120] ← SRC2[127:120]; Fl;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMINUB:  __m64 _m_min_pu8 (__m64 a, __m64 b)
PMINUB:  __m128i _mm_min_epu8 ( __m128i a, __m128i b)

Flags Affected
None.
**Numeric Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.L = 1.
**PMINUD — Minimum of Packed Dword Integers**

<table>
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<th>64/32 bit Mode Support</th>
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</thead>
<tbody>
<tr>
<td>66 0F 3B 3B /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Compare packed unsigned dword integers in xmm1 and xmm2/m128 and store packed minimum values in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 3B /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed unsigned dword integers in xmm2 and xmm3/m128 and store packed minimum values in xmm1.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

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</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Compares packed unsigned dword integers in the destination operand (first operand) and the source operand (second operand), and returns the minimum for each packed value in the destination operand.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

\[
\text{IF (DEST}[31:0] \text{ < SRC}[31:0])}
\text{THEN DEST}[31:0] \leftarrow \text{DEST}[31:0];
\text{ELSE DEST}[31:0] \leftarrow \text{SRC}[31:0]; \text{FI;}
\text{IF (DEST}[63:32] \text{ < SRC}[63:32])}
\text{THEN DEST}[63:32] \leftarrow \text{DEST}[63:32];
\text{ELSE DEST}[63:32] \leftarrow \text{SRC}[63:32]; \text{FI;}
\text{IF (DEST}[95:64] \text{ < SRC}[95:64])}
\text{THEN DEST}[95:64] \leftarrow \text{DEST}[95:64];
\text{ELSE DEST}[95:64] \leftarrow \text{SRC}[95:64]; \text{FI;}
\text{IF (DEST}[127:96] \text{ < SRC}[127:96])}
\]
THEN DEST[127:96] ← DEST[127:96];
ELSE DEST[127:96] ← SRC[127:96]; Fl;

VPMINUD (VEX.128 encoded version)
VPMINUD instruction for 128-bit operands:
IF SRC1[31:0] < SRC2[31:0] THEN
   DEST[31:0] ← SRC1[31:0];
ELSE
   DEST[31:0] ← SRC2[31:0]; Fl;
(* Repeat operation for 2nd through 3rd dwords in source and destination operands *)
IF SRC1[127:95] < SRC2[127:95] THEN
   DEST[127:95] ← SRC1[127:95];
ELSE
   DEST[127:95] ← SRC2[127:95]; Fl;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMINUD: __m128i _mm_min_epu32 ( __m128i a, __m128i b);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
**PMINUW — Minimum of Packed Word Integers**

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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 3A /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Compare packed unsigned word integers in <code>xmm1</code> and <code>xmm2/m128</code> and store packed minimum values in <code>xmm1</code>.</td>
</tr>
<tr>
<td>VEX.NDS.128.66,0F38.WIG 3A/r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare packed unsigned word integers in <code>xmm3/m128</code> and <code>xmm2</code> and return packed minimum values in <code>xmm1</code>.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

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</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Compares packed unsigned word integers in the destination operand (first operand) and the source operand (second operand), and returns the minimum for each packed value in the destination operand.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

\[
\begin{align*}
\text{IF (DEST}[15:0] & < \text{SRC}[15:0]) \\
& \text{THEN } \text{DEST}[15:0] \leftarrow \text{DEST}[15:0]; \\
& \text{ELSE DEST}[15:0] \leftarrow \text{SRC}[15:0]; \text{FI}; \\
\text{IF (DEST}[31:16] & < \text{SRC}[31:16]) \\
& \text{THEN } \text{DEST}[31:16] \leftarrow \text{DEST}[31:16]; \\
& \text{ELSE DEST}[31:16] \leftarrow \text{SRC}[31:16]; \text{FI}; \\
\text{IF (DEST}[47:32] & < \text{SRC}[47:32]) \\
& \text{THEN } \text{DEST}[47:32] \leftarrow \text{DEST}[47:32]; \\
& \text{ELSE DEST}[47:32] \leftarrow \text{SRC}[47:32]; \text{FI}; \\
\text{IF (DEST}[63:48] & < \text{SRC}[63:48]) \\
& \text{THEN } \text{DEST}[63:48] \leftarrow \text{DEST}[63:48]; \\
& \text{ELSE DEST}[63:48] \leftarrow \text{SRC}[63:48]; \text{FI}; \\
\end{align*}
\]
THEN DEST[63:48] ← DEST[63:48];
ELSE DEST[63:48] ← SRC[63:48]; FI;
IF (DEST[79:64] < SRC[79:64])
    THEN DEST[79:64] ← DEST[79:64];
    ELSE DEST[79:64] ← SRC[79:64]; FI;
IF (DEST[95:80] < SRC[95:80])
    THEN DEST[95:80] ← DEST[95:80];
    ELSE DEST[95:80] ← SRC[95:80]; FI;
IF (DEST[111:96] < SRC[111:96])
    THEN DEST[111:96] ← DEST[111:96];
    ELSE DEST[111:96] ← SRC[111:96]; FI;
IF (DEST[127:112] < SRC[127:112])
    THEN DEST[127:112] ← DEST[127:112];
    ELSE DEST[127:112] ← SRC[127:112]; FI;

VPMINUw (VEX.128 encoded version)
VPMINUw instruction for 128-bit operands:
IF SRC1[15:0] < SRC2[15:0] THEN
    DEST[15:0] ← SRC1[15:0];
ELSE
    DEST[15:0] ← SRC2[15:0]; FI;
(* Repeat operation for 2nd through 7th words in source and destination operands *)
    DEST[127:112] ← SRC1[127:112];
ELSE
    DEST[127:112] ← SRC2[127:112]; FI;
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMINUw: __m128i _mm_min_epu16 (__m128i a, __m128i b);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PMOVMSKB—Move Byte Mask

<table>
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<tr>
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<th>CPUID Feature Flag</th>
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<tbody>
<tr>
<td>0F D7 /r1 PMOVMSKB reg, mm</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Move a byte mask of mm to reg. The upper bits of r32 or r64 are zeroed</td>
</tr>
<tr>
<td>66 0F D7 /r PMOVMSKB reg, xmm</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Move a byte mask of xmm to reg. The upper bits of r32 or r64 are zeroed</td>
</tr>
<tr>
<td>VEX.128.66.0F.WIG D7 /r VPMOVMSKB reg, xmm1</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Move a byte mask of xmm1 to reg. The upper bits of r32 or r64 are filled with zeros.</td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

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</thead>
<tbody>
<tr>
<td>RM ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

Description

Creates a mask made up of the most significant bit of each byte of the source operand (second operand) and stores the result in the low byte or word of the destination operand (first operand). The source operand is an MMX technology register or an XMM register; the destination operand is a general-purpose register. When operating on 64-bit operands, the byte mask is 8 bits; when operating on 128-bit operands, the byte mask is 16-bits.

In 64-bit mode, the instruction can access additional registers (XMM8-XMM15, R8-R15) when used with a REX.R prefix. The default operand size is 64-bit in 64-bit mode.

VEX.128 encodings are valid but identical in function. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.

Operation

PMOVMSKB (with 64-bit source operand and r32)

\[
\begin{align*}
r32[0] & \leftarrow \text{SRC}[7]; \\
r32[1] & \leftarrow \text{SRC}[15]; \\
\end{align*}
\]
PMOVMSKB—Move Byte Mask

(* Repeat operation for bytes 2 through 6 *)
\[ r32[7] \leftarrow \text{SRC}[63]; \]
\[ r32[31:8] \leftarrow \text{ZERO_FILL}; \]

(V)PMOVMSKB (with 128-bit source operand and r32)
\[ r32[0] \leftarrow \text{SRC}[7]; \]
\[ r32[1] \leftarrow \text{SRC}[15]; \]
(* Repeat operation for bytes 2 through 14 *)
\[ r32[15] \leftarrow \text{SRC}[127]; \]
\[ r32[31:16] \leftarrow \text{ZERO_FILL}; \]

PMOVMSKB (with 64-bit source operand and r64)
\[ r64[0] \leftarrow \text{SRC}[7]; \]
\[ r64[1] \leftarrow \text{SRC}[15]; \]
(* Repeat operation for bytes 2 through 6 *)
\[ r64[7] \leftarrow \text{SRC}[63]; \]
\[ r64[63:8] \leftarrow \text{ZERO_FILL}; \]

(V)PMOVMSKB (with 128-bit source operand and r64)
\[ r64[0] \leftarrow \text{SRC}[7]; \]
\[ r64[1] \leftarrow \text{SRC}[15]; \]
(* Repeat operation for bytes 2 through 14 *)
\[ r64[15] \leftarrow \text{SRC}[127]; \]
\[ r64[63:16] \leftarrow \text{ZERO_FILL}; \]

Intel C/C++ Compiler Intrinsic Equivalent
PMOVMSKB: \ \ \ \ \text{int } \_\_m\_movemask\_pi8(__m64 a)
PMOVMSKB: \ \ \ \ \text{int } \_\_m\_movemask\_epi8(__m128i a)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 7; additionally
\#UD \ \ \ \ \text{If VEX.L = 1.}
\ \ \ \ \text{If VEX.vvvv } \neq 1111B.
## PMOVSX — Packed Move with Sign Extend

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<tr>
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<tbody>
<tr>
<td>66 0f 38 20 /r PMOVSXBW xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Sign extend 8 packed signed 8-bit integers in the low 8 bytes of xmm2/m64 to 8 packed signed 16-bit integers in xmm1.</td>
<td></td>
</tr>
<tr>
<td>66 0f 38 21 /r PMOVSXBD xmm1, xmm2/m32</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Sign extend 4 packed signed 8-bit integers in the low 4 bytes of xmm2/m32 to 4 packed signed 32-bit integers in xmm1.</td>
<td></td>
</tr>
<tr>
<td>66 0f 38 22 /r PMOVSXBQ xmm1, xmm2/m16</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Sign extend 2 packed signed 8-bit integers in the low 2 bytes of xmm2/m16 to 2 packed signed 64-bit integers in xmm1.</td>
<td></td>
</tr>
<tr>
<td>66 0f 38 23 /r PMOVSXWD xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Sign extend 4 packed signed 16-bit integers in the low 8 bytes of xmm2/m64 to 4 packed signed 32-bit integers in xmm1.</td>
<td></td>
</tr>
<tr>
<td>66 0f 38 24 /r PMOVSXWQ xmm1, xmm2/m32</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Sign extend 2 packed signed 16-bit integers in the low 4 bytes of xmm2/m32 to 2 packed signed 64-bit integers in xmm1.</td>
<td></td>
</tr>
<tr>
<td>66 0f 38 25 /r PMOVSXDXQ xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Sign extend 2 packed signed 32-bit integers in the low 8 bytes of xmm2/m64 to 2 packed signed 64-bit integers in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 20 /r VPMOVSXBW xmm1, xmm2/m64</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Sign extend 8 packed 8-bit integers in the low 8 bytes of xmm2/m64 to 8 packed 16-bit integers in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 21 /r VPMOVSXBD xmm1, xmm2/m32</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Sign extend 4 packed 8-bit integers in the low 4 bytes of xmm2/m32 to 4 packed 32-bit integers in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>
PMOVSX — Packed Move with Sign Extend

**Description**

Sign-extend the low byte/word/dword values in each word/dword/qword element of the source operand (second operand) to word/dword/qword integers and stored as packed data in the destination operand (first operand).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PMOVSX BW**

\[
\begin{align*}
\text{DEST}[15:0] &\leftarrow \text{SignExtend}([7:0]); \\
\text{DEST}[31:16] &\leftarrow \text{SignExtend}([15:8]); \\
\text{DEST}[47:32] &\leftarrow \text{SignExtend}([23:16]); \\
\text{DEST}[63:48] &\leftarrow \text{SignExtend}([31:24]);
\end{align*}
\]

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Opcode/Instruction**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.128.66.0F38.WIG 22 /r</td>
<td>RM V/V</td>
<td>AVX</td>
<td></td>
<td>Sign extend 2 packed 8-bit integers in the low 2 bytes of xmm2/m16 to 2 packed 64-bit integers in xmm1.</td>
</tr>
<tr>
<td>VPMOVSXQB xmm1, xmm2/m16</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 23 /r</td>
<td>RM V/V</td>
<td>AVX</td>
<td></td>
<td>Sign extend 4 packed 16-bit integers in the low 8 bytes of xmm2/m64 to 4 packed 32-bit integers in xmm1.</td>
</tr>
<tr>
<td>VPMOVSXWD xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 24 /r</td>
<td>RM V/V</td>
<td>AVX</td>
<td></td>
<td>Sign extend 2 packed 16-bit integers in the low 4 bytes of xmm2/m32 to 2 packed 64-bit integers in xmm1.</td>
</tr>
<tr>
<td>VPMOVSXWQ xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 25 /r</td>
<td>RM V/V</td>
<td>AVX</td>
<td></td>
<td>Sign extend 2 packed 32-bit integers in the low 8 bytes of xmm2/m64 to 2 packed 64-bit integers in xmm1.</td>
</tr>
<tr>
<td>VPMOVSXDXQ xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, M-Z

DEST[79:64] ← SignExtend(SRC[39:32]);
DEST[95:80] ← SignExtend(SRC[47:40]);
DEST[111:96] ← SignExtend(SRC[55:48]);
DEST[127:112] ← SignExtend(SRC[63:56]);

PMOVSXBD
DEST[31:0] ← SignExtend(SRC[7:0]);
DEST[63:32] ← SignExtend(SRC[15:8]);
DEST[95:64] ← SignExtend(SRC[23:16]);
DEST[127:96] ← SignExtend(SRC[31:24]);

PMOVSXBD
DEST[31:0] ← SignExtend(SRC[7:0]);
DEST[127:64] ← SignExtend(SRC[15:8]);

PMOVSXWD
DEST[31:0] ← SignExtend(SRC[15:0]);
DEST[63:32] ← SignExtend(SRC[31:16]);
DEST[95:64] ← SignExtend(SRC[47:32]);
DEST[127:96] ← SignExtend(SRC[63:48]);

PMOVSXWQ
DEST[63:0] ← SignExtend(SRC[15:0]);
DEST[127:64] ← SignExtend(SRC[31:16]);

PMOVSXDQ
DEST[63:0] ← SignExtend(SRC[31:0]);
DEST[127:64] ← SignExtend(SRC[63:32]);

VPMOVSXBW
Packed_Sign_Extend_BYTE_to_WORD()
DEST[VLMAX-1:128] ← 0

VPMOVSXBD
Packed_Sign_Extend_BYTE_to_DWORD()
DEST[VLMAX-1:128] ← 0

VPMOVSXBD
Packed_Sign_Extend_BYTE_to_QWORD()
DEST[VLMAX-1:128] ← 0

VPMOVSXWD
Packed_Sign_Extend_WORD_to_DWORD()
DEST[VLMAX-1:128] ← 0
VPMOVSXwQ  
Packed_Sign_Extend_WORD_to_QWORD()  
DEST[VLMAX-1:128] ← 0

VPMOVSXDQ  
Packed_Sign_Extend_DWORD_to_QWORD()  
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMOVSXBw:   __m128i _mm_cvt_epi8_epi16 (__m128i a);
PMOVSXBD:   __m128i _mm_cvt_epi8_epi32 (__m128i a);
PMOVSXBQ:   __m128i _mm_cvt_epi8_epi64 (__m128i a);
PMOVSXwD:   __m128i _mm_cvt_epi16_epi32 (__m128i a);
PMOVSXwQ:   __m128i _mm_cvt_epi16_epi64 (__m128i a);
PMOVSXDQ:   __m128i _mm_cvt_epi32_epi64 (__m128i a);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD     If VEX.L = 1.
        If VEX.vvvv != 1111B.
### PMOVZX — Packed Move with Zero Extend

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 30 /r PMOVZXBW xmm1, xmm2/m64</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Zero extend 8 packed 8-bit integers in the low 8 bytes of xmm2/m64 to 8 packed 16-bit integers in xmm1.</td>
</tr>
<tr>
<td>66 0F 38 31 /r PMOVZXBD xmm1, xmm2/m32</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Zero extend 4 packed 8-bit integers in the low 4 bytes of xmm2/m32 to 4 packed 32-bit integers in xmm1.</td>
</tr>
<tr>
<td>66 0F 38 32 /r PMOVZXBD xmm1, xmm2/m16</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Zero extend 2 packed 8-bit integers in the low 2 bytes of xmm2/m16 to 2 packed 64-bit integers in xmm1.</td>
</tr>
<tr>
<td>66 0F 38 33 /r PMOVZXBD xmm1, xmm2/m16</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Zero extend 4 packed 16-bit integers in the low 8 bytes of xmm2/m64 to 4 packed 32-bit integers in xmm1.</td>
</tr>
<tr>
<td>66 0F 38 34 /r PMOVZXBD xmm1, xmm2/m32</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Zero extend 2 packed 16-bit integers in the low 4 bytes of xmm2/m32 to 2 packed 64-bit integers in xmm1.</td>
</tr>
<tr>
<td>66 0F 38 35 /r PMOVZXBD xmm1, xmm2/m64</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Zero extend 2 packed 32-bit integers in the low 8 bytes of xmm2/m64 to 2 packed 64-bit integers in xmm1.</td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 30 /r VPMOVZXWBW xmm1, xmm2/m64</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Zero extend 8 packed 8-bit integers in the low 8 bytes of xmm2/m64 to 8 packed 16-bit integers in xmm1.</td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 31 /r VPMOVZXBD xmm1, xmm2/m32</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Zero extend 4 packed 8-bit integers in the low 4 bytes of xmm2/m32 to 4 packed 32-bit integers in xmm1.</td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 32 /r VPMOVZXBD xmm1, xmm2/m16</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Zero extend 2 packed 8-bit integers in the low 2 bytes of xmm2/m16 to 2 packed 64-bit integers in xmm1.</td>
</tr>
</tbody>
</table>
PMOVZX — Packed Move with Zero Extend

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INSTRUCTION SET REFERENCE, M-Z

INSTRUCTION SET REFERENCE, M-Z

Description
Zero-extend the low byte/word/dword values in each word/dword/qword element of the source operand (second operand) to word/dword/qword integers and stored as packed data in the destination operand (first operand).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.

Operation

PMOVZXBW

\[
\begin{align*}
\text{DEST}[15:0] &\leftarrow \text{ZeroExtend(SRC}[7:0]); \\
\text{DEST}[31:16] &\leftarrow \text{ZeroExtend(SRC}[15:8]); \\
\text{DEST}[47:32] &\leftarrow \text{ZeroExtend(SRC}[23:16]); \\
\text{DEST}[63:48] &\leftarrow \text{ZeroExtend(SRC}[31:24]); \\
\text{DEST}[79:64] &\leftarrow \text{ZeroExtend(SRC}[39:32]); \\
\text{DEST}[95:80] &\leftarrow \text{ZeroExtend(SRC}[47:40]); \\
\text{DEST}[111:96] &\leftarrow \text{ZeroExtend(SRC}[55:48]); \\
\text{DEST}[127:112] &\leftarrow \text{ZeroExtend(SRC}[63:56]); \\
\end{align*}
\]

Zero extend 4 packed 16-bit integers in the low 8 bytes of xmm2/m64 to 4 packed 32-bit integers in xmm1.

Zero extend 2 packed 16-bit integers in the low 4 bytes of xmm2/m32 to 2 packed 64-bit integers in xmm1.

Zero extend 2 packed 32-bit integers in the low 8 bytes of xmm2/m64 to 2 packed 64-bit integers in xmm1.
INSTRUCTION SET REFERENCE, M-Z

PMOVZXBD
   DEST[31:0] ← ZeroExtend(SRC[7:0]);
   DEST[63:32] ← ZeroExtend(SRC[15:8]);
   DEST[95:64] ← ZeroExtend(SRC[23:16]);
   DEST[127:96] ← ZeroExtend(SRC[31:24]);

PMOVZXQB
   DEST[63:0] ← ZeroExtend(SRC[7:0]);
   DEST[127:64] ← ZeroExtend(SRC[15:8]);

PMOVZXWD
   DEST[31:0] ← ZeroExtend(SRC[15:0]);
   DEST[63:32] ← ZeroExtend(SRC[31:16]);
   DEST[95:64] ← ZeroExtend(SRC[47:32]);
   DEST[127:96] ← ZeroExtend(SRC[63:48]);

PMOVZXWQ
   DEST[63:0] ← ZeroExtend(SRC[15:0]);
   DEST[127:64] ← ZeroExtend(SRC[31:16]);

PMOVZXDQ
   DEST[63:0] ← ZeroExtend(SRC[31:0]);
   DEST[127:64] ← ZeroExtend(SRC[63:32]);

VPMOVZXBW
   Packed_Zero_Extend_BYTE_to_WORD()
   DEST[VLMAX-1:128] ← 0

VPMOVZXBD
   Packed_Zero_Extend_BYTE_to_DWORD()
   DEST[VLMAX-1:128] ← 0

VPMOVZXQB
   Packed_Zero_Extend_BYTE_to_QWORD()
   DEST[VLMAX-1:128] ← 0

VPMOVZXWD
   Packed_Zero_Extend_WORD_to_DWORD()
   DEST[VLMAX-1:128] ← 0

VPMOVZXWQ
   Packed_Zero_Extend_WORD_to_QWORD()
   DEST[VLMAX-1:128] ← 0

VPMOVZXDQ
Packed_Zero_Extend_DWORD_to_QWORD()
DEST[VLMAX-1:128] ← 0

Flags Affected
None

Intel C/C++ Compiler Intrinsic Equivalent
PMOVZXBW: __m128i _mm_cvtupu8_epi16 (__m128i a);
PMOVZXBW: __m128i _mm_cvtepu8_epi16 (__m128i a);
PMOVZXBD: __m128i _mm_cvtepu8_epi32 (__m128i a);
PMOVZXBQ: __m128i _mm_cvtepu8_epi64 (__m128i a);
PMOVZXWD: __m128i _mm_cvtepu16_epi32 (__m128i a);
PMOVZXWQ: __m128i _mm_cvtepu16_epi64 (__m128i a);
PMOVZXDQ: __m128i _mm_cvtepu32_epi64 (__m128i a);

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD If VEX.L = 1.
   If VEX.vvvv != 1111B.
**PMULDQ — Multiply Packed Signed Dword Integers**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 28 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Multiply the packed signed dword integers in xmm1 and xmm2/m128 and store the quadword product in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 28 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply packed signed doubleword integers in xmm2 by packed signed doubleword integers in xmm3/m128, and store the quadword results in xmm1.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs two signed multiplications from two pairs of signed dword integers and stores two 64-bit products in the destination operand (first operand). The 64-bit product from the first/third dword element in the destination operand and the first/third dword element of the source operand (second operand) is stored to the low/high qword element of the destination.

If the source is a memory operand then all 128 bits will be fetched from memory but the second and fourth dwords will not be used in the computation.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PMULDQ (128-bit Legacy SSE version)**

DEST[63:0] ← DEST[31:0] * SRC[31:0]  
DEST[127:64] ← DEST[95:64] * SRC[95:64]  
DEST[VLMAX-1:128] (Unmodified)

**VPMULDQ (VEX.128 encoded version)**
PMULDQ — Multiply Packed Signed Dword Integers

DEST[63:0] ← SRC1[31:0] * SRC2[31:0]
DEST[127:64] ← SRC1[95:64] * SRC2[95:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent

PMULDQ: __m128i _mm_mul_epi32(__m128i a, __m128i b);

Flags Affected

None.

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 5; additionally

#UD  If VEX.L = 1.
    If VEX.vvvv != 1111B.
PMULHRSW — Packed Multiply High with Round and Scale

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 0B /r (^1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMULHRSW mm1, mm2/m64</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Multiply 16-bit signed words, scale and round signed doublewords, pack high 16 bits to MM1.</td>
<td></td>
</tr>
<tr>
<td>66 0F 38 0B /r</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMULHRSW xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Multiply 16-bit signed words, scale and round signed doublewords, pack high 16 bits to XMM1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 0B /r</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VPMULHRSW xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Multiply 16-bit signed words, scale and round signed doublewords, pack high 16 bits to xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
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</thead>
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<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

PMULHRSW multiplies vertically each signed 16-bit integer from the destination operand (first operand) with the corresponding signed 16-bit integer of the source operand (second operand), producing intermediate, signed 32-bit integers. Each intermediate 32-bit integer is truncated to the 18 most significant bits. Rounding is always performed by adding 1 to the least significant bit of the 18-bit intermediate result. The final result is obtained by selecting the 16 bits immediately to the right of the most significant bit of each 18-bit intermediate result and packed to the destination operand. Both operands can be MMX register or XMM registers.

When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated. In 64-bit mode, use the REX prefix to access additional registers.
128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

**PMULHRSW (with 64-bit operands)**

\[
\begin{align*}
\text{temp0}[31:0] &= \text{INT32}((\text{DEST}[15:0] * \text{SRC}[15:0]) \gg 14) + 1; \\
\text{temp1}[31:0] &= \text{INT32}((\text{DEST}[31:16] * \text{SRC}[31:16]) \gg 14) + 1; \\
\text{temp2}[31:0] &= \text{INT32}((\text{DEST}[47:32] * \text{SRC}[47:32]) \gg 14) + 1; \\
\text{temp3}[31:0] &= \text{INT32}((\text{DEST}[63:48] * \text{SRC}[63:48]) \gg 14) + 1; \\
\text{DEST}[15:0] &= \text{temp0}[16:1]; \\
\text{DEST}[31:16] &= \text{temp1}[16:1]; \\
\text{DEST}[47:32] &= \text{temp2}[16:1]; \\
\text{DEST}[63:48] &= \text{temp3}[16:1];
\end{align*}
\]

**PMULHRSW (with 128-bit operand)**

\[
\begin{align*}
\text{temp0}[31:0] &= \text{INT32}((\text{DEST}[15:0] * \text{SRC}[15:0]) \gg 14) + 1; \\
\text{temp1}[31:0] &= \text{INT32}((\text{DEST}[31:16] * \text{SRC}[31:16]) \gg 14) + 1; \\
\text{temp2}[31:0] &= \text{INT32}((\text{DEST}[47:32] * \text{SRC}[47:32]) \gg 14) + 1; \\
\text{temp3}[31:0] &= \text{INT32}((\text{DEST}[63:48] * \text{SRC}[63:48]) \gg 14) + 1; \\
\text{temp4}[31:0] &= \text{INT32}((\text{DEST}[79:64] * \text{SRC}[79:64]) \gg 14) + 1; \\
\text{temp5}[31:0] &= \text{INT32}((\text{DEST}[95:80] * \text{SRC}[95:80]) \gg 14) + 1; \\
\text{temp6}[31:0] &= \text{INT32}((\text{DEST}[111:96] * \text{SRC}[111:96]) \gg 14) + 1; \\
\text{temp7}[31:0] &= \text{INT32}((\text{DEST}[127:112] * \text{SRC}[127:112]) \gg 14) + 1; \\
\text{DEST}[15:0] &= \text{temp0}[16:1]; \\
\text{DEST}[31:16] &= \text{temp1}[16:1]; \\
\text{DEST}[47:32] &= \text{temp2}[16:1]; \\
\text{DEST}[63:48] &= \text{temp3}[16:1]; \\
\text{DEST}[79:64] &= \text{temp4}[16:1]; \\
\text{DEST}[95:80] &= \text{temp5}[16:1]; \\
\text{DEST}[111:96] &= \text{temp6}[16:1]; \\
\text{DEST}[127:112] &= \text{temp7}[16:1];
\end{align*}
\]

**VPMULHRSW (VEX.128 encoded version)**

\[
\begin{align*}
\text{temp0}[31:0] &\leftarrow \text{INT32}((\text{SRC}[15:0] * \text{SRC}[15:0]) \gg 14) + 1; \\
\text{temp1}[31:0] &\leftarrow \text{INT32}((\text{SRC}[31:16] * \text{SRC}[31:16]) \gg 14) + 1; \\
\text{temp2}[31:0] &\leftarrow \text{INT32}((\text{SRC}[47:32] * \text{SRC}[47:32]) \gg 14) + 1; \\
\text{temp3}[31:0] &\leftarrow \text{INT32}((\text{SRC}[63:48] * \text{SRC}[63:48]) \gg 14) + 1; \\
\text{temp4}[31:0] &\leftarrow \text{INT32}((\text{SRC}[79:64] * \text{SRC}[79:64]) \gg 14) + 1; \\
\text{temp5}[31:0] &\leftarrow \text{INT32}((\text{SRC}[95:80] * \text{SRC}[95:80]) \gg 14) + 1; \\
\text{temp6}[31:0] &\leftarrow \text{INT32}((\text{SRC}[111:96] * \text{SRC}[111:96]) \gg 14) + 1; \\
\text{temp7}[31:0] &\leftarrow \text{INT32}((\text{SRC}[127:112] * \text{SRC}[127:112]) \gg 14) + 1;
\end{align*}
\]
temp7[31:0] ← INT32 ((SRC1[127:112] * SRC2[127:112]) >>14) + 1
DEST[15:0] ← temp0[16:1]
DEST[31:16] ← temp1[16:1]
DEST[47:32] ← temp2[16:1]
DEST[63:48] ← temp3[16:1]
DEST[79:64] ← temp4[16:1]
DEST[95:80] ← temp5[16:1]
DEST[111:96] ← temp6[16:1]
DEST[127:112] ← temp7[16:1]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PMULHRSW: __m64 _mm_mulhrs_pi16 (__m64 a, __m64 b)
PMULHRSW: __m128i _mm_mulhrs_epi16 (__m128i a, __m128i b)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
## PMULHUW—Multiply Packed Unsigned Integers and Store High Result

### Opcode/ Instruction

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F E4 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Multiply the packed unsigned word integers in <code>mm1</code> register and <code>mm2/m64</code>, and store the high 16 bits of the results in <code>mm1</code>.</td>
</tr>
<tr>
<td>66 0F E4 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Multiply the packed unsigned word integers in <code>xmm1</code> and <code>xmm2/m128</code>, and store the high 16 bits of the results in <code>xmm1</code>.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG E4 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply the packed unsigned word integers in <code>xmm2</code> and <code>xmm3/m128</code>, and store the high 16 bits of the results in <code>xmm1</code>.</td>
</tr>
</tbody>
</table>

### Notes:


### Instruction Operand Encoding

<table>
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<tr>
<th>Op/En</th>
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<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Performs a SIMD unsigned multiply of the packed unsigned word integers in the destination operand (first operand) and the source operand (second operand), and stores the high 16 bits of each 32-bit intermediate results in the destination operand. (Figure 4-7 shows this operation when using 64-bit operands.) The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**PMULHUW (with 64-bit operands)**

\[
\begin{align*}
\text{TEMP0}[31:0] &\leftarrow \text{DEST}[15:0] \times \text{SRC}[15:0]; (* \text{Unsigned multiplication} *) \\
\text{TEMP1}[31:0] &\leftarrow \text{DEST}[31:16] \times \text{SRC}[31:16]; \\
\text{TEMP2}[31:0] &\leftarrow \text{DEST}[47:32] \times \text{SRC}[47:32]; \\
\text{TEMP3}[31:0] &\leftarrow \text{DEST}[63:48] \times \text{SRC}[63:48]; \\
\text{DEST}[15:0] &\leftarrow \text{TEMP0}[31:16]; \\
\text{DEST}[31:16] &\leftarrow \text{TEMP1}[31:16]; \\
\text{DEST}[47:32] &\leftarrow \text{TEMP2}[31:16]; \\
\text{DEST}[63:48] &\leftarrow \text{TEMP3}[31:16];
\end{align*}
\]

**PMULHUW (with 128-bit operands)**

\[
\begin{align*}
\text{TEMP0}[31:0] &\leftarrow \text{DEST}[15:0] \times \text{SRC}[15:0]; (* \text{Unsigned multiplication} *) \\
\text{TEMP1}[31:0] &\leftarrow \text{DEST}[31:16] \times \text{SRC}[31:16]; \\
\text{TEMP2}[31:0] &\leftarrow \text{DEST}[47:32] \times \text{SRC}[47:32]; \\
\text{TEMP3}[31:0] &\leftarrow \text{DEST}[63:48] \times \text{SRC}[63:48]; \\
\text{TEMP4}[31:0] &\leftarrow \text{DEST}[79:64] \times \text{SRC}[79:64]; \\
\text{TEMP5}[31:0] &\leftarrow \text{DEST}[95:80] \times \text{SRC}[95:80]; \\
\text{TEMP6}[31:0] &\leftarrow \text{DEST}[111:96] \times \text{SRC}[111:96]; \\
\text{TEMP7}[31:0] &\leftarrow \text{DEST}[127:112] \times \text{SRC}[127:112]; \\
\text{DEST}[15:0] &\leftarrow \text{TEMP0}[31:16]; \\
\text{DEST}[31:16] &\leftarrow \text{TEMP1}[31:16]; \\
\text{DEST}[47:32] &\leftarrow \text{TEMP2}[31:16]; \\
\text{DEST}[63:48] &\leftarrow \text{TEMP3}[31:16]; \\
\text{DEST}[79:64] &\leftarrow \text{TEMP4}[31:16];
\end{align*}
\]

Figure 4-7. PMULHUW and PMULHW Instruction Operation Using 64-bit Operands
PMULHUW—Multiply Packed Unsigned Integers and Store High Result

DEST[95:80] ← TEMP5[31:16];
DEST[111:96] ← TEMP6[31:16];
DEST[127:112] ← TEMP7[31:16];

VPMULHUw (VEX.128 encoded version)
TEMP0[31:0] ← SRC1[15:0] * SRC2[15:0]
TEMP1[31:0] ← SRC1[31:16] * SRC2[31:16]
TEMP4[31:0] ← SRC1[79:64] * SRC2[79:64]
TEMP5[31:0] ← SRC1[95:80] * SRC2[95:80]
TEMP6[31:0] ← SRC1[111:96] * SRC2[111:96]
DEST[15:0] ← TEMP0[31:16]
DEST[31:16] ← TEMP1[31:16]
DEST[47:32] ← TEMP2[31:16]
DEST[63:48] ← TEMP3[31:16]
DEST[79:64] ← TEMP4[31:16]
DEST[95:80] ← TEMP5[31:16]
DEST[111:96] ← TEMP6[31:16]
DEST[127:112] ← TEMP7[31:16]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMULHUw: __m64 _mm_mulhi_pu16(__m64 a, __m64 b)
PMULHUw: __m128i _mm_mulhi_epu16 (__m128i a, __m128i b)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PMULHW—Multiply Packed Signed Integers and Store High Result

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F E5 /r&lt;sup&gt;1&lt;/sup&gt; PMULHW mm, mm/m64</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Multiply the packed signed word integers in mm1 register and mm2/m64, and store the high 16 bits of the results in mm1.</td>
</tr>
<tr>
<td>66 0F E5 /r PMULHW xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Multiply the packed signed word integers in xmm1 and xmm2/m128, and store the high 16 bits of the results in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG E5 /r VPMULHW xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply the packed signed word integers in xmm2 and xmm3/m128, and store the high 16 bits of the results in xmm1.</td>
</tr>
</tbody>
</table>

NOTES:


### Instruction Operand Encoding

<table>
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<tr>
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<td>ModRMreg (r, w)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/r (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Performs a SIMD signed multiply of the packed signed word integers in the destination operand (first operand) and the source operand (second operand), and stores the high 16 bits of each intermediate 32-bit result in the destination operand. (Figure 4-7 shows this operation when using 64-bit operands.) The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

PMULHW (with 64-bit operands)

\[
\begin{align*}
\text{TEMP0}[31:0] &\leftarrow \text{DEST}[15:0] \times \text{SRC}[15:0]; (* \text{Signed multiplication} *) \\
\text{TEMP1}[31:0] &\leftarrow \text{DEST}[31:16] \times \text{SRC}[31:16]; \\
\text{TEMP2}[31:0] &\leftarrow \text{DEST}[47:32] \times \text{SRC}[47:32]; \\
\text{TEMP3}[31:0] &\leftarrow \text{DEST}[63:48] \times \text{SRC}[63:48]; \\
\text{DEST}[15:0] &\leftarrow \text{TEMP0}[31:16]; \\
\text{DEST}[31:16] &\leftarrow \text{TEMP1}[31:16]; \\
\text{DEST}[47:32] &\leftarrow \text{TEMP2}[31:16]; \\
\text{DEST}[63:48] &\leftarrow \text{TEMP3}[31:16]; \\
\end{align*}
\]

PMULHW (with 128-bit operands)

\[
\begin{align*}
\text{TEMP0}[31:0] &\leftarrow \text{DEST}[15:0] \times \text{SRC}[15:0]; (* \text{Signed multiplication} *) \\
\text{TEMP1}[31:0] &\leftarrow \text{DEST}[31:16] \times \text{SRC}[31:16]; \\
\text{TEMP2}[31:0] &\leftarrow \text{DEST}[47:32] \times \text{SRC}[47:32]; \\
\text{TEMP3}[31:0] &\leftarrow \text{DEST}[63:48] \times \text{SRC}[63:48]; \\
\text{TEMP4}[31:0] &\leftarrow \text{DEST}[79:64] \times \text{SRC}[79:64]; \\
\text{TEMP5}[31:0] &\leftarrow \text{DEST}[95:80] \times \text{SRC}[95:80]; \\
\text{TEMP6}[31:0] &\leftarrow \text{DEST}[111:96] \times \text{SRC}[111:96]; \\
\text{TEMP7}[31:0] &\leftarrow \text{DEST}[127:112] \times \text{SRC}[127:112]; \\
\text{DEST}[15:0] &\leftarrow \text{TEMP0}[31:16]; \\
\text{DEST}[31:16] &\leftarrow \text{TEMP1}[31:16]; \\
\text{DEST}[47:32] &\leftarrow \text{TEMP2}[31:16]; \\
\text{DEST}[63:48] &\leftarrow \text{TEMP3}[31:16]; \\
\text{DEST}[79:64] &\leftarrow \text{TEMP4}[31:16]; \\
\text{DEST}[95:80] &\leftarrow \text{TEMP5}[31:16]; \\
\text{DEST}[111:96] &\leftarrow \text{TEMP6}[31:16]; \\
\text{DEST}[127:112] &\leftarrow \text{TEMP7}[31:16]; \\
\end{align*}
\]

VPMULHW (VEX.128 encoded version)

\[
\begin{align*}
\text{TEMP0}[31:0] &\leftarrow \text{SRC1}[15:0] \times \text{SRC2}[15:0] (* \text{Signed Multiplication} *) \\
\text{TEMP1}[31:0] &\leftarrow \text{SRC1}[31:16] \times \text{SRC2}[31:16] \\
\text{TEMP2}[31:0] &\leftarrow \text{SRC1}[47:32] \times \text{SRC2}[47:32] \\
\text{TEMP3}[31:0] &\leftarrow \text{SRC1}[63:48] \times \text{SRC2}[63:48] \\
\text{TEMP4}[31:0] &\leftarrow \text{SRC1}[79:64] \times \text{SRC2}[79:64] \\
\text{TEMP5}[31:0] &\leftarrow \text{SRC1}[95:80] \times \text{SRC2}[95:80] \\
\text{TEMP6}[31:0] &\leftarrow \text{SRC1}[111:96] \times \text{SRC2}[111:96] \\
\text{TEMP7}[31:0] &\leftarrow \text{SRC1}[127:112] \times \text{SRC2}[127:112] \\
\end{align*}
\]
DEST[15:0] ← TEMP0[31:16]
DEST[31:16] ← TEMP1[31:16]
DEST[47:32] ← TEMP2[31:16]
DEST[63:48] ← TEMP3[31:16]
DEST[79:64] ← TEMP4[31:16]
DEST[95:80] ← TEMP5[31:16]
DEST[111:96] ← TEMP6[31:16]
DEST[127:112] ← TEMP7[31:16]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMULHw: _m64 _mm_mulhi_pi16 (_m64 m1, _m64 m2)
PMULHw: _m128i _mm_mulhi_epi16 (_m128i a, _m128i b)

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PMULLD — Multiply Packed Signed Dword Integers and Store Low Result

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 40 /r PMULLD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Multiply the packed dword signed integers in xmm1 and xmm2/m128 and store the low 32 bits of each product in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 40 /r VPMULLD xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply the packed dword signed integers in xmm2 and xmm3/m128 and store the low 32 bits of each product in xmm1.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

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<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs four signed multiplications from four pairs of signed dword integers and stores the lower 32 bits of the four 64-bit products in the destination operand (first operand). Each dword element in the destination operand is multiplied with the corresponding dword element of the source operand (second operand) to obtain a 64-bit intermediate product.

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

Temp[63:0] ← DEST[31:0] * SRC[31:0];
Temp[63:0] ← DEST[95:64] * SRC[95:64];
Temp[63:0] ← DEST[127:96] * SRC[127:96];
DEST[31:0] ← Temp[31:0];
DEST[63:32] ← Temp[31:0];
DEST[95:64] ← Temp[31:0];
PMULLD — Multiply Packed Signed Dword Integers and Store Low Result

**INSTRUCTION SET REFERENCE, M-Z**

DEST[127:96] ← Temp3[31:0];

**VPMULLD (VEX.128 encoded version)**
Temp0[63:0] ← SRC1[31:0] * SRC2[31:0]
Temp2[63:0] ← SRC1[95:64] * SRC2[95:64]
DEST[31:0] ← Temp0[31:0]
DEST[63:32] ← Temp1[31:0]
DEST[95:64] ← Temp2[31:0]
DEST[127:96] ← Temp3[31:0]
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

PMULLD:  __m128i _mm_mullo_epi32(__m128i a, __m128i b);

**Flags Affected**

None.

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD  If VEX.L = 1.
PMULLW—Multiply Packed Signed Integers and Store Low Result

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>0F D5 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Multiply the packed signed word integers in mm1 register and mm2/m64, and store the low 16 bits of the results in mm1.</td>
</tr>
<tr>
<td>PMULLW mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F D5 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Multiply the packed signed word integers in xmm1 and xmm2/m128, and store the low 16 bits of the results in xmm1.</td>
</tr>
<tr>
<td>PMULLW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F:WIG D5 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply the packed dword signed integers in xmm2 and xmm3/m128 and store the low 32 bits of each product in xmm1.</td>
</tr>
<tr>
<td>VPMULLW xmm1, xmm2, xmm3/m128</td>
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NOTES:

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<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a SIMD signed multiply of the packed signed word integers in the destination operand (first operand) and the source operand (second operand), and stores the low 16 bits of each intermediate 32-bit result in the destination operand. (Figure 4-7 shows this operation when using 64-bit operands.) The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

### Operation

**PMULLW (with 64-bit operands)**

\[
\begin{align*}
\text{TEMP0}[31:0] &\leftarrow \text{DEST}[15:0] \times \text{SRC}[15:0]; (* \text{Signed multiplication } *) \\
\text{TEMP1}[31:0] &\leftarrow \text{DEST}[31:16] \times \text{SRC}[31:16]; \\
\text{TEMP2}[31:0] &\leftarrow \text{DEST}[47:32] \times \text{SRC}[47:32]; \\
\text{TEMP3}[31:0] &\leftarrow \text{DEST}[63:48] \times \text{SRC}[63:48]; \\
\text{DEST}[15:0] &\leftarrow \text{TEMP0}[15:0]; \\
\text{DEST}[31:16] &\leftarrow \text{TEMP1}[15:0]; \\
\text{DEST}[47:32] &\leftarrow \text{TEMP2}[15:0]; \\
\text{DEST}[63:48] &\leftarrow \text{TEMP3}[15:0];
\end{align*}
\]

**PMULLW (with 128-bit operands)**

\[
\begin{align*}
\text{TEMP0}[31:0] &\leftarrow \text{DEST}[15:0] \times \text{SRC}[15:0]; (* \text{Signed multiplication } *) \\
\text{TEMP1}[31:0] &\leftarrow \text{DEST}[31:16] \times \text{SRC}[31:16]; \\
\text{TEMP2}[31:0] &\leftarrow \text{DEST}[47:32] \times \text{SRC}[47:32]; \\
\text{TEMP3}[31:0] &\leftarrow \text{DEST}[63:48] \times \text{SRC}[63:48]; \\
\text{TEMP4}[31:0] &\leftarrow \text{DEST}[79:64] \times \text{SRC}[79:64]; \\
\text{TEMP5}[31:0] &\leftarrow \text{DEST}[95:80] \times \text{SRC}[95:80]; \\
\text{TEMP6}[31:0] &\leftarrow \text{DEST}[111:96] \times \text{SRC}[111:96]; \\
\text{TEMP7}[31:0] &\leftarrow \text{DEST}[127:112] \times \text{SRC}[127:112]; \\
\text{DEST}[15:0] &\leftarrow \text{TEMP0}[15:0]; \\
\text{DEST}[31:16] &\leftarrow \text{TEMP1}[15:0]; \\
\text{DEST}[47:32] &\leftarrow \text{TEMP2}[15:0]; \\
\text{DEST}[63:48] &\leftarrow \text{TEMP3}[15:0]; \\
\text{DEST}[79:64] &\leftarrow \text{TEMP4}[15:0];
\end{align*}
\]
PMULLW—Multiply Packed Signed Integers and Store Low Result

DEST[95:80] ← TEMP5[15:0];
DEST[111:96] ← TEMP6[15:0];
DEST[127:112] ← TEMP7[15:0];

VPMULLW (VEX.128 encoded version)
Temp0[31:0] ← SRC1[15:0] * SRC2[15:0]
Temp1[31:0] ← SRC1[31:16] * SRC2[31:16]
Temp4[31:0] ← SRC1[79:64] * SRC2[79:64]
Temp5[31:0] ← SRC1[95:80] * SRC2[95:80]
Temp6[31:0] ← SRC1[111:96] * SRC2[111:96]
DEST[15:0] ← Temp0[15:0]
DEST[31:16] ← Temp1[15:0]
DEST[47:32] ← Temp2[15:0]
DEST[63:48] ← Temp3[15:0]
DEST[79:64] ← Temp4[15:0]
DEST[95:80] ← Temp5[15:0]
DEST[111:96] ← Temp6[15:0]
DEST[127:112] ← Temp7[15:0]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PMULLW: __m64 _mm_mullo_pi16(__m64 m1, __m64 m2)
PMULLW: __m128i _mm_mullo_epi16 ( __m128i a, __m128i b)

Flags Affected
None.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PMULUDQ—Multiply Packed Unsigned Doubleword Integers

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F F4 /r (^1)</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Multiply unsigned doubleword integer in (mm1) by unsigned doubleword integer in (mm2/m64), and store the quadword result in (mm1).</td>
</tr>
<tr>
<td>PMULUDQ (mm1, mm2/m64)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F F4 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Multiply packed unsigned doubleword integers in (xmm1) by packed unsigned doubleword integers in (xmm2/m128), and store the quadword results in (xmm1).</td>
</tr>
<tr>
<td>PMULUDQ (xmm1, xmm2/m128)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG F4 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Multiply packed unsigned doubleword integers in (xmm2) by packed unsigned doubleword integers in (xmm3/m128), and store the quadword results in (xmm1).</td>
</tr>
<tr>
<td>VPMULUDQ (xmm1, xmm2, xmm3/m128)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Multiplies the first operand (destination operand) by the second operand (source operand) and stores the result in the destination operand. The source operand can be an unsigned doubleword integer stored in the low doubleword of an MMX technology register or a 64-bit memory location, or it can be two packed unsigned doubleword integers stored in the first (low) and third doublewords of an XMM register or an 128-bit memory location. The destination operand can be an unsigned doubleword integer stored in the low doubleword an MMX technology register or two packed doubleword integers stored in the first and third doublewords of an XMM register. The
result is an unsigned quadword integer stored in the destination an MMX technology register or two packed unsigned quadword integers stored in an XMM register. When a quadword result is too large to be represented in 64 bits (overflow), the result is wrapped around and the low 64 bits are written to the destination element (that is, the carry is ignored).

For 64-bit memory operands, 64 bits are fetched from memory, but only the low doubleword is used in the computation; for 128-bit memory operands, 128 bits are fetched from memory, but only the first and third doublewords are used in the computation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PMULUDQ (with 64-Bit operands)**

\[ \text{DEST}[63:0] \leftarrow \text{DEST}[31:0] \times \text{SRC}[31:0]; \]

**PMULUDQ (with 128-Bit operands)**

\[ \text{DEST}[63:0] \leftarrow \text{DEST}[31:0] \times \text{SRC}[31:0]; \]
\[ \text{DEST}[127:64] \leftarrow \text{DEST}[95:64] \times \text{SRC}[95:64]; \]

**VPMULUDQ (VEX.128 encoded version)**

\[ \text{DEST}[63:0] \leftarrow \text{SRC1}[31:0] \times \text{SRC2}[31:0] \]
\[ \text{DEST}[127:64] \leftarrow \text{SRC1}[95:64] \times \text{SRC2}[95:64] \]
\[ \text{DEST}[\text{VLMAX}-1:128] \leftarrow 0 \]

**Intel C/C++ Compiler Intrinsic Equivalent**

PMULUDQ: \_m64 \_mm\_mul\_su32 (\_m64 a, \_m64 b)

PMULUDQ: \_m128i \_mm\_mul\_epu32 (\_m128i a, \_m128i b)

**Flags Affected**

None.

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally
INSTRUCTION SET REFERENCE, M-Z

#UD If VEX.L = 1.
## POP—Pop a Value from the Stack

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8F /0</td>
<td>POP r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Pop top of stack into ( m16 ); increment stack pointer.</td>
</tr>
<tr>
<td>8F /0</td>
<td>POP r/m32</td>
<td>M</td>
<td>N.E.</td>
<td>Valid</td>
<td>Pop top of stack into ( m32 ); increment stack pointer.</td>
</tr>
<tr>
<td>8F /0</td>
<td>POP r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Pop top of stack into ( m64 ); increment stack pointer. Cannot encode 32-bit operand size.</td>
</tr>
<tr>
<td>58+ rw</td>
<td>POP r16</td>
<td>O</td>
<td>Valid</td>
<td>Valid</td>
<td>Pop top of stack into ( r16 ); increment stack pointer.</td>
</tr>
<tr>
<td>58+ rd</td>
<td>POP r32</td>
<td>O</td>
<td>N.E.</td>
<td>Valid</td>
<td>Pop top of stack into ( r32 ); increment stack pointer.</td>
</tr>
<tr>
<td>58+ rd</td>
<td>POP r64</td>
<td>O</td>
<td>Valid</td>
<td>N.E.</td>
<td>Pop top of stack into ( r64 ); increment stack pointer. Cannot encode 32-bit operand size.</td>
</tr>
<tr>
<td>1F</td>
<td>POP DS</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Pop top of stack into DS; increment stack pointer.</td>
</tr>
<tr>
<td>07</td>
<td>POP ES</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Pop top of stack into ES; increment stack pointer.</td>
</tr>
<tr>
<td>17</td>
<td>POP SS</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Pop top of stack into SS; increment stack pointer.</td>
</tr>
<tr>
<td>0F A1</td>
<td>POP FS</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Pop top of stack into FS; increment stack pointer by 16 bits.</td>
</tr>
<tr>
<td>0F A1</td>
<td>POP FS</td>
<td>NP</td>
<td>N.E.</td>
<td>Valid</td>
<td>Pop top of stack into FS; increment stack pointer by 32 bits.</td>
</tr>
<tr>
<td>0F A1</td>
<td>POP FS</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Pop top of stack into FS; increment stack pointer by 64 bits.</td>
</tr>
<tr>
<td>0F A9</td>
<td>POP GS</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Pop top of stack into GS; increment stack pointer by 16 bits.</td>
</tr>
<tr>
<td>0F A9</td>
<td>POP GS</td>
<td>NP</td>
<td>N.E.</td>
<td>Valid</td>
<td>Pop top of stack into GS; increment stack pointer by 32 bits.</td>
</tr>
</tbody>
</table>
**Description**

Loads the value from the top of the stack to the location specified with the destination operand (or explicit opcode) and then increments the stack pointer. The destination operand can be a general-purpose register, memory location, or segment register.

Address and operand sizes are determined and used as follows:

- **Address size.** The D flag in the current code-segment descriptor determines the default address size; it may be overridden by an instruction prefix (67H).
  
  The address size is used only when writing to a destination operand in memory.

- **Operand size.** The D flag in the current code-segment descriptor determines the default operand size; it may be overridden by instruction prefixes (66H or REX.W).
  
  The operand size (16, 32, or 64 bits) determines the amount by which the stack pointer is incremented (2, 4 or 8).

- **Stack-address size.** Outside of 64-bit mode, the B flag in the current stack-segment descriptor determines the size of the stack pointer (16 or 32 bits); in 64-bit mode, the size of the stack pointer is always 64 bits.
  
  The stack-address size determines the width of the stack pointer when reading from the stack in memory and when incrementing the stack pointer. (As stated above, the amount by which the stack pointer is incremented is determined by the operand size.)

If the destination operand is one of the segment registers DS, ES, FS, GS, or SS, the value loaded into the register must be a valid segment selector. In protected mode, popping a segment selector into a segment register automatically causes the descriptor information associated with that segment selector to be loaded into the hidden (shadow) part of the segment register and causes the selector and the descriptor information to be validated (see the "Operation" section below).
A NULL value (0000-0003) may be popped into the DS, ES, FS, or GS register without causing a general protection fault. However, any subsequent attempt to reference a segment whose corresponding segment register is loaded with a NULL value causes a general protection exception (#GP). In this situation, no memory reference occurs and the saved value of the segment register is NULL.

The POP instruction cannot pop a value into the CS register. To load the CS register from the stack, use the RET instruction.

If the ESP register is used as a base register for addressing a destination operand in memory, the POP instruction computes the effective address of the operand after it increments the ESP register. For the case of a 16-bit stack where ESP wraps to 0H as a result of the POP instruction, the resulting location of the memory write is processor-family-specific.

The POP ESP instruction increments the stack pointer (ESP) before data at the old top of stack is written into the destination.

A POP SS instruction inhibits all interrupts, including the NMI interrupt, until after execution of the next instruction. This action allows sequential execution of POP SS and MOV ESP, EBP instructions without the danger of having an invalid stack during an interrupt\(^1\). However, use of the LSS instruction is the preferred method of loading the SS and ESP registers.

In 64-bit mode, using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). When in 64-bit mode, POPs using 32-bit operands are not encodable and POPs to DS, ES, SS are not valid. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\begin{align*}
\text{IF StackAddrSize} &= 32 \\
& \quad \text{THEN} \\
& \quad \quad \text{IF OperandSize} = 32 \\
& \quad \quad \quad \text{THEN} \\
& \quad \quad \quad \quad \text{DEST} \leftarrow \text{SS:ESP}; \; \text{(* Copy a doubleword *)} \\
& \quad \quad \quad \quad \text{ESP} \leftarrow \text{ESP} + 4; \\
& \quad \quad \quad \text{ELSE} \; \text{(* OperandSize = 16*)} \\
& \quad \quad \quad \quad \text{DEST} \leftarrow \text{SS:ESP}; \; \text{(* Copy a word *)}
\end{align*}
\]

1. If a code instruction breakpoint (for debug) is placed on an instruction located immediately after a POP SS instruction, the breakpoint may not be triggered. However, in a sequence of instructions that POP the SS register, only the first instruction in the sequence is guaranteed to delay an interrupt.

   In the following sequence, interrupts may be recognized before POP ESP executes:

   POP SS
   POP SS
   POP ESP
Loading a segment register while in protected mode results in special actions, as described in the following listing. These checks are performed on the segment selector and the segment descriptor it points to.

64-BIT_MODE
IF FS, or GS is loaded with non-NULL selector;
THEN
   IF segment selector index is outside descriptor table limits
      OR segment is not a data or readable code segment
      OR (segment is a data or nonconforming code segment)
      AND (both RPL and CPL > DPL)
      THEN #GP(selector);
      IF segment not marked present
      THEN #NP(selector);
   ELSE
      SegmentRegister ← segment selector;
      SegmentRegister ← segment descriptor;
   FI;
FI;
**INSTRUCTION SET REFERENCE, M-Z**

**POP—Pop a Value from the Stack**

FL;
IF FS, or GS is loaded with a NULL selector;
    THEN
        SegmentRegister ← segment selector;
        SegmentRegister ← segment descriptor;
    FL;

PRETECTED MODE OR COMPATIBILITY MODE;
IF SS is loaded;
    THEN
        IF segment selector is NULL
            THEN #GP(0);
        FL;
        IF segment selector index is outside descriptor table limits
            or segment selector’s RPL ≠ CPL
            or segment is not a writable data segment
            or DPL ≠ CPL
                THEN #GP(selector);
        FL;
        IF segment not marked present
            THEN #SS(selector);
        ELSE
            SS ← segment selector;
            SS ← segment descriptor;
        FL;
    FL;
IF DS, ES, FS, or GS is loaded with non-NULL selector;
    THEN
        IF segment selector index is outside descriptor table limits
            or segment is not a data or readable code segment
            or ((segment is a data or nonconforming code segment)
                and (both RPL and CPL > DPL))
                THEN #GP(selector);
        FL;
        IF segment not marked present
            THEN #NP(selector);
        ELSE
            SegmentRegister ← segment selector;
            SegmentRegister ← segment descriptor;
        FL;
INSTRUCTION SET REFERENCE, M-Z

FI;

IF DS, ES, FS, or GS is loaded with a NULL selector
 THEN
   SegmentRegister ← segment selector;
   SegmentRegister ← segment descriptor;
FI;

Flags Affected
None.

Protected Mode Exceptions

#GP(0) If attempt is made to load SS register with NULL segment selector.
If the destination operand is in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#GP(selector) If segment selector index is outside descriptor table limits.
If the SS register is being loaded and the segment selector’s RPL and the segment descriptor’s DPL are not equal to the CPL.
If the SS register is being loaded and the segment pointed to is a non-writable data segment.
If the DS, ES, FS, or GS register is being loaded and the segment pointed to is not a data or readable code segment.
If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.
#SS(0) If the current top of stack is not within the stack segment.
If a memory operand effective address is outside the SS segment limit.
#SS(selector) If the SS register is being loaded and the segment pointed to is marked not present.
#NP If the DS, ES, FS, or GS register is being loaded and the segment pointed to is marked not present.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference is made while the current privilege level is 3 and alignment checking is enabled.
#UD If the LOCK prefix is used.
**Real-Address Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#UD** If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If an unaligned memory reference is made while alignment checking is enabled.
- **#UD** If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same as for protected mode exceptions.

**64-Bit Mode Exceptions**

- **#GP(0)** If the memory address is in a non-canonical form.
- **#SS(U)** If the stack address is in a non-canonical form.
- **#GP(selector)** If the descriptor is outside the descriptor table limit.
  - If the FS or GS register is being loaded and the segment pointed to is not a data or readable code segment.
  - If the FS or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.
- **#AC(0)** If an unaligned memory reference is made while alignment checking is enabled.
- **#PF(fault-code)** If a page fault occurs.
- **#NP** If the FS or GS register is being loaded and the segment pointed to is marked not present.
- **#UD** If the LOCK prefix is used.
POPA/POPAD—Pop All General-Purpose Registers

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>61</td>
<td>POPA</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Pop DI, SI, BP, BX, DX, CX, and AX.</td>
</tr>
<tr>
<td>61</td>
<td>POPAD</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Pop EDI, ESI, EBP, EBX, EDX, ECX, and EAX.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Pops doublewords (POPAD) or words (POPA) from the stack into the general-purpose registers. The registers are loaded in the following order: EDI, ESI, EBP, EBX, EDX, ECX, and EAX (if the operand-size attribute is 32) and DI, SI, BP, BX, DX, CX, and AX (if the operand-size attribute is 16). (These instructions reverse the operation of the PUSHA/PUSHAD instructions.) The value on the stack for the ESP or SP register is ignored. Instead, the ESP or SP register is incremented after each register is loaded.

The POPA (pop all) and POPAD (pop all double) mnemonics reference the same opcode. The POPA instruction is intended for use when the operand-size attribute is 16 and the POPAD instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when POPA is used and to 32 when POPAD is used (using the operand-size override prefix [66H] if necessary). Others may treat these mnemonics as synonyms (POPA/POPAD) and use the current setting of the operand-size attribute to determine the size of values to be popped from the stack, regardless of the mnemonic used. (The D flag in the current code segment’s segment descriptor determines the operand-size attribute.)

This instruction executes as described in non-64-bit modes. It is not valid in 64-bit mode.

Operation

IF 64-Bit Mode
THEN
  #UD;
ELSE
  IF OperandSize = 32 (* Instruction = POPAD *)
  THEN
    EDI ← Pop();
    ESI ← Pop();
    EBP ← Pop();
INSTRUCTION SET REFERENCE, M-Z

POPA/POPAD—Pop All General-Purpose Registers

Increment ESP by 4; (* Skip next 4 bytes of stack *)
EBX ← Pop();
EDX ← Pop();
ECX ← Pop();
EAX ← Pop();
ELSE (* OperandSize = 16, instruction = POPA *)
DI ← Pop();
SI ← Pop();
BP ← Pop();
Increment ESP by 2; (* Skip next 2 bytes of stack *)
BX ← Pop();
DX ← Pop();
CX ← Pop();
AX ← Pop();
FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#SS(0) If the starting or ending stack address is not within the stack segment.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference is made while the current privilege level is 3 and alignment checking is enabled.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#SS If the starting or ending stack address is not within the stack segment.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#SS(0) If the starting or ending stack address is not within the stack segment.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference is made while alignment checking is enabled.
#UD If the LOCK prefix is used.
Compatibility Mode Exceptions
Same as for protected mode exceptions.

64-Bit Mode Exceptions
#UD If in 64-bit mode.
POPCNT — Return the Count of Number of Bits Set to 1

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F B8 /r</td>
<td>POPCNT r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>POPCNT on r/m16</td>
</tr>
<tr>
<td>F3 0F B8 /r</td>
<td>POPCNT r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>POPCNT on r/m32</td>
</tr>
<tr>
<td>F3 REX.W 0F B8 /r</td>
<td>POPCNT r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>POPCNT on r/m64</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

This instruction calculates number of bits set to 1 in the second operand (source) and returns the count in the first operand (a destination register).

Operation

Count = 0;
For (i=0; i < OperandSize; i++)
{
    IF (SRC[i] = 1) // i'th bit
        THEN Count++;
    FI;
}

DEST ← Count;

Flags Affected

OF, SF, ZF, AF, CF, PF are all cleared. ZF is set if SRC = 0, otherwise ZF is cleared.

Intel C/C++ Compiler Intrinsic Equivalent

POPCNT:    int _mm_popcnt_u32(unsigned int a);
POPCNT:    int64_t _mm_popcnt_u64(unsigned __int64 a);

Protected Mode Exceptions

#GP(0)     If a memory operand effective address is outside the CS, DS, ES, FS or GS segments.
#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF (fault-code) For a page fault.

#UD If CPUID.01H:ECX.POPCNT [Bit 23] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Real Mode Exceptions
#GP(0) If any part of the operand lies outside of the effective address space from 0 to 0FFFFH.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#UD If CPUID.01H:ECX.POPCNT [Bit 23] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Virtual 8086 Mode Exceptions
#GP(0) If any part of the operand lies outside of the effective address space from 0 to 0FFFFH.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF (fault-code) For a page fault.

#UD If CPUID.01H:ECX.POPCNT [Bit 23] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.

Compatibility Mode Exceptions
Same exceptions as in Protected Mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#PF (fault-code) For a page fault.

#UD If CPUID.01H:ECX.POPCNT [Bit 23] = 0.
If LOCK prefix is used.
Either the prefix REP (F3h) or REPN (F2H) is used.
**POPF/POPFD/POPFQ—Pop Stack into EFLAGS Register**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9D</td>
<td>POPF</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Pop top of stack into lower 16 bits of EFLAGS.</td>
</tr>
<tr>
<td>9D</td>
<td>POPFD</td>
<td>NP</td>
<td>N.E.</td>
<td>Valid</td>
<td>Pop top of stack into EFLAGS.</td>
</tr>
<tr>
<td>REX.W + 9D</td>
<td>POPFQ</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Pop top of stack and zero-extend into RFLAGS.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Pops a doubleword (POPF) from the top of the stack (if the current operand-size attribute is 32) and stores the value in the EFLAGS register, or pops a word from the top of the stack (if the operand-size attribute is 16) and stores it in the lower 16 bits of the EFLAGS register (that is, the FLAGS register). These instructions reverse the operation of the PUSHF/PUSHFD instructions.

The POPF (pop flags) and POPFD (pop flags double) mnemonics reference the same opcode. The POPF instruction is intended for use when the operand-size attribute is 16; the POPFD instruction is intended for use when the operand-size attribute is 32. Some assemblers may force the operand size to 16 for POPF and to 32 for POPFD. Others may treat the mnemonics as synonyms (POPF/POPFD) and use the setting of the operand-size attribute to determine the size of values to pop from the stack.

The effect of POPF/POPFD on the EFLAGS register changes, depending on the mode of operation. When the processor is operating in protected mode at privilege level 0 (or in real-address mode, the equivalent to privilege level 0), all non-reserved flags in the EFLAGS register except RF, VIP, VIF, and VM may be modified. VIP, VIF and VM remain unaffected.

When operating in protected mode with a privilege level greater than 0, but less than or equal to IOPL, all flags can be modified except the IOPL field and VIP, VIF, and VM. Here, the IOPL flags are unaffected, the VIP and VIF flags are cleared, and the VM flag is unaffected. The interrupt flag (IF) is altered only when executing at a level at least as privileged as the IOPL. If a POPF/POPFD instruction is executed with insufficient privilege, an exception does not occur but privileged bits do not change.

---

1. RF is always zero after the execution of POPF. This is because POPF, like all instructions, clears RF as it begins to execute.
When operating in virtual-8086 mode, the IOPL must be equal to 3 to use POPF/POPFD instructions; VM, RF, IOPL, VIP, and VIF are unaffected. If the IOPL is less than 3, POPF/POPFD causes a general-protection exception (#GP).

In 64-bit mode, use REX.W to pop the top of stack to RFLAGS. The mnemonic assigned is POPFQ (note that the 32-bit operand is not encodable). POPFQ pops 64 bits from the stack, loads the lower 32 bits into RFLAGS, and zero extends the upper bits of RFLAGS.

See Chapter 3 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information about the EFLAGS registers.

**Operation**

IF VM = 0 (* Not in Virtual-8086 Mode *)
THEN IF CPL = 0
THEN
IF OperandSize = 32;
THEN
EFLAGS ← Pop(); (* 32-bit pop *)
(* All non-reserved flags except RF, VIP, VIF, and VM can be modified; VIP and VIF are cleared; RF, VM, and all reserved bits are unaffected. *)
ELSE IF (Operandsize = 64)
RFLAGS = Pop(); (* 64-bit pop *)
(* All non-reserved flags except RF, VIP, VIF, and VM can be modified; VIP and VIF are cleared; RF, VM, and all reserved bits are unaffected.*)
ELSE (* OperandSize = 16 *)
EFLAGS[15:0] ← Pop(); (* 16-bit pop *)
(* All non-reserved flags can be modified. *)
FI;
ELSE (* CPL > 0 *)
IF OperandSize = 32
THEN
IF CPL > IOPL
THEN
EFLAGS ← Pop(); (* 32-bit pop *)
(* All non-reserved bits except IF, IOPL, RF, VIP, and VIF can be modified; IF, IOPL, RF, VM, and all reserved bits are unaffected; VIP and VIF are cleared. *)
ELSE
EFLAGS ← Pop(); (* 32-bit pop *)
(* All non-reserved bits except IOPL, RF, VIP, and VIF can be modified; IOPL, RF, VM, and all reserved bits are unaffected; VIP and VIF are cleared. *)
FI;
ELSE IF (Operandsize = 64)
    IF CPL > IOPL
        THEN
            RFLAGS ← Pop(); (* 64-bit pop *)
            (* All non-reserved bits except IF, IOPL, RF, VIP, and
             VIF can be modified; IF, IOPL, RF, VM, and all reserved
             bits are unaffected; VIP and VIF are cleared. *)
        ELSE
            RFLAGS ← Pop(); (* 64-bit pop *)
            (* All non-reserved bits except IOPL, RF, VIP, and VIF can be
             modified; IOPL, RF, VM, and all reserved bits are
             unaffected; VIP and VIF are cleared. *)
        FI;
    ELSE (* OperandSize = 16 *)
        EFLAGS[15:0] ← Pop(); (* 16-bit pop *)
        (* All non-reserved bits except IOPL can be modified; IOPL and all
         reserved bits are unaffected. *)
    FI;
ELSE (* In Virtual-8086 Mode *)
    IF IOPL = 3
        THEN IF OperandSize = 32
            THEN
                EFLAGS ← Pop();
                (* All non-reserved bits except VM, RF, IOPL, VIP, and VIF can be
                 modified; VM, RF, IOPL, VIP, VIF, and all reserved bits are unaffected. *)
            ELSE
                EFLAGS[15:0] ← Pop(); FI;
                (* All non-reserved bits except IOPL can be modified; IOPL and all
                 reserved bits are unaffected. *)
            ELSE (* IOPL < 3 *)
                #GP(0); (* Trap to virtual-8086 monitor. *)
            FI;
        FI;
    FI;

Flags Affected
All flags may be affected; see the Operation section for details.

Protected Mode Exceptions
#SS(0) If the top of stack is not within the stack segment.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference is made while the current privilege level is 3 and alignment checking is enabled.

#UD If the LOCK prefix is used.

### Real-Address Mode Exceptions

#SS If the top of stack is not within the stack segment.

#UD If the LOCK prefix is used.

### Virtual-8086 Mode Exceptions

#GP(0) If the I/O privilege level is less than 3.
If an attempt is made to execute the POPF/POPFD instruction with an operand-size override prefix.

#SS(0) If the top of stack is not within the stack segment.

#PF(fault-code) If a page fault occurs.

#AC(0) If an unaligned memory reference is made while alignment checking is enabled.

#UD If the LOCK prefix is used.

### Compatibility Mode Exceptions

Same as for protected mode exceptions.

### 64-Bit Mode Exceptions

#GP(0) If the memory address is in a non-canonical form.

#SS(0) If the stack address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
**POR—Bitwise Logical OR**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF EB /r³</td>
<td>POR mm, mm/m64</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Bitwise OR of mm/m64 and mm.</td>
</tr>
<tr>
<td>66 OF EB /r</td>
<td>POR xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Bitwise OR of xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F0G EB /r</td>
<td>VPOR xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Bitwise OR of xmm2/m128 and xmm3.</td>
</tr>
</tbody>
</table>

**NOTES:**


**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical OR operation on the source operand (second operand) and the destination operand (first operand) and stores the result in the destination operand. The source operand can be an MMX technology register or a 64-bit memory location or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register. Each bit of the result is set to 1 if either or both of the corresponding bits of the first and second operands are 1; otherwise, it is set to 0.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**POR (128-bit Legacy SSE version)**
DEST ← DEST OR SRC
DEST[VLMAX-1:128] (Unmodified)

**VPOR (VEX.128 encoded version)**
DEST ← SRC1 OR SRC2
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**
POR: __m64 _mm_or_si64(__m64 m1, __m64 m2)
POR: __m128i _mm_or_si128(__m128i m1, __m128i m2)

**Flags Affected**
None.

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PREFETCHh—Prefetch Data Into Caches

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 18 /1</td>
<td>PREFETCHT0 m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Move data from m8 closer to the processor using T0 hint.</td>
</tr>
<tr>
<td>0F 18 /2</td>
<td>PREFETCHT1 m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Move data from m8 closer to the processor using T1 hint.</td>
</tr>
<tr>
<td>0F 18 /3</td>
<td>PREFETCHT2 m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Move data from m8 closer to the processor using T2 hint.</td>
</tr>
<tr>
<td>0F 18 /0</td>
<td>PREFETCHNTA m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Move data from m8 closer to the processor using NTA hint.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Fetches the line of data from memory that contains the byte specified with the source operand to a location in the cache hierarchy specified by a locality hint:

- **T0** (temporal data)—prefetch data into all levels of the cache hierarchy.
  - Pentium III processor—1st- or 2nd-level cache.
  - Pentium 4 and Intel Xeon processors—2nd-level cache.
- **T1** (temporal data with respect to first level cache)—prefetch data into level 2 cache and higher.
  - Pentium III processor—2nd-level cache.
  - Pentium 4 and Intel Xeon processors—2nd-level cache.
- **T2** (temporal data with respect to second level cache)—prefetch data into level 2 cache and higher.
  - Pentium III processor—2nd-level cache.
  - Pentium 4 and Intel Xeon processors—2nd-level cache.
- **NTA** (non-temporal data with respect to all cache levels)—prefetch data into non-temporal cache structure and into a location close to the processor, minimizing cache pollution.
  - Pentium III processor—1st-level cache.
PREFETCHh—Prefetch Data Into Caches

The source operand is a byte memory location. (The locality hints are encoded into the machine level instruction using bits 3 through 5 of the ModR/M byte. Use of any ModR/M value other than the specified ones will lead to unpredictable behavior.)

If the line selected is already present in the cache hierarchy at a level closer to the processor, no data movement occurs. Prefetches from uncacheable or WC memory are ignored.

The PREFETCHh instruction is merely a hint and does not affect program behavior. If executed, this instruction moves data closer to the processor in anticipation of future use.

The implementation of prefetch locality hints is implementation-dependent, and can be overloaded or ignored by a processor implementation. The amount of data prefetched is also processor implementation-dependent. It will, however, be a minimum of 32 bytes.

It should be noted that processors are free to speculatively fetch and cache data from system memory regions that are assigned a memory-type that permits speculative reads (that is, the WB, WC, and WT memory types). A PREFETCHh instruction is considered a hint to this speculative behavior. Because this speculative fetching can occur at any time and is not tied to instruction execution, a PREFETCHh instruction is not ordered with respect to the fence instructions (MFENCE, SFENCE, and LFENCE) or locked memory references. A PREFETCHh instruction is also unordered with respect to CLFLUSH instructions, other PREFETCHh instructions, or any other general instruction. It is ordered with respect to serializing instructions such as CPUID, WRMSR, OUT, and MOV CR.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

Operation

FETCH (m8);

Intel C/C++ Compiler Intrinsic Equivalent

void _mm_prefetch(char *p, int i)

The argument "*p" gives the address of the byte (and corresponding cache line) to be prefetched. The value "i" gives a constant (_MM_HINT_T0, _MM_HINT_T1, _MM_HINT_T2, or _MM_HINT_NTA) that specifies the type of prefetch operation to be performed.

Numeric Exceptions

None.
Exceptions (All Operating Modes)

#UD If the LOCK prefix is used.
**INSTRUCTION SET REFERENCE, M-Z**

**PSADBW—Compute Sum of Absolute Differences**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F F6 /r 1</td>
<td>RM V/V</td>
<td>SSE</td>
<td></td>
<td>Computes the absolute differences of the packed unsigned byte integers from mm2 /m64 and mm1; differences are then summed to produce an unsigned word integer result.</td>
</tr>
<tr>
<td>PSADBW mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F F6 /r</td>
<td>RM V/V</td>
<td>SSE2</td>
<td></td>
<td>Computes the absolute differences of the packed unsigned byte integers from xmm2 /m128 and xmm1; the 8 low differences and 8 high differences are then summed separately to produce two unsigned word integer results.</td>
</tr>
<tr>
<td>PSADBW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG F6 /r</td>
<td>RVM V/V</td>
<td>AVX</td>
<td></td>
<td>Computes the absolute differences of the packed unsigned byte integers from xmm3 /m128 and xmm2; the 8 low differences and 8 high differences are then summed separately to produce two unsigned word integer results.</td>
</tr>
<tr>
<td>VPSADBW xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**


**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX:vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**
Computes the absolute value of the difference of 8 unsigned byte integers from the source operand (second operand) and from the destination operand (first operand). These 8 differences are then summed to produce an unsigned word integer result that is stored in the destination operand. The source operand can be an MMX technology register or a 64-bit memory location or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register. Figure 4-9 shows the operation of the PSADBW instruction when using 64-bit operands.

When operating on 64-bit operands, the word integer result is stored in the low word of the destination operand, and the remaining bytes in the destination operand are cleared to all 0s.

When operating on 128-bit operands, two packed results are computed. Here, the 8 low-order bytes of the source and destination operands are operated on to produce a word result that is stored in the low word of the destination operand, and the 8 high-order bytes are operated on to produce a word result that is stored in bits 64 through 79 of the destination operand. The remaining bytes of the destination operand are cleared.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

PSADBW (when using 64-bit operands)

\[
\text{TEMP0} \leftarrow \text{ABS(Dest[7:0] – Src[7:0]}; \\
\text{(* Repeat operation for bytes 2 through 6 *)} \\
\text{TEMP7} \leftarrow \text{ABS(Dest[63:56] – Src[63:56]);}
\]
DEST[15:0] ← SUM(TEMP0:TEMP7);
DEST[63:16] ← 000000000000H;

**PSADBW (when using 128-bit operands)**

TEMP0 ← ABS(DEST[7:0] − SRC[7:0]);
(* Repeat operation for bytes 2 through 14 *)
TEMP15 ← ABS(DEST[127:120] − SRC[127:120]);
DEST[15:0] ← SUM(TEMP0:TEMP7);
DEST[63:16] ← 000000000000H;
DEST[79:64] ← SUM(TEMP8:TEMP15);
DEST[127:80] ← 000000000000H;

DEST[VLMAX-1:128] (Unmodified)

**VPSADBW (VEX.128 encoded version)**

TEMP0 ← ABS(SRC1[7:0] − SRC2[7:0]);
(* Repeat operation for bytes 2 through 14 *)
TEMP15 ← ABS(SRC1[127:120] − SRC2[127:120]);
DEST[15:0] ← SUM(TEMP0:TEMP7);
DEST[63:16] ← 000000000000H;
DEST[79:64] ← SUM(TEMP8:TEMP15);
DEST[127:80] ← 0

DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

PSADBW: __m64 _mm_sad_pu8(__m64 a, __m64 b)
PSADBW: __m128i _mm_sad_epu8(__m128i a, __m128i b)

**Flags Affected**

None.

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.L = 1.
PSHUFB — Packed Shuffle Bytes

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 00 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Shuffle bytes in mm1 according to contents of mm2/m64.</td>
</tr>
<tr>
<td>66 0F 38 00 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSSE3</td>
<td>Shuffle bytes in xmm1 according to contents of xmm2/m128.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG 00 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Shuffle bytes in xmm2 according to contents of xmm3/m128.</td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

PSHUFB performs in-place shuffles of bytes in the destination operand (the first operand) according to the shuffle control mask in the source operand (the second operand). The instruction permutes the data in the destination operand, leaving the shuffle mask unaffected. If the most significant bit (bit[7]) of each byte of the shuffle control mask is set, then constant zero is written in the result byte. Each byte in the shuffle control mask forms an index to permute the corresponding byte in the destination operand. The value of each index is the least significant 4 bits (128-bit operation) or 3 bits (64-bit operation) of the shuffle control byte. Both operands can be MMX register or XMM registers. When the source operand is a 128-bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.
INSTRUCTION SET REFERENCE, M-Z

VEX.128 encoded version: The destination operand is the first operand, the first source operand is the second operand, the second source operand is the third operand. Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise the instruction will #UD.

Operation

PSHUFB (with 64 bit operands)

for i = 0 to 7 {
    if (SRC[(i * 8)+7] = 1) then
        DEST[(i*8)+7..(i*8)+0] ← 0;
    else
        index[2..0] ← SRC[(i*8)+2 .. (i*8)+0];
        DEST[(i*8)+7..(i*8)+0] ← DEST[(index*8+7)..(index*8+0)];
    endif;
}

PSHUFB (with 128 bit operands)

for i = 0 to 15 {
    if (SRC[(i * 8)+7] = 1) then
        DEST[(i*8)+7..(i*8)+0] ← 0;
    else
        index[3..0] ← SRC[(i*8)+3 .. (i*8)+0];
        DEST[(i*8)+7..(i*8)+0] ← DEST[(index*8+7)..(index*8+0)];
    endif
}

DEST[VLMAX-1:128] ← 0

VPShufB (VEX.128 encoded version)

for i = 0 to 15 {
    if (SRC2[(i * 8)+7] = 1) then
        DEST[(i*8)+7..(i*8)+0] ← 0;
    else
        index[3..0] ← SRC2[(i*8)+3 .. (i*8)+0];
        DEST[(i*8)+7..(i*8)+0] ← SRC1[(index*8+7)..(index*8+0)];
    endif
}

DEST[VLMAX-1:128] ← 0
PSHUFB — Packed Shuffle Bytes

**Intel C/C++ Compiler Intrinsic Equivalent**

PSHUFB:  __m64 _mm_shuffle_pi8 (__m64 a, __m64 b)
PSHUFB:  __m128i _mm_shuffle_epi8 (__m128i a, __m128i b)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.L = 1.
INSTRUCTION SET REFERENCE, M-Z

**PSHUFD—Shuffle Packed Doublewords**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 70 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shuffle the doublewords in xmm2/m128 based on the encoding in imm8 and store the result in xmm1.</td>
</tr>
<tr>
<td>PSHUFD xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F:W1G 70 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Shuffle the doublewords in xmm2/m128 based on the encoding in imm8 and store the result in xmm1.</td>
</tr>
<tr>
<td>VPShufd xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Copies doublewords from source operand (second operand) and inserts them in the destination operand (first operand) at the locations selected with the order operand (third operand). Figure 4-11 shows the operation of the PSHUFD instruction and the encoding of the order operand. Each 2-bit field in the order operand selects the contents of one doubleword location in the destination operand. For example, bits 0 and 1 of the order operand select the contents of doubleword 0 of the destination operand. The encoding of bits 0 and 1 of the order operand (see the field encoding in Figure 4-11) determines which doubleword from the source operand will be copied to doubleword 0 of the destination operand.

![Figure 4-11. PSHUFD Instruction Operation](image-url)
The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The order operand is an 8-bit immediate. Note that this instruction permits a doubleword in the source operand to be copied to more than one doubleword location in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:1288) of the destination YMM register are zeroed. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.

**Operation**

**PSHUFD (128-bit Legacy SSE version)**

| DEST[31:0] | (SRC >> (ORDER[1:0] * 32))[31:0]; |
| DEST[63:32] | (SRC >> (ORDER[3:2] * 32))[31:0]; |
| DEST[95:64] | (SRC >> (ORDER[5:4] * 32))[31:0]; |
| DEST[127:96] | (SRC >> (ORDER[7:6] * 32))[31:0]; |
| DEST[VLMAX-1:128] (Unmodified) | 0 |

**VPSHUFD (VEX.128 encoded version)**

| DEST[31:0] | (SRC >> (ORDER[1:0] * 32))[31:0]; |
| DEST[63:32] | (SRC >> (ORDER[3:2] * 32))[31:0]; |
| DEST[95:64] | (SRC >> (ORDER[5:4] * 32))[31:0]; |
| DEST[127:96] | (SRC >> (ORDER[7:6] * 32))[31:0]; |
| DEST[VLMAX-1:128] | 0 |

**Intel C/C++ Compiler Intrinsic Equivalent**

PSHUFD: __m128i _mm_shuffle_epi32(__m128i a, int n)

**Flags Affected**

None.

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.L = 1.

If VEX.vvvv != 1111B.
**PSHUFHW—Shuffle Packed High Words**

<table>
<thead>
<tr>
<th>Opcode/_instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 70 /r lb</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shuffle the high words in (xmm2/m128) based on the encoding in (imm8) and store the result in (xmm1).</td>
</tr>
<tr>
<td>PSHUFHW (xmm1, xmm2/ m128, ) (imm8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.F3.0F.WIG 70 /r lb</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Shuffle the high words in (xmm2/m128) based on the encoding in (imm8) and store the result in (xmm1).</td>
</tr>
<tr>
<td>VPSHUFHW (xmm1, xmm2/m128, ) (imm8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Copies words from the high quadword of the source operand (second operand) and inserts them in the high quadword of the destination operand (first operand) at word locations selected with the order operand (third operand). This operation is similar to the operation used by the PSHUFD instruction, which is illustrated in Figure 4-11. For the PSHUFHW instruction, each 2-bit field in the order operand selects the contents of one word location in the high quadword of the destination operand. The binary encodings of the order operand fields select words (0, 1, 2 or 3, 4) from the high quadword of the source operand to be copied to the destination operand. The low quadword of the source operand is copied to the low quadword of the destination operand.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The order operand is an 8-bit immediate. Note that this instruction permits a word in the high quadword of the source operand to be copied to more than one word location in the high quadword of the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAX-1:128) of the destination YMM register are zeroed. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise the instruction will #UD.
Operation

**PSHUFHW (128-bit Legacy SSE version)**

DEST[63:0] ← SRC[63:0]
DEST[79:64] ← (SRC >> (imm[1:0] * 16))[79:64]
DEST[VLMAX-1:128] (Unmodified)

**VPSHUFHW (VEX.128 encoded version)**

DEST[63:0] ← SRC1[63:0]
DEST[79:64] ← (SRC1 >> (imm[1:0] * 16))[79:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent

PSHUFHW: __m128i _mm_shufflehi_epi16(__m128i a, int n)

Flags Affected

None.

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 4; additionally

#UD If VEX.L = 1.
If VEX.vvvv != 1111B.
INSTRUCTION SET REFERENCE, M-Z

PSHUFLW—Shuffle Packed Low Words

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 70 /r lb</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shuffle the low words in xmm2/m128 based on the encoding in imm8 and store the result in xmm1.</td>
</tr>
<tr>
<td>PSHUFLW xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.F2.0F:WIG 70 /r lb</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Shuffle the low words in xmm2/m128 based on the encoding in imm8 and store the result in xmm1.</td>
</tr>
<tr>
<td>VPSHUFLW xmm1, xmm2/m128, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Copies words from the low quadword of the source operand (second operand) and inserts them in the low quadword of the destination operand (first operand) at word locations selected with the order operand (third operand). This operation is similar to the operation used by the PSHUFD instruction, which is illustrated in Figure 4-11. For the PSHUFLW instruction, each 2-bit field in the order operand selects the contents of one word location in the low quadword of the destination operand. The binary encodings of the order operand fields select words (0, 1, 2, or 3) from the low quadword of the source operand to be copied to the destination operand. The high quadword of the source operand is copied to the high quadword of the destination operand.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The order operand is an 8-bit immediate. Note that this instruction permits a word in the low quadword of the source operand to be copied to more than one word location in the low quadword of the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAX-1:128) of the destination YMM register are zeroed. VEX.vvvv is reserved and must be 1111b, VEX.L must be 0, otherwise instructions will #UD.
**Operation**

**PSHUFLW (128-bit Legacy SSE version)**

\[
\begin{align*}
\text{DEST}[15:0] & \leftarrow (\text{SRC} >> (\text{imm}[1:0] * 16))[15:0] \\
\text{DEST}[31:16] & \leftarrow (\text{SRC} >> (\text{imm}[3:2] * 16))[15:0] \\
\text{DEST}[47:32] & \leftarrow (\text{SRC} >> (\text{imm}[5:4] * 16))[15:0] \\
\text{DEST}[63:48] & \leftarrow (\text{SRC} >> (\text{imm}[7:6] * 16))[15:0] \\
\text{DEST}[127:64] & \leftarrow \text{SRC}[127:64] \\
\text{DEST}[\text{VLMAX}-1:128] & \text{(Unmodified)}
\end{align*}
\]

**VPSHUFLW (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[15:0] & \leftarrow (\text{SRC1} >> (\text{imm}[1:0] * 16))[15:0] \\
\text{DEST}[31:16] & \leftarrow (\text{SRC1} >> (\text{imm}[3:2] * 16))[15:0] \\
\text{DEST}[47:32] & \leftarrow (\text{SRC1} >> (\text{imm}[5:4] * 16))[15:0] \\
\text{DEST}[63:48] & \leftarrow (\text{SRC1} >> (\text{imm}[7:6] * 16))[15:0] \\
\text{DEST}[127:64] & \leftarrow \text{SRC}[127:64] \\
\text{DEST}[\text{VLMAX}-1:128] & \leftarrow 0
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

PSHUFLW: `__m128i _mm_shufflelo_epi16(__m128i a, int n)`

**Flags Affected**

None.

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

- #UD If VEX.L = 1.
- If VEX.vvvv != 1111B.
**PSHUFW—Shuffle Packed Words**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 70 /r b</td>
<td>PSHUFW mm1, mm2/m64, imm8</td>
<td>RMI</td>
<td>Valid</td>
<td>Valid</td>
<td>Shuffle the words in mm2/m64 based on the encoding in imm8 and store the result in mm1.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Copies words from the source operand (second operand) and inserts them in the destination operand (first operand) at word locations selected with the order operand (third operand). This operation is similar to the operation used by the PSHUF D instruction, which is illustrated in Figure 4-11. For the PSHUFW instruction, each 2-bit field in the order operand selects the contents of one word location in the destination operand. The encodings of the order operand fields select words from the source operand to be copied to the destination operand.

The source operand can be an MMX technology register or a 64-bit memory location. The destination operand is an MMX technology register. The order operand is an 8-bit immediate. Note that this instruction permits a word in the source operand to be copied to more than one word location in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

\[
\begin{align*}
\text{DEST}[15:0] & \leftarrow (\text{SRC} \gg (\text{ORDER}[1:0] \times 16))[15:0]; \\
\text{DEST}[31:16] & \leftarrow (\text{SRC} \gg (\text{ORDER}[3:2] \times 16))[15:0]; \\
\text{DEST}[47:32] & \leftarrow (\text{SRC} \gg (\text{ORDER}[5:4] \times 16))[15:0]; \\
\text{DEST}[63:48] & \leftarrow (\text{SRC} \gg (\text{ORDER}[7:6] \times 16))[15:0];
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

PSHUFW: __mm64 _mm_shuffle_pi16(__m64 a, int n)

**Flags Affected**

None.
Numeric Exceptions

None.

Other Exceptions

See Table 22-7, "Exception Conditions for SIMD/MMX Instructions with Memory Reference," in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A.
## PSIGNB/PSIGNW/PSIGND — Packed SIGN

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 38 08 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>PSIGNB mm1, mm2/m64</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Negate/zero/preserve packed byte integers in mm1 depending on the corresponding sign in mm2/m64.</td>
<td></td>
</tr>
<tr>
<td>66 0F 38 08 /r</td>
<td>PSIGNB xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Negate/zero/preserve packed byte integers in xmm1 depending on the corresponding sign in xmm2/m128.</td>
<td></td>
</tr>
<tr>
<td>0F 38 09 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>PSIGNW mm1, mm2/m64</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Negate/zero/preserve packed word integers in mm1 depending on the corresponding sign in mm2/m64.</td>
<td></td>
</tr>
<tr>
<td>66 0F 38 09 /r</td>
<td>PSIGNW xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Negate/zero/preserve packed word integers in xmm1 depending on the corresponding sign in xmm2/m128.</td>
<td></td>
</tr>
<tr>
<td>0F 38 0A /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>PSIGND mm1, mm2/m64</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Negate/zero/preserve packed doubleword integers in mm1 depending on the corresponding sign in mm2/m64.</td>
<td></td>
</tr>
<tr>
<td>66 0F 38 0A /r</td>
<td>PSIGND xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSSE3</td>
<td>Negate/zero/preserve packed doubleword integers in xmm1 depending on the corresponding sign in xmm2/m128.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.WIG</td>
<td>VPSIGNB xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Negate/zero/preserve packed byte integers in xmm2 depending on the corresponding sign in xmm3/m128.</td>
<td></td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, M-Z

PSIGNB/PSIGNW/PSIGND — Packed SIGN

**Description**

PSIGNB/PSIGNW/PSIGND negates each data element of the destination operand (the first operand) if the signed integer value of the corresponding data element in the source operand (the second operand) is less than zero. If the signed integer value of a data element in the source operand is positive, the corresponding data element in the destination operand is unchanged. If a data element in the source operand is zero, the corresponding data element in the destination operand is set to zero.

PSIGNB operates on signed bytes. PSIGNW operates on 16-bit signed words. PSIGND operates on signed 32-bit integers. Both operands can be MMX register or XMM registers. When the source operand is a 128bit memory operand, the operand must be aligned on a 16-byte boundary or a general-protection exception (#GP) will be generated.

In 64-bit mode, use the REX prefix to access additional registers.

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

NOTES:
VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise instructions will #UD.

**Operation**

**PSIGNB (with 64 bit operands)**

IF (SRC[7:0] < 0 )  
    DEST[7:0] ← Neg(DEST[7:0])  
ELSEIF (SRC[7:0] = 0 )  
    DEST[7:0] ← 0  
ELSEIF (SRC[7:0] > 0 )  
    DEST[7:0] ← DEST[7:0]  
Repeat operation for 2nd through 7th bytes  

IF (SRC[63:56] < 0 )  
    DEST[63:56] ← Neg(DEST[63:56])  
ELSEIF (SRC[63:56] = 0 )  
    DEST[63:56] ← 0  
ELSEIF (SRC[63:56] > 0 )  
    DEST[63:56] ← DEST[63:56]

**PSIGNB (with 128 bit operands)**

IF (SRC[7:0] < 0 )  
    DEST[7:0] ← Neg(DEST[7:0])  
ELSEIF (SRC[7:0] = 0 )  
    DEST[7:0] ← 0  
ELSEIF (SRC[7:0] > 0 )  
    DEST[7:0] ← DEST[7:0]  
Repeat operation for 2nd through 15th bytes  
IF (SRC[127:120] < 0 )  
    DEST[127:120] ← Neg(DEST[127:120])  
ELSEIF (SRC[127:120] = 0 )  
    DEST[127:120] ← 0  
ELSEIF (SRC[127:120] > 0 )  
    DEST[127:120] ← DEST[127:120]

**PSIGNW (with 64 bit operands)**

IF (SRC[15:0] < 0 )  
    DEST[15:0] ← Neg(DEST[15:0])  
ELSEIF (SRC[15:0] = 0 )  
    DEST[15:0] ← 0  
ELSEIF (SRC[15:0] > 0 )

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DEST[15:0] ← DEST[15:0]
Repeat operation for 2nd through 3rd words
IF (SRC[63:48] < 0 )
    DEST[63:48] ← Neg(DEST[63:48])
ELSEIF (SRC[63:48] = 0 )
    DEST[63:48] ← 0
ELSEIF (SRC[63:48] > 0 )
    DEST[63:48] ← DEST[63:48]

PSIGNW (with 128 bit operands)

IF (SRC[15:0] < 0 )
    DEST[15:0] ← Neg(DEST[15:0])
ELSEIF (SRC[15:0] = 0 )
    DEST[15:0] ← 0
ELSEIF (SRC[15:0] > 0 )
    DEST[15:0] ← DEST[15:0]
Repeat operation for 2nd through 7th words
IF (SRC[127:112] < 0 )
    DEST[127:112] ← Neg(DEST[127:112])
ELSEIF (SRC[127:112] = 0 )
    DEST[127:112] ← 0
ELSEIF (SRC[127:112] > 0 )

PSIGND (with 64 bit operands)

IF (SRC[31:0] < 0 )
    DEST[31:0] ← Neg(DEST[31:0])
ELSEIF (SRC[31:0] = 0 )
    DEST[31:0] ← 0
ELSEIF (SRC[31:0] > 0 )
    DEST[31:0] ← DEST[31:0]
IF (SRC[63:32] < 0 )
    DEST[63:32] ← Neg(DEST[63:32])
ELSEIF (SRC[63:32] = 0 )
    DEST[63:32] ← 0
ELSEIF (SRC[63:32] > 0 )

PSIGND (with 128 bit operands)

IF (SRC[31:0] < 0 )
    DEST[31:0] ← Neg(DEST[31:0])
ELSEIF (SRC[31:0] = 0 )

INSTRUCTION SET REFERENCE, M-Z

```
DEST[31:0] ← 0
ELSEIF (SRC[31:0] > 0 )
    DEST[31:0] ← DEST[31:0]
Repeat operation for 2nd through 3rd double words
IF (SRC[127:96] < 0 )
    DEST[127:96] ← Neg(DEST[127:96])
ELSEIF (SRC[127:96] = 0 )
    DEST[127:96] ← 0
ELSEIF (SRC[127:96] > 0 )
    DEST[127:96] ← DEST[127:96]
```

**VPSIGNB (VEX.128 encoded version)**
DEST[127:0] ← BYTE_SIGN(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**VPSIGNW (VEX.128 encoded version)**
DEST[127:0] ← WORD_SIGN(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**VPSIGND (VEX.128 encoded version)**
DEST[127:0] ← DWORD_SIGN(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**
PSIGNB:  __m64 _mm_sign_pi8 (__m64 a, __m64 b)
PSIGNB:  __m128i _mm_sign_epi8 (__m128i a, __m128i b)
PSIGNW:  __m64 _mm_sign_pi16 (__m64 a, __m64 b)
PSIGNW:  __m128i _mm_sign_epi16 (__m128i a, __m128i b)
PSIGND:  __m64 _mm_sign_pi32 (__m64 a, __m64 b)
PSIGND:  __m128i _mm_sign_epi32 (__m128i a, __m128i b)

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 4; additionally
#UD If VEX.L = 1.

Intel C/C++ Compiler Intrinsic Equivalent
PSIGNB:  __m64 _mm_sign_pi8 (__m64 a, __m64 b)
PSIGNB:  __m128i _mm_sign_epi8 (__m128i a, __m128i b)
PSIGNW:  __m64 _mm_sign_pi16 (__m64 a, __m64 b)
PSIGNW:  __m128i _mm_sign_epi16 (__m128i a, __m128i b)
PSIGND:  __m64 _mm_sign_pi32 (__m64 a, __m64 b)
PSIGND:  __m128i _mm_sign_epi32 (__m128i a, __m128i b)

**Other Exceptions**
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
**PSLLDQ—Shift Double Quadword Left Logical**

**Opcode/Instruction**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 73 /7 ib PSLLDQ xmm1, imm8</td>
<td>MI V/V</td>
<td>SSE2</td>
<td>Shift xmm1 left by imm8 bytes while shifting in 0s.</td>
<td></td>
</tr>
<tr>
<td>VEX.ND.128.66.0F:WIG 73 /7 ib VPSLLDQ xmm1, xmm2, imm8</td>
<td>VMI V/V</td>
<td>AVX</td>
<td>Shift xmm2 left by imm8 bytes while shifting in 0s and store result in xmm1.</td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MI ModRM:r/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>VMI VEX.vvvv (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

**Description**

Shifts the destination operand (first operand) to the left by the number of bytes specified in the count operand (second operand). The empty low-order bytes are cleared (set to all 0s). If the value specified by the count operand is greater than 15, the destination operand is set to all 0s. The destination operand is an XMM register. The count operand is an 8-bit immediate.

128-bit Legacy SSE version: The source and destination operands are the same. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.vvvv encodes the destination register, and VEX.B + ModRM.r/m encodes the source register. VEX.L must be 0, otherwise instructions will #UD.

**Operation**

**PSLLDQ (128-bit Legacy SSE version)**

```plaintext
TEMP ← COUNT
IF (TEMP > 15) THEN TEMP ← 16; FI
DEST ← DEST << (TEMP * 8)
DEST[VLMAX-1:128] (Unmodified)
```

**VPSLLDQ (VEX.128 encoded version)**

```plaintext
TEMP ← COUNT
IF (TEMP > 15) THEN TEMP ← 16; FI
DEST ← SRC << (TEMP * 8)
DEST[VLMAX-1:128] ← 0
```
**INSTRUCTION SET REFERENCE, M-Z**

**Intel C/C++ Compiler Intrinsic Equivalent**

PSLLDQ:  
\[ \text{__m128i } \_\text{mm}_\text{slli}_\text{si128} (\_\text{m128i } a, \text{int} \text{imm}) \]

**Flags Affected**

None.

**Numeric Exceptions**

None.

**Other Exceptions**

See Exceptions Type 7; additionally

#UD  
If VEX.L = 1.
### PSLLW/PSLLD/PSLLQ—Shift Packed Data Left Logical

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode</th>
<th>CPUID Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F F1 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift words in ( mm ) left ( mm/m64 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLW mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F F1 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift words in ( xmm1 ) left by ( xmm2/m128 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 71 /6 ib</td>
<td>MI</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift words in ( mm ) left by ( imm8 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLW xmm1, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 71 /6 ib</td>
<td>MI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift words in ( xmm1 ) left by ( imm8 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLW xmm1, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F F2 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift doublewords in ( mm ) left by ( mm/m64 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLD mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F F2 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift doublewords in ( xmm1 ) left by ( xmm2/m128 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 72 /6 ib</td>
<td>MI</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift doublewords in ( mm ) left by ( imm8 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLD mm, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 72 /6 ib</td>
<td>MI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift doublewords in ( xmm1 ) left by ( imm8 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLD xmm1, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F F3 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift quadword in ( mm ) left by ( mm/m64 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLQ mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F F3 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift quadwords in ( xmm1 ) left by ( xmm2/m128 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLQ xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 73 /6 ib</td>
<td>MI</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift quadword in ( mm ) left by ( imm8 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLQ mm, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 73 /6 ib</td>
<td>MI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift quadwords in ( xmm1 ) left by ( imm8 ) while shifting in 0s.</td>
</tr>
<tr>
<td>PSLLQ xmm1, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Instruction Set Reference, M-Z

#### InstructionOperand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM:r/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
<tr>
<td>VMI</td>
<td>VEX.vvvv (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Shifts the bits in the individual data elements (words, doublewords, or quadword) in the destination operand (first operand) to the left by the number of bits specified in the count operand (second operand). As the bits in the data elements are shifted left,
the empty low-order bits are cleared (set to 0). If the value specified by the count operand is greater than 15 (for words), 31 (for doublewords), or 63 (for a quad-word), then the destination operand is set to all 0s. Figure 4-12 gives an example of shifting words in a 64-bit operand.

The destination operand may be an MMX technology register or an XMM register; the count operand can be either an MMX technology register or an 64-bit memory location, an XMM register or a 128-bit memory location, or an 8-bit immediate. Note that only the first 64-bits of a 128-bit count operand are checked to compute the count.

![Figure 4-12. PSLLW, PSLLD, and PSLLQ Instruction Operation Using 64-bit Operand](image)

The PSLLW instruction shifts each of the words in the destination operand to the left by the number of bits specified in the count operand; the PSLLD instruction shifts each of the doublewords in the destination operand; and the PSLLQ instruction shifts the quadword (or quadwords) in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged. If the count operand is a memory address, 128 bits are loaded but the upper 64 bits are ignored.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. For shifts with an immediate count (VEX.128.66.0F 71-73 /6), VEX.vvvv encodes the destination register, and VEX.B + ModRM.r/m encodes the source register. VEX.L must be 0, otherwise instructions will #UD. If the count operand is a memory address, 128 bits are loaded but the upper 64 bits are ignored.

**Operation**

**PSLLW (with 64-bit operand)**

IF (COUNT > 15)
THEN
DEST[64:0] ← 0000000000000000H;
ELSE
DEST[15:0] ← ZeroExtend(DEST[15:0] << COUNT);
/* Repeat shift operation for 2nd and 3rd words */
DEST[63:48] ← ZeroExtend(DEST[63:48] << COUNT);
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Fl;

PSLLD (with 64-bit operand)
IF (COUNT > 31)
THEN
   DEST[64:0] ← 0000000000000000H;
ELSE
   DEST[31:0] ← ZeroExtend(DEST[31:0] << COUNT);
   DEST[63:32] ← ZeroExtend(DEST[63:32] << COUNT);
FI;

PSLLQ (with 64-bit operand)
IF (COUNT > 63)
THEN
   DEST[64:0] ← 0000000000000000H;
ELSE
   DEST ← ZeroExtend(DEST << COUNT);
FI;

PSLLW (with 128-bit operand)
COUNT ← COUNT_SOURCE[63:0];
IF (COUNT > 15)
THEN
   DEST[128:0] ← 00000000000000000000000000000000H;
ELSE
   DEST[15:0] ← ZeroExtend(DEST[15:0] << COUNT);
   (* Repeat shift operation for 2nd through 7th words *)
   DEST[127:112] ← ZeroExtend(DEST[127:112] << COUNT);
FI;

PSLLD (with 128-bit operand)
COUNT ← COUNT_SOURCE[63:0];
IF (COUNT > 31)
THEN
   DEST[128:0] ← 00000000000000000000000000000000H;
ELSE
   DEST[31:0] ← ZeroExtend(DEST[31:0] << COUNT);
   (* Repeat shift operation for 2nd and 3rd doublewords *)
   DEST[127:96] ← ZeroExtend(DEST[127:96] << COUNT);
FI;

PSLLQ (with 128-bit operand)
COUNT ← COUNT_SOURCE[63:0];
IF (COUNT > 63)
THEN
INSTRUCTION SET REFERENCE, M-Z

PSLLW (xmm, xmm, xmm/m128)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_WORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

PSLLW (xmm, imm8)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_WORDS(DEST, imm8)
DEST[VLMAX-1:128] ← 0

VPSLLLD (xmm, xmm, xmm/m128)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_DWORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

VPSLLLD (xmm, imm8)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_DWORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

PSLLD (xmm, xmm, xmm/m128)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_DWORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

PSLLD (xmm, imm8)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_DWORDS(DEST, imm8)
DEST[VLMAX-1:128] ← 0

VPSLLLQ (xmm, xmm, xmm/m128)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_QWORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

VPSLLLQ (xmm, imm8)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_QWORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

PSLLQ (xmm, xmm, xmm/m128)
DEST[127:0] ← LOGICAL_LEFT_SHIFT_QWORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

PSLLQ (xmm, imm8)
INSTRUCTION SET REFERENCE, M-Z

DEST[127:0] ← LOGICAL_LEFT_SHIFT_QWORDS(DEST, imm8)
DEST[VLMAX-1:128] (Unmodified)

**VPSLLW (xmm, xmm, xmm/m128)**
DEST[127:0] ← LOGICAL_LEFT_SHIFT_WORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**VPSLLW (xmm, imm8)**
DEST[127:0] ← LOGICAL_LEFT_SHIFT_WORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

**PSLLW (xmm, xmm, xmm/m128)**
DEST[127:0] ← LOGICAL_LEFT_SHIFT_WORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

**PSLLW (xmm, imm8)**
DEST[127:0] ← LOGICAL_LEFT_SHIFT_WORDS(DEST, imm8)
DEST[VLMAX-1:128] (Unmodified)

**VPSLLD (xmm, xmm, xmm/m128)**
DEST[127:0] ← LOGICAL_LEFT_SHIFT_DWORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**VPSLLD (xmm, imm8)**
DEST[127:0] ← LOGICAL_LEFT_SHIFT_DWORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalents**

PSLLW: __m64 _mm_slli_pi16 (__m64 m, int count)
PSLLW: __m64 _mm_sll_pi16 (__m64 m, __m64 count)
PSLLW: __m128i _mm_slli_pi16 (__m64 m, int count)
PSLLW: __m128i _mm_sll_pi16 (__m64 m, __m128i count)
PSLLD: __m64 _mm_slli_epi32 (__m64 m, int count)
PSLLD: __m64 _mm_sll_epi32 (__m64 m, __m64 count)
PSLLD: __m128i _mm_slli_epi32 (__m128i m, int count)
PSLLD: __m128i _mm_sll_epi32 (__m128i m, __m128i count)
PSLLQ: __m64 _mm_slli_si64 (__m64 m, int count)
PSLLQ: __m64 _mm_sll_si64 (__m64 m, __m64 count)
PSLLQ: __m128i _mm_slli_epi64 (__m128i m, int count)
PSLLQ: __m128i _mm_sll_epi64 (__m128i m, __m128i count)
Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4 and 7 for non-VEX-encoded instructions.

#UD If VEX.L = 1.
### PSRAW/PSRAD—Shift Packed Data Right Arithmetic

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PSRAW mm, mm/m64</strong></td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift words in <em>mm</em> right by <em>mm/m64</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>PSRAW xmm1, xmm2/m128</strong></td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift words in <em>xmm1</em> right by <em>xmm2/m128</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>PSRAW mm, imm8</strong></td>
<td>MI</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift words in <em>mm</em> right by <em>imm8</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>PSRAW xmm1, imm8</strong></td>
<td>MI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift words in <em>xmm1</em> right by <em>imm8</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>PSRAD mm, mm/m64</strong></td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift doublewords in <em>mm</em> right by <em>mm/m64</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>PSRAD xmm1, xmm2/m128</strong></td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift doubleword in <em>xmm1</em> right by <em>xmm2/m128</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>PSRAD mm, imm8</strong></td>
<td>MI</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift doublewords in <em>mm</em> right by <em>imm8</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>PSRAD xmm1, imm8</strong></td>
<td>MI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift doublewords in <em>xmm1</em> right by <em>imm8</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>VPSRAW xmm1, xmm2, xmm3/m128</strong></td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Shift words in <em>xmm2</em> right by amount specified in <em>xmm3/m128</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>VPSRAW xmm1, xmm2, imm8</strong></td>
<td>VMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Shift words in <em>xmm2</em> right by <em>imm8</em> while shifting in sign bits.</td>
</tr>
<tr>
<td><strong>VPSRAD xmm1, xmm2, xmm3/m128</strong></td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Shift doublewords in <em>xmm2</em> right by amount specified in <em>xmm3/m128</em> while shifting in sign bits.</td>
</tr>
</tbody>
</table>
**INSTRUCTION SET REFERENCE, M-Z**

**PSRAW/PSRAD—Shift Packed Data Right Arithmetic**

**INSTRUCTION OPERAND ENCODING**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRMreg (r)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
<tr>
<td>VMI</td>
<td>VEX.vvvv (w)</td>
<td>ModRMreg (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Shifts the bits in the individual data elements (words or doublewords) in the destination operand (first operand) to the right by the number of bits specified in the count operand (second operand). As the bits in the data elements are shifted right, the empty high-order bits are filled with the initial value of the sign bit of the data element. If the value specified by the count operand is greater than 15 (for words) or 31 (for doublewords), each destination data element is filled with the initial value of the sign bit of the element. (Figure 4-13 gives an example of shifting words in a 64-bit operand.)

**Figure 4-13. PSRAW and PSRAD Instruction Operation Using a 64-bit Operand**

**NOTES:**

The destination operand may be an MMX technology register or an XMM register; the count operand can be either an MMX technology register or an 64-bit memory location, an XMM register or a 128-bit memory location, or an 8-bit immediate. Note that only the first 64-bits of a 128-bit count operand are checked to compute the count.

The PSRAW instruction shifts each of the words in the destination operand to the right by the number of bits specified in the count operand, and the PSRAD instruction shifts each of the doublewords in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged. If the count operand is a memory address, 128 bits are loaded but the upper 64 bits are ignored.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. For shifts with an immediate count (VEX.128.66.0F 71-73 /4), VEX.vvvv encodes the destination register, and VEX.B + ModRM.r/m encodes the source register. VEX.L must be 0, otherwise instructions will #UD. Bits (255:128) of the corresponding YMM destination register remain unchanged. If the count operand is a memory address, 128 bits are loaded but the upper 64 bits are ignored.

**Operation**

**PSRAW (with 64-bit operand)**

IF (COUNT > 15)
    THEN COUNT ← 16;
FL;
DEST[15:0] ← SignExtend(DEST[15:0] >> COUNT);
(* Repeat shift operation for 2nd and 3rd words *)
DEST[63:48] ← SignExtend(DEST[63:48] >> COUNT);

**PSRAD (with 64-bit operand)**

IF (COUNT > 31)
    THEN COUNT ← 32;
FL;
DEST[31:0] ← SignExtend(DEST[31:0] >> COUNT);
DEST[63:32] ← SignExtend(DEST[63:32] >> COUNT);

**PSRAW (with 128-bit operand)**

COUNT ← COUNT_SOURCE[63:0];
IF (COUNT > 15)
    THEN COUNT ← 16;
FL;
DEST[15:0] ← SignExtend(DEST[15:0] >> COUNT);
INSTRUCTION SET REFERENCE, M-Z

PSRAW/PSRAD—Shift Packed Data Right Arithmetic

(* Repeat shift operation for 2nd through 7th words *)
DEST[127:112] ← SignExtend(DEST[127:112] >> COUNT);

**PSRAD (with 128-bit operand)**
COUNT ← COUNT_SOURCE[63:0];
IF (COUNT > 31)
    THEN COUNT ← 32;
FI;
DEST[31:0] ← SignExtend(DEST[31:0] >> COUNT);
(* Repeat shift operation for 2nd and 3rd doublewords *)
DEST[127:96] ← SignExtend(DEST[127:96] >> COUNT);

**PSRAW (xmm, xmm, xmm/m128)**
DEST[127:0] ← ARITHMETIC_RIGHT_SHIFT_WORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

**PSRAW (xmm, imm8)**
DEST[127:0] ← ARITHMETIC_RIGHT_SHIFT_WORDS(DEST, imm8)
DEST[VLMAX-1:128] (Unmodified)

**VPSRAW (xmm, xmm, xmm/m128)**
DEST[127:0] ← ARITHMETIC_RIGHT_SHIFT_WORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**VPSRAW (xmm, imm8)**
DEST[127:0] ← ARITHMETIC_RIGHT_SHIFT_WORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

**PSRAD (xmm, xmm, xmm/m128)**
DEST[127:0] ← ARITHMETIC_RIGHT_SHIFT_DWORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

**PSRAD (xmm, imm8)**
DEST[127:0] ← ARITHMETIC_RIGHT_SHIFT_DWORDS(DEST, imm8)
DEST[VLMAX-1:128] (Unmodified)

**VPSRAD (xmm, xmm, xmm/m128)**
DEST[127:0] ← ARITHMETIC_RIGHT_SHIFT_DWORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**VPSRAD (xmm, imm8)**
DEST[127:0] ← ARITHMETIC_RIGHT_SHIFT_DWORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

PSRAW/PSRAD—Shift Packed Data Right Arithmetic
Intel C/C++ Compiler Intrinsic Equivalents

PSRAW: __m64 _mm_srai_pi16 (__m64 m, int count)
PSRAW: __m64 _mm_sra_pi16 (__m64 m, __m64 count)
PSRAD: __m64 _mm_srai_pi32 (__m64 m, int count)
PSRAD: __m64 _mm_sra_pi32 (__m64 m, __m64 count)
PSRAW: __m128i _mm_srai_epi16 (__m128i m, int count)
PSRAW: __m128i _mm_sra_epi16 (__m128i m, __m128i count)
PSRAD: __m128i _mm_srai_epi32 (__m128i m, int count)
PSRAD: __m128i _mm_sra_epi32 (__m128i m, __m128i count)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4 and 7 for non-VEX-encoded instructions.

#UD                  If VEX.L = 1.
PSRLDQ—Shift Double Quadword Right Logical

Description
Shifts the destination operand (first operand) to the right by the number of bytes specified in the count operand (second operand). The empty high-order bytes are cleared (set to all 0s). If the value specified by the count operand is greater than 15, the destination operand is set to all 0s. The destination operand is an XMM register. The count operand is an 8-bit immediate.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The source and destination operands are the same. Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.vvv encodes the destination register, and VEX.B + ModRM.r/m encodes the source register. VEX.L must be 0, otherwise instructions will #UD.

Operation

PSRLDQ (128-bit Legacy SSE version)

TEMP ← COUNT
IF (TEMP > 15) THEN TEMP ← 16; FI
DEST ← DEST >> (TEMP * 8)
DEST[VLMAX-1:128] (Unmodified)

VPSRLDQ (VEX.128 encoded version)

TEMP ← COUNT
IF (TEMP > 15) THEN TEMP ← 16; FI
DEST ← SRC >> (TEMP * 8)
INSTRUCTION SET REFERENCE, M-Z

DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PSRLDQ: __m128i _mm_srli_si128 ( __m128i a, int imm)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 7; additionally
#UD If VEX.L = 1.
### PSRLW/PSRLD/PSRLQ—Shift Packed Data Right Logical

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF D1 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift words in mm right by amount specified in mm/m64 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLW mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF D1 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift words in xmm1 right by amount specified in xmm2/m128 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF 71 /2 ib</td>
<td>MI</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift words in mm right by imm8 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLW mm, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF 71 /2 ib</td>
<td>MI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift words in xmm1 right by imm8 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLW xmm1, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF D2 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift doublewords in mm right by amount specified in mm/m64 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLD mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF D2 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift doublewords in xmm1 right by amount specified in xmm2/m128 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF 72 /2 ib</td>
<td>MI</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift doublewords in mm right by imm8 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLD mm, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF 72 /2 ib</td>
<td>MI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift doublewords in xmm1 right by imm8 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLD xmm1, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF D3 /r</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift mm right by amount specified in mm/m64 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLQ mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 OF D3 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift quadwords in xmm1 right by amount specified in xmm2/m128 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLQ xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OF 73 /2 ib</td>
<td>MI</td>
<td>V/V</td>
<td>MMX</td>
<td>Shift mm right by imm8 while shifting in 0s.</td>
</tr>
<tr>
<td>PSRLQ mm, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**INSTRUCTION SET REFERENCE, M-Z**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 73 /2 ib</td>
<td>MI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shift quadwords in xmm1 right by imm8 while shifting in Os.</td>
</tr>
<tr>
<td>PSRLQ xmm1, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG D1 /r</td>
<td>VVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Shift words in xmm2 right by amount specified in xmm3/m128 while shifting in Os.</td>
</tr>
<tr>
<td>VPSRLW xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG D2 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Shift doublewords in xmm2 right by amount specified in xmm3/m128 while shifting in Os.</td>
</tr>
<tr>
<td>VPSRLD xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG D3 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Shift quadwords in xmm2 right by amount specified in xmm3/m128 while shifting in Os.</td>
</tr>
<tr>
<td>VPSRLQ xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**NOTES:**

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:r/m (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM:r/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:r/m (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
<tr>
<td>VMI</td>
<td>VEX.vvvv (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, M-Z

Description
Shifts the bits in the individual data elements (words, doublewords, or quadword) in the destination operand (first operand) to the right by the number of bits specified in the count operand (second operand). As the bits in the data elements are shifted right, the empty high-order bits are cleared (set to 0). If the value specified by the count operand is greater than 15 (for words), 31 (for doublewords), or 63 (for a quadword), then the destination operand is set to all 0s. Figure 4-14 gives an example of shifting words in a 64-bit operand.

The destination operand may be an MMX technology register or an XMM register; the count operand can be either an MMX technology register or an 64-bit memory location, an XMM register or a 128-bit memory location, or an 8-bit immediate. Note that only the first 64-bits of a 128-bit count operand are checked to compute the count.

The PSRLW instruction shifts each of the words in the destination operand to the right by the number of bits specified in the count operand; the PSRLD instruction shifts each of the doublewords in the destination operand; and the PSRLQ instruction shifts the quadword (or quadwords) in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged. If the count operand is a memory address, 128 bits are loaded but the upper 64 bits are ignored.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. For shifts with an immediate count (VEX.128.66.0F 71-73 /2), VEX.vvvv encodes the destination register, and VEX.B + ModRM.r/m encodes the source register. VEX.L must be 0, otherwise instructions will #UD. If the count operand is a memory address, 128 bits are loaded but the upper 64 bits are ignored.

Operation

PSRLW (with 64-bit operand)
   IF (COUNT > 15)
      THEN

Figure 4-14. PSRLW, PSRLD, and PSRLQ Instruction Operation Using 64-bit Operand

The PSRLW instruction shifts each of the words in the destination operand to the right by the number of bits specified in the count operand; the PSRLD instruction shifts each of the doublewords in the destination operand; and the PSRLQ instruction shifts the quadword (or quadwords) in the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged. If the count operand is a memory address, 128 bits are loaded but the upper 64 bits are ignored.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. For shifts with an immediate count (VEX.128.66.0F 71-73 /2), VEX.vvvv encodes the destination register, and VEX.B + ModRM.r/m encodes the source register. VEX.L must be 0, otherwise instructions will #UD. If the count operand is a memory address, 128 bits are loaded but the upper 64 bits are ignored.

Operation

PSRLW (with 64-bit operand)
   IF (COUNT > 15)
      THEN


INSTRUCTION SET REFERENCE, M-Z

DEST[64:0] ← 0000000000000000H
ELSE
   DEST[15:0] ← ZeroExtend(Dest[15:0] >> COUNT);
   (* Repeat shift operation for 2nd and 3rd words *)
   DEST[63:48] ← ZeroExtend(Dest[63:48] >> COUNT);
Fi;

PSRLD (with 64-bit operand)
IF (COUNT > 31)
THEN
   DEST[64:0] ← 0000000000000000H
ELSE
   DEST[31:0] ← ZeroExtend(Dest[31:0] >> COUNT);
   DEST[63:32] ← ZeroExtend(Dest[63:32] >> COUNT);
Fi;

PSRLQ (with 64-bit operand)
IF (COUNT > 63)
THEN
   DEST[64:0] ← 0000000000000000H
ELSE
   DEST ← ZeroExtend(Dest >> COUNT);
Fi;

PSRLW (with 128-bit operand)
COUNT ← COUNT_SOURCE[63:0];
IF (COUNT > 15)
THEN
   DEST[128:0] ← 00000000000000000000000000000000H
ELSE
   DEST[15:0] ← ZeroExtend(Dest[15:0] >> COUNT);
   (* Repeat shift operation for 2nd through 7th words *)
   DEST[127:112] ← ZeroExtend(Dest[127:112] >> COUNT);
Fi;

PSRLD (with 128-bit operand)
COUNT ← COUNT_SOURCE[63:0];
IF (COUNT > 31)
THEN
   DEST[128:0] ← 00000000000000000000000000000000H
ELSE
   DEST[31:0] ← ZeroExtend(Dest[31:0] >> COUNT);
   (* Repeat shift operation for 2nd and 3rd doublewords *)
   DEST[127:96] ← ZeroExtend(Dest[127:96] >> COUNT);
Fi;
**PSRLQ (with 128-bit operand)**

COUNT ← COUNT_SOURCE[63:0];
IF (COUNT > 15)
THEN
   DEST[128:0] ← 00000000000000000000000000000000H
ELSE
   DEST[63:0] ← ZeroExtend(DEST[63:0] >> COUNT);
   DEST[127:64] ← ZeroExtend(DEST[127:64] >> COUNT);
FI;

**PSRLW (xmm, xmm, xmm/m128)**
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_WORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

**PSRLW (xmm, imm8)**
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_WORDS(DEST, imm8)
DEST[VLMAX-1:128] (Unmodified)

**VPSRLW (xmm, xmm, xmm/m128)**
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_WORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**VPSRLW (xmm, imm8)**
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_WORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

**PSRLD (xmm, xmm, xmm/m128)**
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_DWORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

**PSRLD (xmm, imm8)**
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_DWORDS(DEST, imm8)
DEST[VLMAX-1:128] (Unmodified)

**VPSRLD (xmm, xmm, xmm/m128)**
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_DWORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

**VPSRLD (xmm, imm8)**
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_DWORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

**PSRLQ (xmm, xmm, xmm/m128)**
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DEST[127:0] ← LOGICAL_RIGHT_SHIFT_QWORDS(DEST, SRC)
DEST[VLMAX-1:128] (Unmodified)

PSRLQ (xmm, imm8)
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_QWORDS(DEST, imm8)
DEST[VLMAX-1:128] (Unmodified)

VPSRLQ (xmm, xmm, xmm/m128)
DEST[127:0] ← LOGICAL_RIGHT_SHIFT_QWORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

VPSRLQ (xmm, imm8)
DEST[127:0] ← LOGICAL_RIGHTSHIFT_QWORDS(SRC1, imm8)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents

PSRLW: __m64 _mm_srli_pi16(__m64 m, int count)
PSRLW: __m64 _mm_srl_pi16 (__m64 m, __m64 count)
PSRLW: __m128i _mm_srli_epi16 (__m128i m, int count)
PSRLW: __m128i _mm_srl_epi16 (__m128i m, __m128i count)
PSRLD: __m64 _mm_srli_pi32 (__m64 m, int count)
PSRLD: __m128i _mm_srli_epi32 (__m128i m, int count)
PSRLD: __m128i _mm_srl_epi32 (__m128i m, __m128i count)
PSRLQ: __m64 _mm_srli_si64 (__m64 m, int count)
PSRLQ: __m64 _mm_srl_si64 (__m64 m, __m64 count)
PSRLQ: __m128i _mm_srli_epi64 (__m128i m, int count)
PSRLQ: __m128i _mm_srl_epi64 (__m128i m, __m128i count)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4 and 7 for non-VEX-encoded instructions.

#UD If VEX.L = 1.
### PSUBB/PSUBW/PSUBD—Subtract Packed Integers

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 88 /r^1</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Subtract packed byte integers in <code>mm/m64</code> from packed byte integers in <code>mm</code>.</td>
</tr>
<tr>
<td>PSUBB <code>mm, mm/m64</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 88 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract packed byte integers in <code>xmm2/m128</code> from packed byte integers in <code>xmm1</code>.</td>
</tr>
<tr>
<td>PSUBB <code>xmm1, xmm2/m128</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 89 /r^1</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Subtract packed word integers in <code>mm/m64</code> from packed word integers in <code>mm</code>.</td>
</tr>
<tr>
<td>PSUBW <code>mm, mm/m64</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 89 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract packed word integers in <code>xmm2/m128</code> from packed word integers in <code>xmm1</code>.</td>
</tr>
<tr>
<td>PSUBW <code>xmm1, xmm2/m128</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F FA /r^1</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Subtract packed doubleword integers in <code>mm/m64</code> from packed doubleword integers in <code>mm</code>.</td>
</tr>
<tr>
<td>PSUBD <code>mm, mm/m64</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F FA /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract packed doubleword integers in <code>xmm2/mem128</code> from packed doubleword integers in <code>xmm1</code>.</td>
</tr>
<tr>
<td>PSUBD <code>xmm1, xmm2/m128</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### VEX.NDS.128.66.0F.WIG

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Op/En</th>
<th>Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VPSUBB <code>xmm1, xmm2, xmm3/m128</code></td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed byte integers in <code>xmm3/m128</code> from <code>xmm2</code>.</td>
</tr>
<tr>
<td>VPSUBB <code>xmm1, xmm2, xmm3/m128</code></td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtracted packed word integers in <code>xmm3/m128</code> from <code>xmm2</code>.</td>
</tr>
<tr>
<td>VPSUBD <code>xmm1, xmm2, xmm3/m128</code></td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtracted packed doubleword integers in <code>xmm3/m128</code> from <code>xmm2</code>.</td>
</tr>
</tbody>
</table>

**NOTES:**

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**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:r/m (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD subtract of the packed integers of the source operand (second operand) from the packed integers of the destination operand (first operand), and stores the packed integer results in the destination operand. See Figure 9-4 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an illustration of a SIMD operation. Overflow is handled with wraparound, as described in the following paragraphs.

These instructions can operate on either 64-bit or 128-bit operands. When operating on 64-bit operands, the destination operand must be an MMX technology register and the source operand can be either an MMX technology register or a 64-bit memory location. When operating on 128-bit operands, the destination operand must be an XMM register and the source operand can be either an XMM register or a 128-bit memory location.

The PSUBB instruction subtracts packed byte integers. When an individual result is too large or too small to be represented in a byte, the result is wrapped around and the low 8 bits are written to the destination element.

The PSUBW instruction subtracts packed word integers. When an individual result is too large or too small to be represented in a word, the result is wrapped around and the low 16 bits are written to the destination element.

The PSUBD instruction subtracts packed doubleword integers. When an individual result is too large or too small to be represented in a doubleword, the result is wrapped around and the low 32 bits are written to the destination element.

Note that the PSUBB, PSUBW, and PSUBD instructions can operate on either unsigned or signed (two’s complement notation) packed integers; however, it does not set bits in the EFLAGS register to indicate overflow and/or a carry. To prevent undetected overflow conditions, software must control the ranges of values upon which it operates.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise instructions will #UD.
Operation

**PSUBB (with 64-bit operands)**

\[ \text{DEST}[7:0] \leftarrow \text{DEST}[7:0] - \text{SRC}[7:0]; \]
(* Repeat subtract operation for 2nd through 7th byte *)

\[ \text{DEST}[63:56] \leftarrow \text{DEST}[63:56] - \text{SRC}[63:56]; \]

**PSUBB (with 128-bit operands)**

\[ \text{DEST}[7:0] \leftarrow \text{DEST}[7:0] - \text{SRC}[7:0]; \]
(* Repeat subtract operation for 2nd through 14th byte *)

\[ \text{DEST}[127:120] \leftarrow \text{DEST}[111:120] - \text{SRC}[127:120]; \]

**PSUBW (with 64-bit operands)**

\[ \text{DEST}[15:0] \leftarrow \text{DEST}[15:0] - \text{SRC}[15:0]; \]
(* Repeat subtract operation for 2nd and 3rd word *)

\[ \text{DEST}[63:48] \leftarrow \text{DEST}[63:48] - \text{SRC}[63:48]; \]

**PSUBW (with 128-bit operands)**

\[ \text{DEST}[15:0] \leftarrow \text{DEST}[15:0] - \text{SRC}[15:0]; \]
(* Repeat subtract operation for 2nd through 7th word *)

\[ \text{DEST}[127:112] \leftarrow \text{DEST}[111:120] - \text{SRC}[127:120]; \]

**PSUBD (with 64-bit operands)**

\[ \text{DEST}[31:0] \leftarrow \text{DEST}[31:0] - \text{SRC}[31:0]; \]
\[ \text{DEST}[63:32] \leftarrow \text{DEST}[63:32] - \text{SRC}[63:32]; \]

**PSUBD (with 128-bit operands)**

\[ \text{DEST}[31:0] \leftarrow \text{DEST}[31:0] - \text{SRC}[31:0]; \]
(* Repeat subtract operation for 2nd and 3rd doubleword *)

\[ \text{DEST}[127:96] \leftarrow \text{DEST}[127:96] - \text{SRC}[127:96]; \]

**VPSUBB (VEX.128 encoded version)**

\[ \text{DEST}[7:0] \leftarrow \text{SRC1}[7:0]-\text{SRC2}[7:0] \]
\[ \text{DEST}[15:8] \leftarrow \text{SRC1}[15:8]-\text{SRC2}[15:8] \]
\[ \text{DEST}[23:16] \leftarrow \text{SRC1}[23:16]-\text{SRC2}[23:16] \]
\[ \text{DEST}[31:24] \leftarrow \text{SRC1}[31:24]-\text{SRC2}[31:24] \]
\[ \text{DEST}[39:32] \leftarrow \text{SRC1}[39:32]-\text{SRC2}[39:32] \]
\[ \text{DEST}[47:40] \leftarrow \text{SRC1}[47:40]-\text{SRC2}[47:40] \]
\[ \text{DEST}[55:48] \leftarrow \text{SRC1}[55:48]-\text{SRC2}[55:48] \]
\[ \text{DEST}[63:56] \leftarrow \text{SRC1}[63:56]-\text{SRC2}[63:56] \]
\[ \text{DEST}[71:64] \leftarrow \text{SRC1}[71:64]-\text{SRC2}[71:64] \]
\[ \text{DEST}[79:72] \leftarrow \text{SRC1}[79:72]-\text{SRC2}[79:72] \]
\[ \text{DEST}[87:80] \leftarrow \text{SRC1}[87:80]-\text{SRC2}[87:80] \]
\[ \text{DEST}[95:88] \leftarrow \text{SRC1}[95:88]-\text{SRC2}[95:88] \]
\[ \text{DEST}[103:96] \leftarrow \text{SRC1}[103:96]-\text{SRC2}[103:96] \]
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DEST[111:104] ← SRC[111:104]-SRC2[111:104]
DEST[127:120] ← SRC[127:120]-SRC2[127:120]
DEST[VLMAX-1:128] ← 00

VPSUBW (VEX.128 encoded version)
DEST[15:0] ← SRC[15:0]-SRC2[15:0]
DEST[31:16] ← SRC[31:16]-SRC2[31:16]
DEST[79:64] ← SRC[79:64]-SRC2[79:64]
DEST[95:80] ← SRC[95:80]-SRC2[95:80]
DEST[111:96] ← SRC[111:96]-SRC2[111:96]
DEST[VLMAX-1:128] ← 0

VPSUBD (VEX.128 encoded version)
DEST[31:0] ← SRC[31:0]-SRC2[31:0]
DEST[95:64] ← SRC[95:64]-SRC2[95:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PSUBB: __m64 _mm_sub_pi8(__m64 m1, __m64 m2)
PSUBW: __m64 _mm_sub_pi16(__m64 m1, __m64 m2)
PSUBD: __m64 _mm_sub_pi32(__m64 m1, __m64 m2)
PSUBB: __m128i _mm_sub_epi8 (__m128i a, __m128i b)
PSUBW: __m128i _mm_sub_epi16 (__m128i a, __m128i b)
PSUBD: __m128i _mm_sub_epi32 (__m128i a, __m128i b)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
**PSUBQ—Subtract Packed Quadword Integers**

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F FB /r^1</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract quadword integer in mm1 from mm2 /m64.</td>
</tr>
<tr>
<td>PSUBQ mm1, mm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F FB /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract packed quadword integers in xmm1 from xmm2 /m128.</td>
</tr>
<tr>
<td>PSUBQ xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F:WIG FB/r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed quadword integers in xmm3/m128 from xmm2.</td>
</tr>
<tr>
<td>VPSUBQ xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**NOTES:**

### Instruction Operand Encoding

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<thead>
<tr>
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<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Subtracts the second operand (source operand) from the first operand (destination operand) and stores the result in the destination operand. The source operand can be a quadword integer stored in an MMX technology register or a 64-bit memory location, or it can be two packed quadword integers stored in an XMM register or an 128-bit memory location. The destination operand can be a quadword integer stored in an MMX technology register or two packed quadword integers stored in an XMM register. When packed quadword operands are used, a SIMD subtract is performed. When a quadword result is too large to be represented in 64 bits (overflow), the result is wrapped around and the low 64 bits are written to the destination element (that is, the carry is ignored).

Note that the PSUBQ instruction can operate on either unsigned or signed (two's complement notation) integers; however, it does not set bits in the EFLAGS register to indicate overflow and/or a carry. To prevent undetected overflow conditions, software must control the ranges of the values upon which it operates.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).
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128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.
VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise instructions will #UD.

Operation

PSUBQ (with 64-Bit operands)

DEST[63:0] ← DEST[63:0] − SRC[63:0];

PSUBQ (with 128-Bit operands)

DEST[63:0] ← DEST[63:0] − SRC[63:0];
DEST[127:64] ← DEST[127:64] − SRC[127:64];

VPSUBQ (VEX.128 encoded version)

DEST[63:0] ← SRC1[63:0]-SRC2[63:0]
DEST[127:64] ← SRC1[127:64]-SRC2[127:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents

PSUBQ: __m64 _mm_sub_si64(__m64 m1, __m64 m2)
PSUBQ: __m128i _mm_sub_epi64(__m128i m1, __m128i m2)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
### PSUBSB/PSUBSW—Subtract Packed Signed Integers with Signed Saturation

<table>
<thead>
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<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F E8 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Subtract signed packed bytes in <code>mm/m64</code> from signed packed bytes in <code>mm</code> and saturate results.</td>
</tr>
<tr>
<td>PSUBSB mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F E8 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract signed packed byte integers in <code>xmm2/m128</code> from packed signed byte integers in <code>xmm1</code> and saturate results.</td>
</tr>
<tr>
<td>PSUBSB xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F E9 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Subtract signed packed words in <code>mm/m64</code> from signed packed words in <code>mm</code> and saturate results.</td>
</tr>
<tr>
<td>PSUBSW mm, mm/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F E9 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract packed signed word integers in <code>xmm2/m128</code> from packed signed word integers in <code>xmm1</code> and saturate results.</td>
</tr>
<tr>
<td>PSUBSW xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG E8 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed signed byte integers in <code>xmm3/m128</code> from packed signed byte integers in <code>xmm2</code> and saturate results.</td>
</tr>
<tr>
<td>VPSUBSB xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG E9 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed signed word integers in <code>xmm3/m128</code> from packed signed word integers in <code>xmm2</code> and saturate results.</td>
</tr>
<tr>
<td>VPSUBSW xmm1, xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**NOTES:**

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**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD subtract of the packed signed integers of the source operand (second operand) from the packed signed integers of the destination operand (first operand), and stores the packed integer results in the destination operand. See Figure 9-4 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a SIMD operation. Overflow is handled with signed saturation, as described in the following paragraphs.

These instructions can operate on either 64-bit or 128-bit operands. When operating on 64-bit operands, the destination operand must be an MMX technology register and the source operand can be either an MMX technology register or a 64-bit memory location. When operating on 128-bit operands, the destination operand must be an XMM register and the source operand can be either an XMM register or a 128-bit memory location.

The PSUBSB instruction subtracts packed signed byte integers. When an individual byte result is beyond the range of a signed byte integer (that is, greater than 7FH or less than 80H), the saturated value of 7FH or 80H, respectively, is written to the destination operand.

The PSUBSW instruction subtracts packed signed word integers. When an individual word result is beyond the range of a signed word integer (that is, greater than 7FFFH or less than 8000H), the saturated value of 7FFFH or 8000H, respectively, is written to the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise instructions will #UD.

**Operation**

**PSUBSB (with 64-bit operands)**

\[
\text{DEST}[7:0] \leftarrow \text{SaturateToSignedByte}(\text{DEST}[7:0] - \text{SRC}[7:0]);
\]

(* Repeat subtract operation for 2nd through 7th bytes *)

\[
\text{DEST}[63:56] \leftarrow \text{SaturateToSignedByte}(\text{DEST}[63:56] - \text{SRC}[63:56]);
\]

**PSUBSB (with 128-bit operands)**

\[
\text{DEST}[7:0] \leftarrow \text{SaturateToSignedByte}(\text{DEST}[7:0] - \text{SRC}[7:0]);
\]
(* Repeat subtract operation for 2nd through 14th bytes *)

PSUBSW (with 64-bit operands)
(* Repeat subtract operation for 2nd and 7th words *)

PSUBSW (with 128-bit operands)
(* Repeat subtract operation for 2nd through 7th words *)

VPSUBSB
DEST[7:0] ← SaturateToSignedByte (SRC1[7:0] - SRC2[7:0]);
(* Repeat subtract operation for 2nd through 14th bytes *)
DEST[VLMAX-1:128] ← 0

VPSUBSW
DEST[15:0] ← SaturateToSignedWord (SRC1[15:0] - SRC2[15:0]);
(* Repeat subtract operation for 2nd through 7th words *)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PSUBSB: __m64 _mm_subs_pi8(__m64 m1, __m64 m2)
PSUBSB: __m128i _mm_subs_epi8(__m128i m1, __m128i m2)
PSUBSW: __m64 _mm_subs_pi16(__m64 m1, __m64 m2)
PSUBSW: __m128i _mm_subs_epi16(__m128i m1, __m128i m2)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
## PSUBUSB/PSUBUSW—Subtract Packed Unsigned Integers with Unsigned Saturation

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
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<tbody>
<tr>
<td>0F D8 /r&lt;sup&gt;1&lt;/sup&gt; PSUBUSB mm, mm/m64</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Subtract unsigned packed bytes in mm/m64 from unsigned packed bytes in mm and saturate result.</td>
</tr>
<tr>
<td>66 0F D8 /r PSUBUSB xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract packed unsigned byte integers in xmm2/m128 from packed unsigned byte integers in xmm1 and saturate result.</td>
</tr>
<tr>
<td>0F D9 /r&lt;sup&gt;1&lt;/sup&gt; PSUBUSW mm, mm/m64</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Subtract unsigned packed words in mm/m64 from unsigned packed words in mm and saturate result.</td>
</tr>
<tr>
<td>66 0F D9 /r PSUBUSW xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract packed unsigned word integers in xmm2/m128 from packed unsigned word integers in xmm1 and saturate result.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG D8 /r VPSUBUSB xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed unsigned byte integers in xmm3/m128 from packed unsigned byte integers in xmm2 and saturate result.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG D9 /r VPSUBUSW xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed unsigned word integers in xmm3/m128 from packed unsigned word integers in xmm2 and saturate result.</td>
</tr>
</tbody>
</table>

### NOTES:


---

4-406  Vol. 2B  PSUBUSB/PSUBUSW—Subtract Packed Unsigned Integers with Unsigned Saturation
**Description**

Performs a SIMD subtract of the packed unsigned integers of the source operand (second operand) from the packed unsigned integers of the destination operand (first operand), and stores the packed unsigned integer results in the destination operand. See Figure 9-4 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for an illustration of a SIMD operation. Overflow is handled with unsigned saturation, as described in the following paragraphs.

These instructions can operate on either 64-bit or 128-bit operands. When operating on 64-bit operands, the destination operand must be an MMX technology register and the source operand can be either an MMX technology register or a 64-bit memory location. When operating on 128-bit operands, the destination operand must be an XMM register and the source operand can be either an XMM register or a 128-bit memory location.

The PSUBUSB instruction subtracts packed unsigned byte integers. When an individual byte result is less than zero, the saturated value of 00H is written to the destination operand.

The PSUBUSW instruction subtracts packed unsigned word integers. When an individual word result is less than zero, the saturated value of 0000H is written to the destination operand.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise instructions will #UD.

**Operation**

**PSUBUSB (with 64-bit operands)**

\[
\text{DEST}[7:0] \leftarrow \text{SaturateToUnsignedByte} (\text{DEST}[7:0] - \text{SRC}[7:0]); \\
\text{DEST}[63:56] \leftarrow \text{SaturateToUnsignedByte} (\text{DEST}[63:56] - \text{SRC}[63:56]);
\]

**PSUBUSB (with 128-bit operands)**

\[
\text{DEST}[7:0] \leftarrow \text{SaturateToUnsignedByte} (\text{DEST}[7:0] - \text{SRC}[7:0]); \\
\text{DEST}[127:120] \leftarrow \text{SaturateToUnsignedByte} (\text{DEST}[127:120] - \text{SRC}[127:120]);
\]
INSTRUCTION SET REFERENCE, M-Z

PSUBUSW (with 64-bit operands)
DEST[15:0] ← SaturateToUnsignedWord (DEST[15:0] − SRC[15:0]);
(* Repeat add operation for 2nd and 3rd words *)

PSUBUSW (with 128-bit operands)
DEST[15:0] ← SaturateToUnsignedWord (DEST[15:0] − SRC[15:0]);
(* Repeat add operation for 2nd through 7th words *)

VPSUBUSB
DEST[7:0] ← SaturateToUnsignedByte (SRC1[7:0] - SRC2[7:0]);
(* Repeat subtract operation for 2nd through 14th bytes *)
DEST[127:120] ← SaturateToUnsignedByte (SRC1[127:120] - SRC2[127:120]);
DEST[VLMAX-1:128] ← 0

VPSUBUSW
DEST[15:0] ← SaturateToUnsignedWord (SRC1[15:0] - SRC2[15:0]);
(* Repeat subtract operation for 2nd through 7th words *)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PSUBUSB: __m64 _mm_subs_pu8(__m64 m1, __m64 m2)
PSUBUSB: __m128i _mm_subs_epu8(__m128i m1, __m128i m2)
PSUBUSW: __m64 _mm_subs_pu16(__m64 m1, __m64 m2)
PSUBUSW: __m128i _mm_subs_epu16(__m128i m1, __m128i m2)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PTEST- Logical Compare

**Description**

PTEST and VPTEST set the ZF flag if all bits in the result are 0 of the bitwise AND of the first source operand (first operand) and the second source operand (second operand). VPTEST sets the CF flag if all bits in the result are 0 of the bitwise AND of the second source operand (second operand) and the logical NOT of the destination operand.

The first source register is specified by the ModR/M reg field.

128-bit versions: The first source register is an XMM register. The second source register can be an XMM register or a 128-bit memory location. The destination register is not modified.

VEX.256 encoded version: The first source register is a YMM register. The second source register can be a YMM register or a 256-bit memory location. The destination register is not modified.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

**Operation**

(V)PTEST (128-bit version)

\[
\begin{align*}
\text{IF } & \left( \text{SRC}[127:0] \right) \text{ BITWISE AND } \text{DEST}[127:0] = 0 \\
\text{THEN } & \text{ZF } \leftarrow 1; \\
\text{ELSE } & \text{ZF } \leftarrow 0;
\end{align*}
\]

**Opcode/Description**

<table>
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<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
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</thead>
<tbody>
<tr>
<td>66 0F 38 17 /r PTEST xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>SSE4_1</td>
<td>Set ZF if xmm2/m128 AND xmm1 result is all 0s. Set CF if xmm2/m128 AND NOT xmm1 result is all 0s.</td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.WIG 17 /r VPTEST xmm1, xmm2/m128</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Set ZF and CF depending on bitwise AND and ANDN of sources.</td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F38.WIG 17 /r VPTEST ymm1, ymm2/m256</td>
<td>RM V/V</td>
<td>AVX</td>
<td>Set ZF and CF depending on bitwise AND and ANDN of sources.</td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
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<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
IF (SRC[127:0] BITWISE AND NOT DEST[127:0] = 0)
    THEN CF ← 1;
    ELSE CF ← 0;
DEST (unmodified)
AF ← OF ← PF ← SF ← 0;

VPTEST (VEX.256 encoded version)
IF (SRC[255:0] BITWISE AND DEST[255:0] = 0) THEN ZF ← 1;
    ELSE ZF ← 0;
IF (SRC[255:0] BITWISE AND NOT DEST[255:0] = 0) THEN CF ← 1;
    ELSE CF ← 0;
DEST (unmodified)
AF ← OF ← PF ← SF ← 0;

Intel C/C++ Compiler Intrinsic Equivalent
PTEST
int _mm_testz_si128 (__m128i s1, __m128i s2);
int _mm_testc_si128 (__m128i s1, __m128i s2);
int _mm_testnzc_si128 (__m128i s1, __m128i s2);

VPTEST
int _mm256_testz_si256 (__m256i s1, __m256i s2);
int _mm256_testc_si256 (__m256i s1, __m256i s2);
int _mm256_testnzc_si256 (__m256i s1, __m256i s2);

Flags Affected
The OF, AF, PF, SF flags are cleared and the ZF, CF flags are set according to the operation.

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.vvvv != 1111B.
**PUNPCKHBW/PUNPCKHWD/PUNPCKHDQ/PUNPCKHQDQ— Unpack High Data**

<table>
<thead>
<tr>
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<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>0F 68 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM</td>
<td>V/V</td>
<td>MMX</td>
<td>Unpack and interleave high-order bytes from <em>mm</em> and <em>mm/m64</em> into <em>mm</em>.</td>
</tr>
<tr>
<td>PUNPCKHBW <em>mm, mm/m64</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 68 /r</td>
<td></td>
<td>V/V</td>
<td>SSE2</td>
<td>Unpack and interleave high-order bytes from <em>xmm1</em> and <em>xmm2/m128</em> into <em>xmm1</em>.</td>
</tr>
<tr>
<td>PUNPCKHBW <em>xmm1, xmm2/m128</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 69 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td>V/V</td>
<td>MMX</td>
<td>Unpack and interleave high-order words from <em>mm</em> and <em>mm/m64</em> into <em>mm</em>.</td>
</tr>
<tr>
<td>PUNPCKHWD <em>mm, mm/m64</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 69 /r</td>
<td></td>
<td>V/V</td>
<td>SSE2</td>
<td>Unpack and interleave high-order words from <em>xmm1</em> and <em>xmm2/m128</em> into <em>xmm1</em>.</td>
</tr>
<tr>
<td>PUNPCKHWD <em>xmm1, xmm2/m128</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 6A /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td>V/V</td>
<td>MMX</td>
<td>Unpack and interleave high-order doublewords from <em>mm</em> and <em>mm/m64</em> into <em>mm</em>.</td>
</tr>
<tr>
<td>PUNPCKHDQ <em>mm, mm/m64</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 6A /r</td>
<td></td>
<td>V/V</td>
<td>SSE2</td>
<td>Unpack and interleave high-order doublewords from <em>xmm1</em> and <em>xmm2/m128</em> into <em>xmm1</em>.</td>
</tr>
<tr>
<td>PUNPCKHDQ <em>xmm1, xmm2/m128</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 6D /r</td>
<td></td>
<td>V/V</td>
<td>SSE2</td>
<td>Unpack and interleave high-order quadwords from <em>xmm1</em> and <em>xmm2/m128</em> into <em>xmm1</em>.</td>
</tr>
<tr>
<td>PUNPCKHQDQ <em>xmm1, xmm2/m128</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 68/r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Interleave high-order bytes from <em>xmm2</em> and <em>xmm3/m128</em> into <em>xmm1</em>.</td>
</tr>
<tr>
<td>VPUNPCKHBW <em>xmm1,xmm2, xmm3/m128</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 69/r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Interleave high-order words from <em>xmm2</em> and <em>xmm3/m128</em> into <em>xmm1</em>.</td>
</tr>
<tr>
<td>VPUNPCKHWD <em>xmm1,xmm2, xmm3/m128</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 6A/r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Interleave high-order doublewords from <em>xmm2</em> and <em>xmm3/m128</em> into <em>xmm1</em>.</td>
</tr>
<tr>
<td>VPUNPCKHDQ <em>xmm1, xmm2, xmm3/m128</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*PUNPCKHBW/PUNPCKHWD/PUNPCKHDQ/PUNPCKHQDQ— Unpack High Data*
INSTRUCTION SET REFERENCE, M-Z

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>VEX.NDS.128.66.0F.WIG 6D/r VPUNPCKHQDQ xmm1, xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Interleave high-order quadword from xmm2 and xmm3/m128 into xmm1 register.</td>
</tr>
</tbody>
</table>

NOTES:

Instruction Operand Encoding

<table>
<thead>
<tr>
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<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Unpacks and interleaves the high-order data elements (bytes, words, doublewords, or quadwords) of the destination operand (first operand) and source operand (second operand) into the destination operand. Figure 4-15 shows the unpack operation for bytes in 64-bit operands. The low-order data elements are ignored.

![Figure 4-15. PUNPCKHBW Instruction Operation Using 64-bit Operands](image-url)

The source operand can be an MMX technology register or a 64-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register. When the source data comes from a 64-bit memory operand, the full 64-bit operand is accessed from memory, but the instruction uses only the high-order 32 bits. When the source data comes from a
128-bit memory operand, an implementation may fetch only the appropriate 64 bits; however, alignment to a 16-byte boundary and normal segment checking will still be enforced.

The PUNPCKHBW instruction interleaves the high-order bytes of the source and destination operands, the PUNPCKHWD instruction interleaves the high-order words of the source and destination operands, the PUNPCKHDQ instruction interleaves the high-order doubleword (or doublewords) of the source and destination operands, and the PUNPCKHQDQ instruction interleaves the high-order quadwords of the source and destination operands.

These instructions can be used to convert bytes to words, words to doublewords, doublewords to quadwords, and quadwords to double quadwords, respectively, by placing all 0s in the source operand. Here, if the source operand contains all 0s, the result (stored in the destination operand) contains zero extensions of the high-order data elements from the original value in the destination operand. For example, with the PUNPCKHBW instruction the high-order bytes are zero extended (that is, unpacked into unsigned word integers), and with the PUNPCKHWD instruction, the high-order words are zero extended (unpacked into unsigned doubleword integers).

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE versions: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded versions: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise instructions will #UD.

**Operation**

PUNPCKHBW instruction with 64-bit operands:
- DEST[7:0] ← DEST[39:32];
- DEST[23:16] ← DEST[47:40];
- DEST[31:24] ← SRC[47:40];
- DEST[47:40] ← SRC[55:48];
- DEST[55:48] ← DEST[63:56];
- DEST[63:56] ← SRC[63:56];

PUNPCKHWD instruction with 64-bit operands:
- DEST[15:0] ← DEST[47:32];
- DEST[31:16] ← SRC[47:32];
- DEST[47:32] ← DEST[63:48];
- DEST[63:48] ← SRC[63:48];

PUNPCKHDQ instruction with 64-bit operands:
- DEST[31:0] ← DEST[63:32];
INSTRUCTION SET REFERENCE, M-Z

DEST[63:32] ← SRC[63:32];
PUNPCKHBW instruction with 128-bit operands:
  DEST[7:0] ← DEST[71:64];
  DEST[15:8] ← SRC[71:64];
  DEST[23:16] ← DEST[79:72];
  DEST[31:24] ← SRC[79:72];
  DEST[39:32] ← DEST[87:80];
  DEST[47:40] ← SRC[87:80];
  DEST[55:48] ← DEST[95:88];
  DEST[63:56] ← SRC[95:88];
  DEST[71:64] ← DEST[103:96];
  DEST[79:72] ← SRC[103:96];
  DEST[87:80] ← DEST[111:104];
  DEST[95:88] ← SRC[111:104];
  DEST[103:96] ← DEST[119:112];
  DEST[111:104] ← SRC[119:112];
  DEST[119:112] ← DEST[127:120];
  DEST[127:120] ← SRC[127:120];
PUNPCKHWD instruction with 128-bit operands:
  DEST[15:0] ← DEST[79:64];
  DEST[31:16] ← SRC[79:64];
  DEST[47:32] ← DEST[95:80];
  DEST[63:48] ← SRC[95:80];
  DEST[79:64] ← DEST[111:96];
  DEST[95:80] ← SRC[111:96];
  DEST[111:96] ← DEST[127:112];
  DEST[127:112] ← SRC[127:112];
PUNPCKHDQ instruction with 128-bit operands:
  DEST[31:0] ← DEST[95:64];
  DEST[63:32] ← SRC[95:64];
  DEST[95:64] ← DEST[127:96];
  DEST[127:96] ← SRC[127:96];
PUNPCKHQDQ instruction:
  DEST[63:0] ← DEST[127:64];
  DEST[127:64] ← SRC[127:64];
PUNPCKHBW
  DEST[127:0] ← INTERLEAVE_HIGH_BYTES(DEST, SRC)
  DEST[VLMAX-1:128] (Unmodified)
VPUNPCKHBW
DEST[127:0] \leftrightarrow \text{INTERLEAVE\_HIGH\_BYTES(SRC1, SRC2)} \\
DEST[VLMAX-1:128] \leftrightarrow 0

**PUNPCKHWD** \\
DEST[127:0] \leftrightarrow \text{INTERLEAVE\_HIGH\_WORDS(DEST, SRC)} \\
DEST[VLMAX-1:128] (Unmodified)

**VPUNPCKHWD** \\
DEST[127:0] \leftrightarrow \text{INTERLEAVE\_HIGH\_WORDS(SRC1, SRC2)} \\
DEST[VLMAX-1:128] \leftrightarrow 0

**PUNPCKHDQ** \\
DEST[127:0] \leftrightarrow \text{INTERLEAVE\_HIGH\_DWORDS(DEST, SRC)} \\
DEST[VLMAX-1:128] (Unmodified)

**VPUNPCKHDQ** \\
DEST[127:0] \leftrightarrow \text{INTERLEAVE\_HIGH\_DWORDS(SRC1, SRC2)} \\
DEST[VLMAX-1:128] \leftrightarrow 0

**PUNPCKHQDQ** \\
DEST[127:0] \leftrightarrow \text{INTERLEAVE\_HIGH\_QWORDS(DEST, SRC)} \\
DEST[VLMAX-1:128] (Unmodified)

**VPUNPCKHQDQ** \\
DEST[127:0] \leftrightarrow \text{INTERLEAVE\_HIGH\_QWORDS(SRC1, SRC2)} \\
DEST[VLMAX-1:128] \leftrightarrow 0

**Intel C/C++ Compiler Intrinsic Equivalents**

- **PUNPCKHBw:** \_m64 \_mm\_unpackhi\_pi8(\_m64 m1, \_m64 m2)
- **PUNPCKHBw:** \_m128i \_mm\_unpackhi\_epi8(\_m128i m1, \_m128i m2)
- **PUNPCKHWD:** \_m64 \_mm\_unpackhi\_pi16(\_m64 m1, \_m64 m2)
- **PUNPCKHWD:** \_m128i \_mm\_unpackhi\_epi16(\_m128i m1, \_m128i m2)
- **PUNPCKHDQ:** \_m64 \_mm\_unpackhi\_pi32(\_m64 m1, \_m64 m2)
- **PUNPCKHDQ:** \_m128i \_mm\_unpackhi\_epi32(\_m128i m1, \_m128i m2)
- **PUNPCKHQDQ:** \_m128i \_mm\_unpackhi\_epi64 (\_m128i a, \_m128i b)

**Flags Affected**

None.
INSTRUCTION SET REFERENCE, M-Z

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
### PUNPCKLBw/PUNPCKLWD/PUNPCKLDQ/PUNPCKLQDQ— Unpack Low Data

<table>
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<tr>
<th>Opcode/ Instruction</th>
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<tbody>
<tr>
<td>0F 60 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM V/V</td>
<td>MMX</td>
<td>Interleave low-order bytes from mm and mm/m32 into mm.</td>
<td></td>
</tr>
<tr>
<td>PUNPCKLBw mm, mm/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 60 /r</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Interleave low-order bytes from xmm1 and xmm2/m128 into xmm1.</td>
<td></td>
</tr>
<tr>
<td>PUNPCKLBw xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 61 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM V/V</td>
<td>MMX</td>
<td>Interleave low-order words from mm and mm/m32 into mm.</td>
<td></td>
</tr>
<tr>
<td>PUNPCKLWD mm, mm/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 61 /r</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Interleave low-order words from xmm1 and xmm2/m128 into xmm1.</td>
<td></td>
</tr>
<tr>
<td>PUNPCKLWD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 62 /r&lt;sup&gt;1&lt;/sup&gt;</td>
<td>RM V/V</td>
<td>MMX</td>
<td>Interleave low-order doublewords from mm and mm/m32 into mm.</td>
<td></td>
</tr>
<tr>
<td>PUNPCKLDQ mm, mm/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 62 /r</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Interleave low-order doublewords from xmm1 and xmm2/m128 into xmm1.</td>
<td></td>
</tr>
<tr>
<td>PUNPCKLDQ xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66 0F 6C /r</td>
<td>RM V/V</td>
<td>SSE2</td>
<td>Interleave low-order quadword from xmm1 and xmm2/m128 into xmm1 register.</td>
<td></td>
</tr>
<tr>
<td>PUNPCKLQDQ xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VEX.NDS.128.66.0F.WIG**

- 60/r | Interleave low-order bytes from xmm2 and xmm3/m128 into xmm1. |
- VEX.NDS.128.66.0F.WIG 61/r | Interleave low-order words from xmm2 and xmm3/m128 into xmm1. |
- VEX.NDS.128.66.0F.WIG 62/r | Interleave low-order doublewords from xmm2 and xmm3/m128 into xmm1. |
### INSTRUCTION SET REFERENCE, M-Z

**PUNPCKLBW/PUNPCKLWD/PUNPCKLDQ/PUNPCKLQDQ— Unpack Low Data**

#### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Description

Unpacks and interleaves the low-order data elements (bytes, words, doublewords, and quadwords) of the destination operand (first operand) and source operand (second operand) into the destination operand. (Figure 4-16 shows the unpack operation for bytes in 64-bit operands.). The high-order data elements are ignored.

![Figure 4-16. PUNPCKLBW Instruction Operation Using 64-bit Operands](image)

The source operand can be an MMX technology register or a 32-bit memory location, or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register. When the source data comes from a 128-bit memory operand, an implementation may fetch only the appropriate 64 bits; however, alignment to a 16-byte boundary and normal segment checking will still be enforced.

**NOTES:**

The PUNPCKLBW instruction interleaves the low-order bytes of the source and destination operands, the PUNPCKLWD instruction interleaves the low-order words of the source and destination operands, the PUNPCKLDQ instruction interleaves the low-order doublewords (or doublewords) of the source and destination operands, and the PUNPCKLQDQ instruction interleaves the low-order quadwords of the source and destination operands.

These instructions can be used to convert bytes to words, words to doublewords, doublewords to quadwords, and quadwords to double quadwords, respectively, by placing all 0s in the source operand. Here, if the source operand contains all 0s, the result (stored in the destination operand) contains zero extensions of the high-order data elements from the original value in the destination operand. For example, with the PUNPCKLBW instruction the high-order bytes are zero extended (that is, unpacked into unsigned word integers), and with the PUNPCKLWD instruction, the high-order words are zero extended (unpacked into unsigned doubleword integers).

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE versions: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded versions: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise instructions will #UD.

**Operation**

PUNPCKLBW instruction with 64-bit operands:

\[
\begin{align*}
&\text{DEST}[63:56] \leftarrow \text{SRC}[31:24]; \\
&\text{DEST}[55:48] \leftarrow \text{DEST}[31:24]; \\
&\text{DEST}[47:40] \leftarrow \text{SRC}[23:16]; \\
&\text{DEST}[39:32] \leftarrow \text{DEST}[23:16]; \\
&\text{DEST}[31:24] \leftarrow \text{SRC}[15:8]; \\
&\text{DEST}[23:16] \leftarrow \text{DEST}[15:8]; \\
&\text{DEST}[15:8] \leftarrow \text{SRC}[7:0]; \\
&\text{DEST}[7:0] \leftarrow \text{DEST}[7:0];
\end{align*}
\]

PUNPCKLWD instruction with 64-bit operands:

\[
\begin{align*}
&\text{DEST}[63:48] \leftarrow \text{SRC}[31:16]; \\
&\text{DEST}[47:32] \leftarrow \text{DEST}[31:16]; \\
&\text{DEST}[31:16] \leftarrow \text{SRC}[15:0]; \\
&\text{DEST}[15:0] \leftarrow \text{DEST}[15:0];
\end{align*}
\]

PUNPCKLDQ instruction with 64-bit operands:

\[
\begin{align*}
&\text{DEST}[63:32] \leftarrow \text{SRC}[31:0]; \\
&\text{DEST}[31:0] \leftarrow \text{DEST}[31:0];
\end{align*}
\]

PUNPCKLBW instruction with 128-bit operands:

\[
\begin{align*}
&\text{DEST}[7:0] \leftarrow \text{DEST}[7:0];
\end{align*}
\]

PUNPCKLBW/PUNPCKLWD/PUNPCKLDQ/PUNPCKLQDQ— Unpack Low Data
INSTRUCTION SET REFERENCE, M-Z

DEST[15:8] ← SRC[7:0];
DEST[23:16] ← DEST[15:8];
DEST[31:24] ← SRC[15:8];
DEST[47:40] ← SRC[23:16];
DEST[55:48] ← DEST[31:24];
DEST[63:56] ← SRC[31:24];
DEST[71:64] ← DEST[39:32];
DEST[79:72] ← SRC[39:32];
DEST[87:80] ← DEST[47:40];
DEST[95:88] ← SRC[47:40];
DEST[103:96] ← DEST[55:48];
DEST[111:104] ← SRC[55:48];
DEST[119:112] ← DEST[63:56];
DEST[127:120] ← SRC[63:56];

PUNPCKLWD instruction with 128-bit operands:
DEST[15:0] ← DEST[15:0];
DEST[31:16] ← SRC[15:0];
DEST[47:32] ← DEST[31:16];
DEST[63:48] ← SRC[31:16];
DEST[79:64] ← DEST[47:32];
DEST[95:80] ← SRC[47:32];
DEST[111:96] ← DEST[63:48];
DEST[127:112] ← SRC[63:48];

PUNPCKLDQ instruction with 128-bit operands:
DEST[31:0] ← DEST[31:0];
DEST[63:32] ← SRC[31:0];
DEST[95:64] ← DEST[63:32];
DEST[127:96] ← SRC[63:32];

PUNPCKLQDQ
DEST[63:0] ← DEST[63:0];
DEST[127:64] ← SRC[63:0];

VPUNPCKLBW
DEST[127:0] ← INTERLEAVE_BYTES(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

VPUNPCKLWD
DEST[127:0] ← INTERLEAVE_WORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0
VPUNPCKLDQ
DEST[127:0] ← INTERLEAVE_DWORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

VPUNPCKLQDQ
DEST[127:0] ← INTERLEAVE_QWORDS(SRC1, SRC2)
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalents
PUNPCKLBW: __m64 _mm_unpacklo_pi8 (__m64 m1, __m64 m2)
PUNPCKLBW: __m128i _mm_unpacklo_epi8 (__m128i m1, __m128i m2)
PUNPCKLWD: __m64 _mm_unpacklo_pi16 (__m64 m1, __m64 m2)
PUNPCKLWD: __m128i _mm_unpacklo_epi16 (__m128i m1, __m128i m2)
PUNPCKLDQ: __m64 _mm_unpacklo_pi32 (__m64 m1, __m64 m2)
PUNPCKLDQ: __m128i _mm_unpacklo_epi32 (__m128i m1, __m128i m2)
PUNPCKLQDQ: __m128i _mm_unpacklo_epi64 (__m128i m1, __m128i m2)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
PUSH—Push Word, Doubleword or Quadword Onto the Stack

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF /6</td>
<td>PUSH r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Push r/m16.</td>
</tr>
<tr>
<td>FF /6</td>
<td>PUSH r/m32</td>
<td>M</td>
<td>N.E.</td>
<td>Valid</td>
<td>Push r/m32.</td>
</tr>
<tr>
<td>FF /6</td>
<td>PUSH r/m64</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Push r/m64.</td>
</tr>
<tr>
<td>50+rw</td>
<td>PUSH r16</td>
<td>O</td>
<td>Valid</td>
<td>Valid</td>
<td>Push r16.</td>
</tr>
<tr>
<td>50+rd</td>
<td>PUSH r32</td>
<td>O</td>
<td>N.E.</td>
<td>Valid</td>
<td>Push r32.</td>
</tr>
<tr>
<td>50+rd</td>
<td>PUSH r64</td>
<td>O</td>
<td>Valid</td>
<td>N.E.</td>
<td>Push r64.</td>
</tr>
<tr>
<td>6B</td>
<td>PUSH imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Push imm16.</td>
</tr>
<tr>
<td>6B</td>
<td>PUSH imm32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Push imm32.</td>
</tr>
<tr>
<td>0E</td>
<td>PUSH CS</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Push CS.</td>
</tr>
<tr>
<td>16</td>
<td>PUSH SS</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Push SS.</td>
</tr>
<tr>
<td>1E</td>
<td>PUSH DS</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Push DS.</td>
</tr>
<tr>
<td>06</td>
<td>PUSH ES</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Push ES.</td>
</tr>
<tr>
<td>0F A0</td>
<td>PUSH FS</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Push FS.</td>
</tr>
<tr>
<td>0F A8</td>
<td>PUSH GS</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Push GS.</td>
</tr>
</tbody>
</table>

NOTES:
* See IA-32 Architecture Compatibility section below.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0</td>
<td>opcode + rd (w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>I</td>
<td>imm8/16/32</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
Decrement the stack pointer and then stores the source operand on the top of the stack. Address and operand sizes are determined and used as follows:

- Address size. The D flag in the current code-segment descriptor determines the default address size; it may be overridden by an instruction prefix (67H).

The address size is used only when referencing a source operand in memory.
• **Operand size.** The D flag in the current code-segment descriptor determines the default operand size; it may be overridden by instruction prefixes (66H or REX.W).

  The operand size (16, 32, or 64 bits) determines the amount by which the stack pointer is decremented (2, 4 or 8).

  If the source operand is an immediate and its size is less than the operand size, a sign-extended value is pushed on the stack. If the source operand is a segment register (16 bits) and the operand size is greater than 16 bits, a zero-extended value is pushed on the stack.

• **Stack-address size.** Outside of 64-bit mode, the B flag in the current stack-segment descriptor determines the size of the stack pointer (16 or 32 bits); in 64-bit mode, the size of the stack pointer is always 64 bits.

  The stack-address size determines the width of the stack pointer when writing to the stack in memory and when decrementing the stack pointer. (As stated above, the amount by which the stack pointer is decremented is determined by the operand size.)

  If the operand size is less than the stack-address size, the PUSH instruction may result in a misaligned stack pointer (a stack pointer that is not aligned on a doubleword or quadword boundary).

The PUSH ESP instruction pushes the value of the ESP register as it existed before the instruction was executed. If a PUSH instruction uses a memory operand in which the ESP register is used for computing the operand address, the address of the operand is computed before the ESP register is decremented.

If the ESP or SP register is 1 when the PUSH instruction is executed in real-address mode, a stack-fault exception (#SS) is generated (because the limit of the stack segment is violated). Its delivery encounters a second stack-fault exception (for the same reason), causing generation of a double-fault exception (#DF). Delivery of the double-fault exception encounters a third stack-fault exception, and the logical processor enters shutdown mode. See the discussion of the double-fault exception in Chapter 6 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.*

**IA-32 Architecture Compatibility**

For IA-32 processors from the Intel 286 on, the PUSH ESP instruction pushes the value of the ESP register as it existed before the instruction was executed. (This is also true for Intel 64 architecture, real-address and virtual-8086 modes of IA-32 architecture.) For the Intel® 8086 processor, the PUSH SP instruction pushes the new value of the SP register (that is the value after it has been decremented by 2).

**Operation**

IF SRC is a segment register

THEN

```
PUSH—Push Word, Doubleword or Quadword Onto the Stack
```
IF operand size = 16
    THEN TEMP ← SRC;
    ELSE TEMP ← ZeroExtend(SRC); (* extend to operand size *)
FI;
ELSE IF SRC is immediate byte
    THEN TEMP ← SignExtend(SRC); (* extend to operand size *)
    ELSE IF SRC is immediate word
        THEN TEMP ← SRC; (* operand size is 16 *)
    ELSE IF SRC is immediate doubleword
        THEN
            IF operand size = 32
                THEN TEMP ← SRC;
                ELSE TEMP ← SignExtend(SRC); (* extend to operand size of 64 *)
            FI;
        ELSE IF SRC is in memory
            THEN TEMP ← SRC; (* use address and operand sizes *)
            ELSE TEMP ← SRC; (* SRC is register; use operand size *)
        FI;
    ELSE IF SRC is in memory
        THEN TEMP ← SRC; (* use address and operand sizes *)
        ELSE TEMP ← SRC; (* SRC is register; use operand size *)
    FI;
IF in 64-bit mode
    THEN
        IF operand size = 64
            THEN
                ESP ← ESP − 4;
                Memory[SS:ESP] ← TEMP; (* Push doubleword *)
            ELSE
                ESP ← ESP − 2;
                Memory[SS:ESP] ← TEMP; (* Push word *)
            FI;
        ELSE IF stack-address size = 32
            THEN
                IF operand size = 32
                    THEN
                        RSP ← RSP − 8;
                        Memory[RSP] ← TEMP; (* Push quadword *)
                    ELSE
                        RSP ← RSP − 2;
                        Memory[RSP] ← TEMP; (* Push word *)
                    FI;
                ELSE IF stack-address size = 32
                    THEN
                        IF operand size = 32
                            THEN
                                SP ← SP − 8;
                                Memory[SS:SP] ← TEMP; (* Push doubleword *)
                            ELSE
                                SP ← SP − 4;
                                Memory[SS:SP] ← TEMP; (* Push word *)
                            FI;
                        ELSE IF stack-address size = 32
                            THEN
                                IF operand size = 32
                                    THEN
                                        ESP ← ESP − 8;
                                        Memory[SS:ESP] ← TEMP; (* Push quadword *)
                                    ELSE
                                        ESP ← ESP − 4;
                                        Memory[SS:ESP] ← TEMP; (* Push word *)
                                    FI;
                                ELSE IF stack-address size = 32
                                    THEN
                                        IF operand size = 32
                                            THEN
                                                RSP ← RSP − 8;
                                                Memory[RSP] ← TEMP; (* Push quadword *)
                                            ELSE
                                                RSP ← RSP − 4;
                                                Memory[RSP] ← TEMP; (* Push word *)
                                            FI;
                                        ELSE IF stack-address size = 32
                                            THEN
                                                IF operand size = 32
                                                    THEN
                                                        SP ← SP − 8;
                                                        Memory[SS:SP] ← TEMP; (* Push doubleword *)
                                                    ELSE
                                                        SP ← SP − 4;
                                                        Memory[SS:SP] ← TEMP; (* Push word *)
                                                    FI;
INSTRUCTION SET REFERENCE, M-Z

PUSH—Push Word, Doubleword or Quadword Onto the Stack

ELSE (* operand size = 16 *)
    SP ← SP − 2;
    Memory[SS:SP] ← TEMP; (* Push word *)
FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
    If the new value of the SP or ESP register is outside the stack segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, M-Z

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
#SS(0) If the stack address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
PUSHA/PUSHAD—Push All General-Purpose Registers

Description

Pushes the contents of the general-purpose registers onto the stack. The registers are stored on the stack in the following order: EAX, ECX, EDX, EBX, ESP (original value), EBP, ESI, and EDI (if the current operand-size attribute is 32) and AX, CX, DX, BX, SP (original value), BP, SI, and DI (if the operand-size attribute is 16). These instructions perform the reverse operation of the POPA/POPAD instructions. The value pushed for the ESP or SP register is its value before prior to pushing the first register (see the "Operation" section below).

The PUSHA (push all) and PUSHAD (push all double) mnemonics reference the same opcode. The PUSHA instruction is intended for use when the operand-size attribute is 16 and the PUSHAD instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when PUSHA is used and to 32 when PUSHAD is used. Others may treat these mnemonics as synonyms (PUSHA/PUSHAD) and use the current setting of the operand-size attribute to determine the size of values to be pushed from the stack, regardless of the mnemonic used.

In the real-address mode, if the ESP or SP register is 1, 3, or 5 when PUSHA/PUSHAD executes: an #SS exception is generated but not delivered (the stack error reported prevents #SS delivery). Next, the processor generates a #DF exception and enters a shutdown state as described in the #DF discussion in Chapter 6 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

This instruction executes as described in compatibility mode and legacy mode. It is not valid in 64-bit mode.

Operation

IF 64-bit Mode

THEN #UD
IF OperandSize = 32 (* PUSHAD instruction *)
THEN
   Temp ← (ESP);
   Push(EAX);
   Push(ECX);
   Push(EDX);
   Push(EBX);
   Push(Temp);
   Push(EBP);
   Push(ESI);
   Push(EDI);
ELSE (* OperandSize = 16, PUSHA instruction *)
   Temp ← (SP);
   Push(AX);
   Push(CX);
   Push(DX);
   Push(BX);
   Push(Temp);
   Push(BP);
   Push(SI);
   Push(DI);
FI;

Flags Affected
None.

Protected Mode Exceptions
#SS(0) If the starting or ending stack address is outside the stack segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference is made while the current privilege level is 3 and alignment checking is enabled.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If the ESP or SP register contains 7, 9, 11, 13, or 15.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If the ESP or SP register contains 7, 9, 11, 13, or 15.
PUSHA/PUSHAD—Push All General-Purpose Registers

#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference is made while alignment checking is enabled.
#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
#UD If in 64-bit mode.
PUSHF/PUSHFD—Push EFLAGS Register onto the Stack

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/ En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9C</td>
<td>PUSHF</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Push lower 16 bits of EFLAGS.</td>
</tr>
<tr>
<td>9C</td>
<td>PUSHFD</td>
<td>NP</td>
<td>N.E.</td>
<td>Valid</td>
<td>Push EFLAGS.</td>
</tr>
<tr>
<td>9C</td>
<td>PUSHFQ</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Push RFLAGS.</td>
</tr>
</tbody>
</table>

Description

Decrement the stack pointer by 4 (if the current operand-size attribute is 32) and pushes the entire contents of the EFLAGS register onto the stack, or decrements the stack pointer by 2 (if the operand-size attribute is 16) and pushes the lower 16 bits of the EFLAGS register (that is, the FLAGS register) onto the stack. These instructions reverse the operation of the POPF/POPFD instructions.

When copying the entire EFLAGS register to the stack, the VM and RF flags (bits 16 and 17) are not copied; instead, the values for these flags are cleared in the EFLAGS image stored on the stack. See Chapter 3 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for more information about the EFLAGS register.

The PUSHF (push flags) and PUSHFD (push flags double) mnemonics reference the same opcode. The PUSHF instruction is intended for use when the operand-size attribute is 16 and the PUSHFD instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when PUSHF is used and to 32 when PUSHFD is used. Others may treat these mnemonics as synonyms (PUSHF/PUSHFD) and use the current setting of the operand-size attribute to determine the size of values to be pushed from the stack, regardless of the mnemonic used.

In 64-bit mode, the instruction’s default operation is to decrement the stack pointer (RSP) by 8 and pushes RFLAGS on the stack. 16-bit operation is supported using the operand size override prefix 66H. 32-bit operand size cannot be encoded in this mode. When copying RFLAGS to the stack, the VM and RF flags (bits 16 and 17) are not copied; instead, values for these flags are cleared in the RFLAGS image stored on the stack.

When in virtual-8086 mode and the I/O privilege level (IOPL) is less than 3, the PUSHF/PUSHFD instruction causes a general protection exception (#GP).
In the real-address mode, if the ESP or SP register is 1 when PUSHF/PUSHFD instruction executes: an #SS exception is generated but not delivered (the stack error reported prevents #SS delivery). Next, the processor generates a #DF exception and enters a shutdown state as described in the #DF discussion in Chapter 6 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

**Operation**

IF (PE = 0) or (PE = 1 and ((VM = 0) or (VM = 1 and IOPL = 3)))
(* Real-Address Mode, Protected mode, or Virtual-8086 mode with IOPL equal to 3 *)
THEN
   IF OperandSize = 32
       THEN
           push (EFLAGS AND 00FCFFFFH);
               (* VM and RF EFLAG bits are cleared in image stored on the stack *)
       ELSE
           push (EFLAGS); (* Lower 16 bits only *)
       FI;
   ELSE IF 64-bit MODE (* In 64-bit Mode *)
       IF OperandSize = 64
           THEN
               push (RFLAGS AND 00000000_00FCFFFFH);
                   (* VM and RF RFLAG bits are cleared in image stored on the stack; *)
           ELSE
               push (EFLAGS); (* Lower 16 bits only *)
           FI;
       ELSE (* In Virtual-8086 Mode with IOPL less than 3 *)
           #GP(0); (* Trap to virtual-8086 monitor *)
       FI;

**Flags Affected**

None.

**Protected Mode Exceptions**

#SS(0) If the new value of the ESP register is outside the stack segment boundary.

#PF(fault-code) If a page fault occurs.

#AC(0) If an unaligned memory reference is made while the current privilege level is 3 and alignment checking is enabled.

#UD If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, M-Z

Real-Address Mode Exceptions
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If the I/O privilege level is less than 3.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference is made while alignment checking is enabled.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0) If the memory address is in a non-canonical form.
#SS(0) If the stack address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory reference is made while the current privilege level is 3 and alignment checking is enabled.
#UD If the LOCK prefix is used.
PXOR—Logical Exclusive OR

**Opcode*/Instruction | Op/En | 64/32 bit Mode Support | CPUID Feature Flag | Description
---|---|---|---|---
0F EF /r¹ | RM | V/V | MMX | Bitwise XOR of mm/m64 and mm.
66 0F EF /r | RM | V/V | SSE2 | Bitwise XOR of xmm2/m128 and xmm1.
VEX.NDS.128.66.0F.WIG EF /r | RVM | V/V | AVX | Bitwise XOR of xmm3/m128 and xmm2.

**NOTES:**

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical exclusive-OR (XOR) operation on the source operand (second operand) and the destination operand (first operand) and stores the result in the destination operand. The source operand can be an MMX technology register or a 64-bit memory location or it can be an XMM register or a 128-bit memory location. The destination operand can be an MMX technology register or an XMM register. Each bit of the result is 1 if the corresponding bits of the two operands are different; each bit is 0 if the corresponding bits of the operands are the same.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: Bits (VLMAX-1:128) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed. VEX.L must be 0, otherwise instructions will #UD.

**Operation**

PXOR (128-bit Legacy SSE version)
DEST ← DEST XOR SRC
DEST[VLMAX-1:128] (Unmodified)

VPXOR (VEX.128 encoded version)
DEST ← SRC1 XOR SRC2
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
PXOR: __m64 _mm_xor_si64 (__m64 m1, __m64 m2)
PXOR: __m128i _mm_xor_si128 ( __m128i a, __m128i b)

Flags Affected
None.

Numeric Exceptions
None.

Other Exceptions
See Exceptions Type 4; additionally
#UD If VEX.L = 1.
### RCL/RCR/ROL/ROR—Rotate

<table>
<thead>
<tr>
<th>Opcode**</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compartment/Legal Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0 /2</td>
<td>RCL r/m8, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 9 bits (CF, r/m8) left once.</td>
</tr>
<tr>
<td>REX + D0 /2</td>
<td>RCL r/m8*, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 9 bits (CF, r/m8) left once.</td>
</tr>
<tr>
<td>D2 /2</td>
<td>RCL r/m8, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 9 bits (CF, r/m8) left CL times.</td>
</tr>
<tr>
<td>REX + D2 /2</td>
<td>RCL r/m8*, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 9 bits (CF, r/m8) left CL times.</td>
</tr>
<tr>
<td>C0 /2 ib</td>
<td>RCL r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 9 bits (CF, r/m8) left imm8 times.</td>
</tr>
<tr>
<td>REX + C0 /2 ib</td>
<td>RCL r/m8*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 9 bits (CF, r/m8) left imm8 times.</td>
</tr>
<tr>
<td>D1 /2</td>
<td>RCL r/m16, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 17 bits (CF, r/m16) left once.</td>
</tr>
<tr>
<td>D3 /2</td>
<td>RCL r/m16, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 17 bits (CF, r/m16) left CL times.</td>
</tr>
<tr>
<td>C1 /2 ib</td>
<td>RCL r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 17 bits (CF, r/m16) left imm8 times.</td>
</tr>
<tr>
<td>D1 /2</td>
<td>RCL r/m32, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 33 bits (CF, r/m32) left once.</td>
</tr>
<tr>
<td>REX.W + D1 /2</td>
<td>RCL r/m64, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 65 bits (CF, r/m64) left once. Uses a 6 bit count.</td>
</tr>
<tr>
<td>D3 /2</td>
<td>RCL r/m32, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 33 bits (CF, r/m32) left CL times.</td>
</tr>
<tr>
<td>REX.W + D3 /2</td>
<td>RCL r/m64, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 65 bits (CF, r/m64) left CL times. Uses a 6 bit count.</td>
</tr>
<tr>
<td>C1 /2 ib</td>
<td>RCL r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 33 bits (CF, r/m32) left imm8 times.</td>
</tr>
<tr>
<td>REX.W + C1 /2 ib</td>
<td>RCL r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 65 bits (CF, r/m64) left imm8 times. Uses a 6 bit count.</td>
</tr>
<tr>
<td>D0 /3</td>
<td>RCR r/m8, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 9 bits (CF, r/m8) right once.</td>
</tr>
<tr>
<td>REX + D0 /3</td>
<td>RCR r/m8*, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 9 bits (CF, r/m8) right once.</td>
</tr>
<tr>
<td>Opcode**</td>
<td>Instruction</td>
<td>Op/En</td>
<td>64-Bit Mode</td>
<td>Comp/Leg Mode</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------------</td>
<td>-------</td>
<td>-------------</td>
<td>---------------</td>
<td>-------------</td>
</tr>
<tr>
<td>D2 /3</td>
<td>RCR r/m8, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 9 bits (CF, r/m8) right CL times.</td>
</tr>
<tr>
<td>REX + D2 /3</td>
<td>RCR r/m8*, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 9 bits (CF, r/m8) right CL times.</td>
</tr>
<tr>
<td>C0 /3 ib</td>
<td>RCR r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 9 bits (CF, r/m8) right imm8 times.</td>
</tr>
<tr>
<td>REX + C0 /3 ib</td>
<td>RCR r/m8*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 9 bits (CF, r/m8) right imm8 times.</td>
</tr>
<tr>
<td>D1 /3</td>
<td>RCR r/m16, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 17 bits (CF, r/m16) right once.</td>
</tr>
<tr>
<td>D3 /3</td>
<td>RCR r/m16, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 17 bits (CF, r/m16) right CL times.</td>
</tr>
<tr>
<td>C1 /3 ib</td>
<td>RCR r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 17 bits (CF, r/m16) right imm8 times.</td>
</tr>
<tr>
<td>D1 /3</td>
<td>RCR r/m32, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 33 bits (CF, r/m32) right once. Uses a 6 bit count.</td>
</tr>
<tr>
<td>REX.W + D1 /3</td>
<td>RCR r/m64, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 65 bits (CF, r/m64) right once. Uses a 6 bit count.</td>
</tr>
<tr>
<td>D3 /3</td>
<td>RCR r/m32, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 33 bits (CF, r/m32) right CL times.</td>
</tr>
<tr>
<td>REX.W + D3 /3</td>
<td>RCR r/m64, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 65 bits (CF, r/m64) right CL times. Uses a 6 bit count.</td>
</tr>
<tr>
<td>C1 /3 ib</td>
<td>RCR r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 33 bits (CF, r/m32) right imm8 times.</td>
</tr>
<tr>
<td>REX.W + C1 /3 ib</td>
<td>RCR r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 65 bits (CF, r/m64) right imm8 times. Uses a 6 bit count.</td>
</tr>
<tr>
<td>D0 /0</td>
<td>ROL r/m8, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 8 bits r/m8 left once.</td>
</tr>
<tr>
<td>REX + D0 /0</td>
<td>ROL r/m8*, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 8 bits r/m8 left once</td>
</tr>
<tr>
<td>D2 /0</td>
<td>ROL r/m8, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 8 bits r/m8 left CL times.</td>
</tr>
<tr>
<td>REX + D2 /0</td>
<td>ROL r/m8*, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 8 bits r/m8 left CL times.</td>
</tr>
<tr>
<td>C0 /0 ib</td>
<td>ROL r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 8 bits r/m8 left imm8 times.</td>
</tr>
<tr>
<td>Opcode**</td>
<td>Instruction</td>
<td>Op/En</td>
<td>64-Bit Mode</td>
<td>Compit/ Leg Mode</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------------</td>
<td>-------</td>
<td>-------------</td>
<td>-----------------</td>
<td>-------------</td>
</tr>
<tr>
<td>REX + C0 /0 ib</td>
<td>ROL r/m8*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 8 bits r/m8 left imm8 times.</td>
</tr>
<tr>
<td>D1 /0</td>
<td>ROL r/m16, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 16 bits r/m16 left once.</td>
</tr>
<tr>
<td>D3 /0</td>
<td>ROL r/m16, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 16 bits r/m16 left CL times.</td>
</tr>
<tr>
<td>C1 /0 ib</td>
<td>ROL r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 16 bits r/m16 left imm8 times.</td>
</tr>
<tr>
<td>D1 /0</td>
<td>ROL r/m32, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 32 bits r/m32 left once.</td>
</tr>
<tr>
<td>REX.W + D1 /0</td>
<td>ROL r/m64, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 64 bits r/m64 left once. Uses a 6 bit count.</td>
</tr>
<tr>
<td>D3 /0</td>
<td>ROL r/m32, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 32 bits r/m32 left CL times.</td>
</tr>
<tr>
<td>REX.W + D3 /0</td>
<td>ROL r/m64, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 64 bits r/m64 left CL times. Uses a 6 bit count.</td>
</tr>
<tr>
<td>C1 /0 ib</td>
<td>ROL r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 32 bits r/m32 left imm8 times.</td>
</tr>
<tr>
<td>C1 /0 ib</td>
<td>ROL r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 64 bits r/m64 left imm8 times. Uses a 6 bit count.</td>
</tr>
<tr>
<td>D0 /1</td>
<td>ROR r/m8, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 8 bits r/m8 right once.</td>
</tr>
<tr>
<td>REX + D0 /1</td>
<td>ROR r/m8*, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 8 bits r/m8 right once.</td>
</tr>
<tr>
<td>D2 /1</td>
<td>ROR r/m8, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 8 bits r/m8 right CL times.</td>
</tr>
<tr>
<td>REX + D2 /1</td>
<td>ROR r/m8*, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 8 bits r/m8 right CL times.</td>
</tr>
<tr>
<td>C0 /1 ib</td>
<td>ROR r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 8 bits r/m16 right imm8 times.</td>
</tr>
<tr>
<td>REX + C0 /1 ib</td>
<td>ROR r/m8*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Rotate 8 bits r/m16 right imm8 times.</td>
</tr>
<tr>
<td>D1 /1</td>
<td>ROR r/m16, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 16 bits r/m16 right once.</td>
</tr>
<tr>
<td>D3 /1</td>
<td>ROR r/m16, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Rotate 16 bits r/m16 right CL times.</td>
</tr>
</tbody>
</table>
Shifts (rotates) the bits of the first operand (destination operand) the number of bit positions specified in the second operand (count operand) and stores the result in the destination operand. The destination operand can be a register or a memory location; the count operand is an unsigned integer that can be an immediate or a value in the CL register. In legacy and compatibility mode, the processor restricts the count to a number between 0 and 31 by masking all the bits in the count operand except the 5 least-significant bits.

The rotate left (ROL) and rotate through carry left (RCL) instructions shift all the bits toward more-significant bit positions, except for the most-significant bit, which is rotated to the least-significant bit location. The rotate right (ROR) and rotate through carry right (RCR) instructions shift all the bits toward less-significant bit positions, except for the least-significant bit, which is rotated to the most-significant bit location.
carry right (RCR) instructions shift all the bits toward less significant bit positions, except for the least-significant bit, which is rotated to the most-significant bit location.

The RCL and RCR instructions include the CF flag in the rotation. The RCL instruction shifts the CF flag into the least-significant bit and shifts the most-significant bit into the CF flag. The RCR instruction shifts the CF flag into the most-significant bit and shifts the least-significant bit into the CF flag. For the ROL and ROR instructions, the original value of the CF flag is not a part of the result, but the CF flag receives a copy of the bit that was shifted from one end to the other.

The OF flag is defined only for the 1-bit rotates; it is undefined in all other cases (except RCL and RCR instructions only: a zero-bit rotate does nothing, that is affects no flags). For left rotates, the OF flag is set to the exclusive OR of the CF bit (after the rotate) and the most-significant bit of the result. For right rotates, the OF flag is set to the exclusive OR of the two most-significant bits of the result.

In 64-bit mode, using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Use of REX.W promotes the first operand to 64 bits and causes the count operand to become a 6-bit counter.

**IA-32 Architecture Compatibility**

The 8086 does not mask the rotation count. However, all other IA-32 processors (starting with the Intel 286 processor) do mask the rotation count to 5 bits, resulting in a maximum count of 31. This masking is done in all operating modes (including the virtual-8086 mode) to reduce the maximum execution time of the instructions.

**Operation**

(* RCL and RCR instructions *)
SIZE ← OperandSize;
CASE (determine count) OF
  SIZE ← 8: tempCOUNT ← (COUNT AND 1FH) MOD 9;
  SIZE ← 16: tempCOUNT ← (COUNT AND 1FH) MOD 17;
  SIZE ← 32: tempCOUNT ← COUNT AND 1FH;
  SIZE ← 64: tempCOUNT ← COUNT AND 3FH;
ESAC;

(* RCL instruction operation *)
WHILE (tempCOUNT ≠ 0)
  DO
    tempCF ← MSB(DEST);
    DEST ← (DEST * 2) + CF;
    CF ← tempCF;
    tempCOUNT ← tempCOUNT - 1;
  OD;
INSTRUCTION SET REFERENCE, M-Z

ELIHw;
IF COUNT = 1
    THEN OF ← MSB(DEST) XOR CF;
    ELSE OF is undefined;
FI;

(* RCR instruction operation *)
IF COUNT = 1
    THEN OF ← MSB(DEST) XOR CF;
    ELSE OF is undefined;
FI;
WHILE (tempCOUNT ≠ 0)
    DO
        tempCF ← LSB(SRC);
        DEST ← (DEST / 2) + (CF * 2^{SIZE});
        CF ← tempCF;
        tempCOUNT ← tempCOUNT - 1;
    OD;

(* ROL and ROR instructions *)
IF OperandSize = 64
    THEN COUNTMASK = 3FH;
    ELSE COUNTMASK = 1FH;
FI;

(* ROL instruction operation *)
tempCOUNT ← (COUNT & COUNTMASK) MOD SIZE
WHILE (tempCOUNT ≠ 0)
    DO
        tempCF ← MSB(DEST);
        DEST ← (DEST * 2) + tempCF;
        tempCOUNT ← tempCOUNT - 1;
    OD;
ELIHw;
CF ← LSB(DEST);
IF (COUNT & COUNTMASK) = 1
    THEN OF ← MSB(DEST) XOR CF;
    ELSE OF is undefined;
FI;

(* ROR instruction operation *)
tempCOUNT ← (COUNT & COUNTMASK) MOD SIZE
WHILE (tempCOUNT ≠ 0)
   DO
      tempCF ← LSB(SRC);
      DEST ← (DEST / 2) + (tempCF × 2\text{SIZE});
      tempCOUNT ← tempCOUNT - 1;
   OD;
   EIHW;
   CF ← MSB(DEST);
   IF (COUNT & COUNTMASK) = 1
      THEN OF ← MSB(DEST) XOR MSB − 1(DEST);
      ELSE OF is undefined;
   FI;

Flags Affected
The CF flag contains the value of the bit shifted into it. The OF flag is affected only for single-bit rotates (see "Description" above); it is undefined for multi-bit rotates. The SF, ZF, AF, and PF flags are not affected.

Protected Mode Exceptions
#GP(0) If the source operand is located in a non-writable segment.
   If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, M-Z

#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the source operand is located in a nonwritable segment.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
RCPPS—Compute Reciprocals of Packed Single-Precision Floating-Point Values

**Description**

Performs a SIMD computation of the approximate reciprocals of the four packed single-precision floating-point values in the source operand (second operand) stores the packed single-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 10-5 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for an illustration of a SIMD single-precision floating-point operation.

The relative error for this approximation is:

$$|\text{Relative Error}| \leq 1.5 \times 2^{-12}$$

The RCPPS instruction is not affected by the rounding control bits in the MXCSR register. When a source value is a 0.0, an ∞ of the sign of the source value is returned. A denormal source value is treated as a 0.0 (of the same sign). Tiny results are always flushed to 0.0, with the sign of the operand. (Input values greater than or equal to $1.1111111110100000000000000B+2^{125}$) are guaranteed to not produce tiny

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Opcode Table

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En 64/32 bit Mode Support CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 53 /r RCPPS xmm1, xmm2/m128</td>
<td>RM V/V SSE</td>
<td>Computes the approximate reciprocals of the packed single-precision floating-point values in xmm2/m128 and stores the results in xmm1.</td>
</tr>
<tr>
<td>VEX.128.0F:WIG 53 /r VRCPPS xmm1, xmm2/m128</td>
<td>RM V/V AVX</td>
<td>Computes the approximate reciprocals of packed single-precision values in xmm2/mem and stores the results in xmm1.</td>
</tr>
<tr>
<td>VEX.256.0F:WIG 53 /r VRCPPS ymm1, ymm2/m256</td>
<td>RM V/V AVX</td>
<td>Computes the approximate reciprocals of packed single-precision values in ymm2/mem and stores the results in ymm1.</td>
</tr>
</tbody>
</table>
results; input values less than or equal to $|1.0000000000011000000001B*2^{126}|$ are guaranteed to produce tiny results, which are in turn flushed to 0.0; and input values in between this range may or may not produce tiny results, depending on the implementation.) When a source value is an SNaN or QNaN, the SNaN is converted to a QNaN or the source QNaN is returned.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

**Operation**

**RCPPS (128-bit Legacy SSE version)**
- DEST[31:0] ← APPROXIMATE(1/SRC[31:0])
- DEST[63:32] ← APPROXIMATE(1/SRC[63:32])
- DEST[95:64] ← APPROXIMATE(1/SRC[95:64])
- DEST[127:96] ← APPROXIMATE(1/SRC[127:96])
- DEST[VLMAX-1:128] (Unmodified)

**VRCPSS (VEX.128 encoded version)**
- DEST[31:0] ← APPROXIMATE(1/SRC[31:0])
- DEST[63:32] ← APPROXIMATE(1/SRC[63:32])
- DEST[95:64] ← APPROXIMATE(1/SRC[95:64])
- DEST[127:96] ← APPROXIMATE(1/SRC[127:96])
- DEST[VLMAX-1:128] ← 0

**VRCPSS (VEX.256 encoded version)**
- DEST[31:0] ← APPROXIMATE(1/SRC[31:0])
- DEST[63:32] ← APPROXIMATE(1/SRC[63:32])
- DEST[95:64] ← APPROXIMATE(1/SRC[95:64])
- DEST[127:96] ← APPROXIMATE(1/SRC[127:96])
- DEST[159:128] ← APPROXIMATE(1/SRC[159:128])
- DEST[191:160] ← APPROXIMATE(1/SRC[191:160])
DEST[223:192] ← APPROXIMATE(1/SRC[223:192])
DEST[255:224] ← APPROXIMATE(1/SRC[255:224])

**Intel C/C++ Compiler Intrinsic Equivalent**
RCCPS: \_m128 \_mm\_rcp\_ps\(_m128 a\)
RCPPS: \_m256 \_mm256\_rcp\_ps\(_m256 a\);

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 4; additionally

#UD If VEX.vvvv ≠ 1111B.
RCPSS—Compute Reciprocal of Scalar Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 OF 53 /r</td>
<td>RCPSS xmm1, xmm2/m32</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Computes the approximate reciprocal of the scalar single-precision floating-point value in xmm2/m32 and stores the result in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.WIG 53 /r</td>
<td>VRCPPS xmm1, xmm2, xmm3/m32</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes the approximate reciprocal of the scalar single-precision floating-point value in xmm3/m32 and stores the result in xmm1. Also, upper single precision floating-point values (bits[127:32]) from xmm2 are copied to xmm1[127:32].</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg (w)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (w)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Computes of an approximate reciprocal of the low single-precision floating-point value in the source operand (second operand) and stores the single-precision floating-point result in the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The three high-order doublewords of the destination operand remain unchanged. See Figure 10-6 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for an illustration of a scalar single-precision floating-point operation.

The relative error for this approximation is:

\[|\text{Relative Error}| \leq 1.5 \times 2^{-12}\]

The RCPSS instruction is not affected by the rounding control bits in the MXCSR register. When a source value is a 0.0, an \( \infty \) of the sign of the source value is returned. A denormal source value is treated as a 0.0 (of the same sign). Tiny results
are always flushed to 0.0, with the sign of the operand. (Input values greater than or equal to \[1.1111111110100000000B \times 2^{125}\] are guaranteed to not produce tiny results; input values less than or equal to \[1.00000000001100000001B \times 2^{126}\] are guaranteed to produce tiny results, which are in turn flushed to 0.0; and input values in between this range may or may not produce tiny results, depending on the implementation.) When a source value is an SNaN or QNaN, the SNaN is converted to a QNaN or the source QNaN is returned.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

**RCPSS (128-bit Legacy SSE version)**

\[
\text{DEST}[31:0] \leftarrow \text{APPROXIMATE}(1/\text{SRC}[31:0])
\]

\[
\text{DEST}[\text{VLMAX}-1:32] \text{ (Unmodified)}
\]

**VRCPSS (VEX.128 encoded version)**

\[
\text{DEST}[31:0] \leftarrow \text{APPROXIMATE}(1/\text{SRC2}[31:0])
\]

\[
\text{DEST}[127:32] \leftarrow \text{SRC1}[127:32]
\]

\[
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

RCPSS: \_m128 \_mm_rcp_ss\(_\_m128\ a\)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 5.
RDFSBASE/RDGSBASE—Read FS/GS Segment Base

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Loads the general-purpose register indicated by the modR/M:r/m field with the FS or GS segment base address.

The destination operand may be either a 32-bit or a 64-bit general-purpose register. The REX.W prefix indicates the operand size is 64 bits. If no REX.W prefix is used, the operand size is 32 bits; the upper 32 bits of the source base address (for FS or GS) are ignored and upper 32 bits of the destination register are cleared.

This instruction is supported only in 64-bit mode.

### Operation

\[ \text{DEST} \leftarrow \text{FS/GS segment base address} \]

### Flags Affected

None

### C/C++ Compiler Intrinsic Equivalent

- RDFSBASE: \texttt{unsigned int \_readfsbase\_u32(void );}
- RDGSBASE: \texttt{unsigned \_int64 \_readgsbase\_u64(void );}
- RDFSBASE: \texttt{unsigned int \_readgsbase\_u32(void );}
- RDGSBASE: \texttt{unsigned \_int64 \_readgsbase\_u64(void );}
Protected Mode Exceptions
#UD The RDFSBASE and RDGSBASE instructions are not recognized in protected mode.

Real-Address Mode Exceptions
#UD The RDFSBASE and RDGSBASE instructions are not recognized in real-address mode.

Virtual-8086 Mode Exceptions
#UD The RDFSBASE and RDGSBASE instructions are not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
#UD The RDFSBASE and RDGSBASE instructions are not recognized in compatibility mode.

64-Bit Mode Exceptions
#UD If the LOCK prefix is used.
  If CR4.FSGSBASE[bit 16] = 0.
  If CPUID.07H:0H:EBX.FSGSBASE[bit 0] = 0.
RDMSR—Read from Model Specific Register

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 32</td>
<td>RDMSR</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Read MSR specified by ECX into EDX:EAX.</td>
</tr>
</tbody>
</table>

NOTES:
* See IA-32 Architecture Compatibility section below.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Reads the contents of a 64-bit model specific register (MSR) specified in the ECX register into registers EDX:EAX. (On processors that support the Intel 64 architecture, the high-order 32 bits of RCX are ignored.) The EDX register is loaded with the high-order 32 bits of the MSR and the EAX register is loaded with the low-order 32 bits. (On processors that support the Intel 64 architecture, the high-order 32 bits of each of RAX and RDX are cleared.) If fewer than 64 bits are implemented in the MSR being read, the values returned to EDX:EAX in unimplemented bit locations are undefined.

This instruction must be executed at privilege level 0 or in real-address mode; otherwise, a general protection exception #GP(0) will be generated. Specifying a reserved or unimplemented MSR address in ECX will also cause a general protection exception.

The MSRs control functions for testability, execution tracing, performance-monitoring, and machine check errors. Chapter 34, “Model-Specific Registers (MSRs),” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, lists all the MSRs that can be read with this instruction and their addresses. Note that each processor family has its own set of MSRs.

The CPUID instruction should be used to determine whether MSRs are supported (CPUID.01H:EDX[5] = 1) before using this instruction.

IA-32 Architecture Compatibility

The MSRs and the ability to read them with the RDMSR instruction were introduced into the IA-32 Architecture with the Pentium processor. Execution of this instruction by an IA-32 processor earlier than the Pentium processor results in an invalid opcode exception #UD.
See “Changes to Instruction Behavior in VMX Non-Root Operation” in Chapter 25 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, for more information about the behavior of this instruction in VMX non-root operation.

Operation

EDX:EAX ← MSR[ECX];

Flags Affected

None.

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0.
If the value in ECX specifies a reserved or unimplemented MSR address.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If the value in ECX specifies a reserved or unimplemented MSR address.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) The RDMSR instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the current privilege level is not 0.
If the value in ECX or RCX specifies a reserved or unimplemented MSR address.

#UD If the LOCK prefix is used.
RDPMC—Read Performance-Monitoring Counters

### Instruction Encoding

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 33</td>
<td>RDPMC</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Read performance-monitoring counter specified by ECX into EDX:EAX.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

The EAX register is loaded with the low-order 32 bits. The EDX register is loaded with the supported high-order bits of the counter. The number of high-order bits loaded into EDX is implementation specific on processors that do not support architectural performance monitoring. The width of fixed-function and general-purpose performance counters on processors supporting architectural performance monitoring are reported by CPUID 0AH leaf. See below for the treatment of the EDX register for “fast” reads.

The ECX register selects one of two types of performance counters, specifies the index relative to the base of each counter type, and selects “fast” read mode if supported. The two counter types are:

- General-purpose or special-purpose performance counters: The number of general-purpose counters is model specific if the processor does not support architectural performance monitoring, see Chapter 30 of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*. Special-purpose counters are available only in selected processor members, see Section 30.13, 30.14 of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*. This counter type is selected if ECX[30] is clear.

- Fixed-function performance counter. The number fixed-function performance counters is enumerated by CPUID 0AH leaf. See Chapter 30 of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*. This counter type is selected if ECX[30] is set.

ECX[29:0] specifies the index. The width of general-purpose performance counters are 40-bits for processors that do not support architectural performance monitoring counters. The width of special-purpose performance counters are implementation specific. The width of fixed-function performance counters and general-purpose performance counters on processor supporting architectural performance monitoring are reported by CPUID 0AH leaf.
Table 4-15 lists valid indices of the general-purpose and special-purpose performance counters according to the derived DisplayFamily_DisplayModel values of CPUID encoding for each processor family (see CPUID instruction in Chapter 3, “Instruction Set Reference, A-L” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A).

**Table 4-15. Valid General and Special Purpose Performance Counter Index Range for RDPMC**

<table>
<thead>
<tr>
<th>Processor Family</th>
<th>DisplayFamily_Display Model/ Other Signatures</th>
<th>Valid PMC Index Range</th>
<th>General-purpose Counters</th>
</tr>
</thead>
<tbody>
<tr>
<td>P6</td>
<td>06H_01H, 06H_03H, 06H_05H, 06H_06H, 06H_07H, 06H_08H, 06H_0AH, 06H_0BH</td>
<td>0, 1</td>
<td>0, 1</td>
</tr>
<tr>
<td>Pentium® 4, Intel® Xeon processors</td>
<td>0FH_00H, 0FH_01H, 0FH_02H (0FH_03H, 0FH_04H, 0FH_06H) and (L3 is absent)</td>
<td>≥ 0 and ≤ 17</td>
<td>≥ 0 and ≤ 17</td>
</tr>
<tr>
<td>Pentium 4, Intel Xeon processors</td>
<td>06H_09H, 06H_0DH</td>
<td>≥ 0 and ≤ 25</td>
<td>≥ 0 and ≤ 17</td>
</tr>
<tr>
<td>Pentium M processors</td>
<td>06H_0EH</td>
<td>0, 1</td>
<td>0, 1</td>
</tr>
<tr>
<td>64-bit Intel Xeon processors with L3</td>
<td>06H_0FH</td>
<td>0, 1</td>
<td>0, 1</td>
</tr>
<tr>
<td>Intel® Core™ Solo and Intel® Core™ Duo processors, Dual-core Intel® Xeon® processor LV</td>
<td>(0FH_06H) and (L3 is present)</td>
<td>≥ 0 and ≤ 25</td>
<td>≥ 0 and ≤ 17</td>
</tr>
<tr>
<td>Intel® Core™2 Duo processor, Intel Xeon processor 3000, 5100, 5300, 7300 Series - general-purpose PMC</td>
<td>06H_17H</td>
<td>0, 1</td>
<td>0, 1</td>
</tr>
<tr>
<td>Intel Xeon processors 7100 series with L3</td>
<td>(06H_1DH)</td>
<td>≥ 0 and ≤ 9</td>
<td>0, 1</td>
</tr>
<tr>
<td>Intel® Core™2 Duo processor family, Intel Xeon processor family - general-purpose PMC</td>
<td>06H_1CH</td>
<td>0, 1</td>
<td>0, 1</td>
</tr>
<tr>
<td>Intel Xeon processors 7400 series</td>
<td>06H_1AH, 06H_1EH, 06H_1FH, 06H_2EH</td>
<td>0-3</td>
<td>0, 1, 2, 3</td>
</tr>
<tr>
<td>Intel® Atom™ processor family</td>
<td>06H_1CH</td>
<td>0, 1</td>
<td>0, 1</td>
</tr>
<tr>
<td>Intel® Core™i7 processor, Intel Xeon processors 5500 series</td>
<td>06H_1AH, 06H_1EH, 06H_1FH, 06H_2EH</td>
<td>0-3</td>
<td>0, 1, 2, 3</td>
</tr>
</tbody>
</table>

The Pentium 4 and Intel Xeon processors also support "fast" (32-bit) and “slow” (40-bit) reads on the first 18 performance counters. Selected this option using
ECX[31]. If bit 31 is set, RDPMC reads only the low 32 bits of the selected performance counter. If bit 31 is clear, all 40 bits are read. A 32-bit result is returned in EAX and EDX is set to 0. A 32-bit read executes faster on Pentium 4 processors and Intel Xeon processors than a full 40-bit read.

On 64-bit Intel Xeon processors with L3, performance counters with indices 18-25 are 32-bit counters. EDX is cleared after executing RDPMC for these counters. On Intel Xeon processor 7100 series with L3, performance counters with indices 18-25 are also 32-bit counters.

In Intel Core 2 processor family, Intel Xeon processor 3000, 5100, 5300 and 7400 series, the fixed-function performance counters are 40-bits wide; they can be accessed by RDMPC with ECX between from 4000_0000H and 4000_0002H.

On Intel Xeon processor 7400 series, there are eight 32-bit special-purpose counters addressable with indices 2-9, ECX[30]=0.

When in protected or virtual 8086 mode, the performance-monitoring counters enabled (PCE) flag in register CR4 restricts the use of the RDPMC instruction as follows. When the PCE flag is set, the RDPMC instruction can be executed at any privilege level; when the flag is clear, the instruction can only be executed at privilege level 0. (When in real-address mode, the RDPMC instruction is always enabled.)

The performance-monitoring counters can also be read with the RDMSR instruction, when executing at privilege level 0.

The performance-monitoring counters are event counters that can be programmed to count events such as the number of instructions decoded, number of interrupts received, or number of cache loads. Chapter 19, “Performance Monitoring Events,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B, lists the events that can be counted for various processors in the Intel 64 and IA-32 architecture families.

The RDPMC instruction is not a serializing instruction; that is, it does not imply that all the events caused by the preceding instructions have been completed or that events caused by subsequent instructions have not begun. If an exact event count is desired, software must insert a serializing instruction (such as the CPUID instruction) before and/or after the RDPMC instruction.

In the Pentium 4 and Intel Xeon processors, performing back-to-back fast reads are not guaranteed to be monotonic. To guarantee monotonicity on back-to-back reads, a serializing instruction must be placed between the two RDPMC instructions.

The RDPMC instruction can execute in 16-bit addressing mode or virtual-8086 mode; however, the full contents of the ECX register are used to select the counter, and the event count is stored in the full EAX and EDX registers. The RDPMC instruction was introduced into the IA-32 Architecture in the Pentium Pro processor and the Pentium processor with MMX technology. The earlier Pentium processors have performance-monitoring counters, but they must be read with the RDMSR instruction.
Operation

(* Intel Core i7 processor family and Intel Xeon processor 3400, 5500 series*)

Most significant counter bit (MSCB) = 47

IF ((CR4.PCE = 1) or (CPL = 0) or (CR0.PE = 0))
   THEN IF (ECX[30] = 1 and ECX[29:0] in valid fixed-counter range)
      EAX ← IA32_FIXED_CTR(ECX)[30:0];
      EDX ← IA32_FIXED_CTR(ECX)[MSCB:32];
   ELSE IF (ECX[30] = 0 and ECX[29:0] in valid general-purpose counter range)
      EAX ← PMC(ECX[30:0])[31:0];
      EDX ← PMC(ECX[30:0])[MSCB:32];
   ELSE (* ECX is not valid or CR4.PCE is 0 and CPL is 1, 2, or 3 and CR0.PE is 1 *)
      #GP(0);
   FI;

(* Intel Core 2 Duo processor family and Intel Xeon processor 3000, 5100, 5300, 7400 series*)

Most significant counter bit (MSCB) = 39

IF ((CR4.PCE = 1) or (CPL = 0) or (CR0.PE = 0))
   THEN IF (ECX[30] = 1 and ECX[29:0] in valid fixed-counter range)
      EAX ← IA32_FIXED_CTR(ECX)[30:0];
      EDX ← IA32_FIXED_CTR(ECX)[MSCB:32];
   ELSE IF (ECX[30] = 0 and ECX[29:0] in valid general-purpose counter range)
      EAX ← PMC(ECX[30:0])[31:0];
      EDX ← PMC(ECX[30:0])[MSCB:32];
   ELSE IF (ECX[30] = 0 and ECX[29:0] in valid special-purpose counter range)
      EAX ← PMC(ECX[30:0])[31:0]; (* 32-bit read *)
   ELSE (* ECX is not valid or CR4.PCE is 0 and CPL is 1, 2, or 3 and CR0.PE is 1 *)
      #GP(0);
   FI;

(* P6 family processors and Pentium processor with MMX technology *)

IF (ECX = 0 or 1) and ((CR4.PCE = 1) or (CPL = 0) or (CR0.PE = 0))
   THEN
      EAX ← PMC(ECX)[31:0];
      EDX ← PMC(ECX)[39:32];
   ELSE (* ECX is not 0 or 1 or CR4.PCE is 0 and CPL is 1, 2, or 3 and CR0.PE is 1 *)
      #GP(0);
   FI;

(* Processors with CPUID family 15 *)

RDPMC—Read Performance-Monitoring Counters
INSTRUCTION SET REFERENCE, M-Z

IF ((CR4.PCE = 1) or (CPL = 0) or (CR0.PE = 0))
  THEN IF (ECX[30:0] = 0:17)
    THEN IF ECX[31] = 0
      THEN
        EAX ← PMC(ECX[30:0])[31:0]; (* 40-bit read *)
        EDX ← PMC(ECX[30:0])[39:32];
      ELSE (* ECX[31] = 1 *)
        THEN
          EAX ← PMC(ECX[30:0])[31:0]; (* 32-bit read *)
          EDX ← 0;
        FI;
    ELSE IF (*64-bit Intel Xeon processor with L3 *)
      THEN IF (ECX[30:0] = 18:25)
        EAX ← PMC(ECX[30:0])[31:0]; (* 32-bit read *)
        EDX ← 0;
      FI;
    ELSE IF (*Intel Xeon processor 7100 series with L3 *)
      THEN IF (ECX[30:0] = 18:25)
        EAX ← PMC(ECX[30:0])[31:0]; (* 32-bit read *)
        EDX ← 0;
      FI;
    ELSE (* Invalid PMC index in ECX[30:0], see Table 4-18. *)
      GP(0);
    FI;
  ELSE (* CR4.PCE = 0 and (CPL = 1, 2, or 3) and CR0.PE = 1 *)
    #GP(0);
  FI;
Flags Affected
None.

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0 and the PCE flag in the CR4 register is clear.
  If an invalid performance counter index is specified (see Table 4-15).
  (Pentium 4 and Intel Xeon processors) If the value in ECX[30:0] is not within the valid range.

#UD If the LOCK prefix is used.
Real-Address Mode Exceptions

#G P If an invalid performance counter index is specified (see Table 4-15).
(Pentium 4 and Intel Xeon processors) If the value in ECX[30:0] is not within the valid range.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If the PCE flag in the CR4 register is clear.
If an invalid performance counter index is specified (see Table 4-15).
(Pentium 4 and Intel Xeon processors) If the value in ECX[30:0] is not within the valid range.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the current privilege level is not 0 and the PCE flag in the CR4 register is clear.
If an invalid performance counter index is specified in ECX[30:0] (see Table 4-15).

#UD If the LOCK prefix is used.
RDRAND—Read Random Number

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Loads a hardware generated random value and store it in the destination register. The size of the random value is determined by the destination register size and operating mode. The Carry Flag indicates whether a random value is available at the time the instruction is executed. CF=1 indicates that the data in the destination is valid. Otherwise CF=0 and the data in the destination operand will be returned as zeros for the specified width. All other flags are forced to 0 in either situation. Software must check the state of CF=1 for determining if a valid random value has been returned, otherwise it is expected to loop and retry execution of RDRAND (see Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, Section 7.3.17, "Random Number Generator Instruction").

This instruction is available at all privilege levels.

In 64-bit mode, the instruction's default operation size is 32 bits. Using a REX prefix in the form of REX.B permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bit operands. See the summary chart at the beginning of this section for encoding data and limits.

Operation

IF HW_RND_GEN.ready = 1
THEN
    CASE of
        osize is 64: DEST[63:0] ← HW_RND_GEN.data;
        osize is 32: DEST[31:0] ← HW_RND_GEN.data;
INSTRUCTION SET REFERENCE, M-Z

RDRAND—Read Random Number

```assembly
osize is 16: DEST[15:0] ← HW_RND_GEN.data;
ESAC
CF ← 1;
ELSE
    CASE of
        osize is 64: DEST[63:0] ← 0;
        osize is 32: DEST[31:0] ← 0;
        osize is 16: DEST[15:0] ← 0;
    ESAC
    CF ← 0;
FI
OF, SF, ZF, AF, PF ← 0;

Flags Affected
All flags are affected.

Intel C/C++ Compiler Intrinsic Equivalent
RDRAND:    int _rdrand16_step( unsigned short * );
RDRAND:    int _rdrand32_step( unsigned int * );
RDRAND:    int _rdrand64_step( unsigned __int64 * );

Protected Mode Exceptions
#UD If the LOCK prefix is used.
    If the F2H or F3H prefix is used.
    If CPUID.01H:ECX.RDRAND[bit 30] = 0.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
RDTSC—Read Time-Stamp Counter

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 31</td>
<td>RDTSC</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Read time-stamp counter into EDX:EAX.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Loads the current value of the processor’s time-stamp counter (a 64-bit MSR) into the EDX:EAX registers. The EDX register is loaded with the high-order 32 bits of the MSR and the EAX register is loaded with the low-order 32 bits. (On processors that support the Intel 64 architecture, the high-order 32 bits of each of RAX and RDX are cleared.)

The processor monotonically increments the time-stamp counter MSR every clock cycle and resets it to 0 whenever the processor is reset. See “Time Stamp Counter” in Chapter 17 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B, for specific details of the time stamp counter behavior.

When in protected or virtual 8086 mode, the time stamp disable (TSD) flag in register CR4 restricts the use of the RDTSC instruction as follows. When the TSD flag is clear, the RDTSC instruction can be executed at any privilege level; when the flag is set, the instruction can only be executed at privilege level 0. (When in real-address mode, the RDTSC instruction is always enabled.)

The time-stamp counter can also be read with the RDMSR instruction, when executing at privilege level 0.

The RDTSC instruction is not a serializing instruction. It does not necessarily wait until all previous instructions have been executed before reading the counter. Similarly, subsequent instructions may begin execution before the read operation is performed. If software requires RDTSC to be executed only after all previous instructions have completed locally, it can either use RDTSCP (if the processor supports that instruction) or execute the sequence LFENCE;RDTSC.

This instruction was introduced by the Pentium processor.

See "Changes to Instruction Behavior in VMX Non-Root Operation” in Chapter 25 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, for more information about the behavior of this instruction in VMX non-root operation.

Operation

IF (CR4.TSD = 0) or (CPL = 0) or (CR0.PE = 0)
THEN EDX:EAX ← TimeStampCounter;
ELSE (* CR4.TSD = 1 and (CPL = 1, 2, or 3) and CR0.PE = 1 *)
    #GP(0);
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the TSD flag in register CR4 is set and the CPL is greater than 0.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If the TSD flag in register CR4 is set.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
RDTSCP—Read Time-Stamp Counter and Processor ID

Description

Loads the current value of the processor’s time-stamp counter (a 64-bit MSR) into the EDX:EAX registers and also loads the IA32_TSC_AUX MSR (address C000_0103H) into the ECX register. The EDX register is loaded with the high-order 32 bits of the IA32_TSC MSR; the EAX register is loaded with the low-order 32 bits of the IA32_TSC MSR; and the ECX register is loaded with the low-order 32-bits of IA32_TSC_AUX MSR. On processors that support the Intel 64 architecture, the high-order 32 bits of each of RAX, RDX, and RCX are cleared.

The processor monotonically increments the time-stamp counter MSR every clock cycle and resets it to 0 whenever the processor is reset. See “Time Stamp Counter” in Chapter 17 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B, for specific details of the time stamp counter behavior.

When in protected or virtual 8086 mode, the time stamp disable (TSD) flag in register CR4 restricts the use of the RDTSCP instruction as follows. When the TSD flag is clear, the RDTSCP instruction can be executed at any privilege level; when the flag is set, the instruction can only be executed at privilege level 0. (When in real-address mode, the RDTSCP instruction is always enabled.)

The RDTSCP instruction waits until all previous instructions have been executed before reading the counter. However, subsequent instructions may begin execution before the read operation is performed.

The presence of the RDTSCP instruction is indicated by CPUID leaf 80000001H, EDX bit 27. If the bit is set to 1 then RDTSCP is present on the processor.

See “Changes to Instruction Behavior in VMX Non-Root Operation” in Chapter 25 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, for more information about the behavior of this instruction in VMX non-root operation.

Operation

IF (CR4.TSD = 0) or (CPL = 0) or (CR0.PE = 0)
THEN
    EDX:EAX ← TimeStampCounter;
    ECX ← IA32_TSC_AUX[31:0];
ELSE (* CR4.TSD = 1 and (CPL = 1, 2, or 3) and CR0.PE = 1 *)
    #GP(0);
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the TSD flag in register CR4 is set and the CPL is greater than 0.
#UD If the LOCK prefix is used.
    If CPUID.80000001H:EDX.RDTSCP[bit 27] = 0.

Real-Address Mode Exceptions
#UD If the LOCK prefix is used.
    If CPUID.80000001H:EDX.RDTSCP[bit 27] = 0.

Virtual-8086 Mode Exceptions
#GP(0) If the TSD flag in register CR4 is set.
#UD If the LOCK prefix is used.
    If CPUID.80000001H:EDX.RDTSCP[bit 27] = 0.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
## REP/REPE/REPZ/REPNE/REPNZ—Repeat String Operation Prefix

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 6C</td>
<td>REP INS m8, DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input (E)CX bytes from port DX into ES:[(E)DI].</td>
</tr>
<tr>
<td>F3 6C</td>
<td>REP INS m8, DX</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Input RCX bytes from port DX into [RDI].</td>
</tr>
<tr>
<td>F3 6D</td>
<td>REP INS m16, DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input (E)CX words from port DX into ES:[(E)DI].</td>
</tr>
<tr>
<td>F3 6D</td>
<td>REP INS m32, DX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Input (E)CX doublewords from port DX into ES:[(E)DI].</td>
</tr>
<tr>
<td>F3 6D</td>
<td>REP INS r/m32, DX</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Input RCX default size from port DX into [RDI].</td>
</tr>
<tr>
<td>F3 A4</td>
<td>REP MOVS m8, m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Move (E)CX bytes from DS:[(E)SI] to ES:[(E)DI].</td>
</tr>
<tr>
<td>F3 REX.W A4</td>
<td>REP MOVS m8, m8</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move RCX bytes from [RSI] to [RDI].</td>
</tr>
<tr>
<td>F3 A5</td>
<td>REP MOVS m16, m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Move (E)CX words from DS:[(E)SI] to ES:[(E)DI].</td>
</tr>
<tr>
<td>F3 A5</td>
<td>REP MOVS m32, m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Move (E)CX doublewords from DS:[(E)SI] to ES:[(E)DI].</td>
</tr>
<tr>
<td>F3 REX.W A5</td>
<td>REP MOVS m64, m64</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Move RCX quadwords from [RSI] to [RDI].</td>
</tr>
<tr>
<td>F3 6E</td>
<td>REP OUTS DX, r/m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output (E)CX bytes from DS:[(E)SI] to port DX.</td>
</tr>
<tr>
<td>F3 REX.W 6E</td>
<td>REP OUTS DX, r/m8*</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Output RCX bytes from [RSI] to port DX.</td>
</tr>
<tr>
<td>F3 6F</td>
<td>REP OUTS DX, r/m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output (E)CX words from DS:[(E)SI] to port DX.</td>
</tr>
<tr>
<td>F3 6F</td>
<td>REP OUTS DX, r/m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Output (E)CX doublewords from DS:[(E)SI] to port DX.</td>
</tr>
<tr>
<td>F3 REX.W 6F</td>
<td>REP OUTS DX, r/m32</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Output RCX default size from [RSI] to port DX.</td>
</tr>
<tr>
<td>F3 AC</td>
<td>REP LODS AL</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Load (E)CX bytes from DS:[(E)SI] to AL.</td>
</tr>
<tr>
<td>F3 REX.W AC</td>
<td>REP LODS AL</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load RCX bytes from [RSI] to AL.</td>
</tr>
<tr>
<td>F3 AD</td>
<td>REP LODS AX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Load (E)CX words from DS:[(E)SI] to AX.</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>Op/En</td>
<td>64-Bit Mode</td>
<td>Compat/ Leg Mode</td>
<td>Description</td>
</tr>
<tr>
<td>-------</td>
<td>---------------------</td>
<td>-------</td>
<td>-------------</td>
<td>-----------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>F3 AD</td>
<td>REP LODS EAX</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Load (E)CX doublewords from DS:((ESI) to EAX.</td>
</tr>
<tr>
<td>F3 REX.W AD</td>
<td>REP LODS RAX</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Load RCX quadwords from [RSI] to RAX.</td>
</tr>
<tr>
<td>F3 AA</td>
<td>REP STOS m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Fill (E)CX bytes at ES:((EDI) with AL.</td>
</tr>
<tr>
<td>F3 REX.W AA</td>
<td>REP STOS m8</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Fill RCX bytes at [RDI] with AL.</td>
</tr>
<tr>
<td>F3 AB</td>
<td>REP STOS m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Fill (E)CX words at ES:((EDI) with AX.</td>
</tr>
<tr>
<td>F3 AB</td>
<td>REP STOS m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Fill (E)CX doublewords at ES:((EDI) with EAX.</td>
</tr>
<tr>
<td>F3 REX.W AB</td>
<td>REP STOS m64</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Fill RCX quadwords at [RDI] with RAX.</td>
</tr>
<tr>
<td>F3 A6</td>
<td>REPE CMPS m8, m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Find nonmatching bytes in ES:((EDI) and DS:((ESI).</td>
</tr>
<tr>
<td>F3 REX.W A6</td>
<td>REPE CMPS m8, m8</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Find non-matching bytes in [RDI] and [RSI].</td>
</tr>
<tr>
<td>F3 A7</td>
<td>REPE CMPS m16, m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Find nonmatching words in ES:((EDI) and DS:((ESI).</td>
</tr>
<tr>
<td>F3 A7</td>
<td>REPE CMPS m32, m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Find nonmatching doublewords in ES:((EDI) and DS:((ESI).</td>
</tr>
<tr>
<td>F3 REX.W A7</td>
<td>REPE CMPS m64, m64</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Find non-matching quadwords in [RDI] and [RSI].</td>
</tr>
<tr>
<td>F3 AE</td>
<td>REPE SCAS m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Find non-AL byte starting at ES:((EDI).</td>
</tr>
<tr>
<td>F3 REX.W AE</td>
<td>REPE SCAS m8</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Find non-AL byte starting at [RDI].</td>
</tr>
<tr>
<td>F3 AF</td>
<td>REPE SCAS m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Find non-AX word starting at ES:((EDI).</td>
</tr>
<tr>
<td>F3 AF</td>
<td>REPE SCAS m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Find non-EAX doubleword starting at ES:((EDI).</td>
</tr>
<tr>
<td>F3 REX.W AF</td>
<td>REPE SCAS m64</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Find non-RAX quadword starting at [RDI].</td>
</tr>
<tr>
<td>F2 A6</td>
<td>REPNE CMPS m8, m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Find matching bytes in ES:((EDI) and DS:((ESI).</td>
</tr>
</tbody>
</table>
Replicates a string operation the number of times specified in the count register or until the indicated condition of the ZF flag is no longer met. The REP (repeat), REPE (repeat while equal), REPNE (repeat while not equal), REPZ (repeat while zero), and REPNZ (repeat while not zero) mnemonics are prefixes that can be added to one of the string instructions. The REP prefix can be added to the INS, OUTS, MOVVS, MOVDS, and STOS instructions, and the REPE, REPNE, REPZ, and REPNZ prefixes can be added to the CMPS and SCAS instructions. (The REPZ and REPNZ prefixes are synonymous forms of the REPE and REPNE prefixes, respectively.) The behavior of the REP prefix is undefined when used with non-string instructions.

The REP prefixes apply only to one string instruction at a time. To repeat a block of instructions, use the LOOP instruction or another looping construct. All of these repeat prefixes cause the associated instruction to be repeated until the count in register is decremented to 0. See Table 4-16.

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th><strong>Op/En</strong></th>
<th><strong>Operand 1</strong></th>
<th><strong>Operand 2</strong></th>
<th><strong>Operand 3</strong></th>
<th><strong>Operand 4</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Repeats a string instruction the number of times specified in the count register or until the indicated condition of the ZF flag is no longer met. The REP (repeat), REPE (repeat while equal), REPNE (repeat while not equal), REPZ (repeat while zero), and REPNZ (repeat while not zero) mnemonics are prefixes that can be added to one of the string instructions. The REP prefix can be added to the INS, OUTS, MOVVS, MOVDS, and STOS instructions, and the REPE, REPNE, REPZ, and REPNZ prefixes can be added to the CMPS and SCAS instructions. (The REPZ and REPNZ prefixes are synonymous forms of the REPE and REPNE prefixes, respectively.) The behavior of the REP prefix is undefined when used with non-string instructions.

The REP prefixes apply only to one string instruction at a time. To repeat a block of instructions, use the LOOP instruction or another looping construct. All of these repeat prefixes cause the associated instruction to be repeated until the count in register is decremented to 0. See Table 4-16.
The REPE, REPNE, REPZ, and REPNZ prefixes also check the state of the ZF flag after each iteration and terminate the repeat loop if the ZF flag is not in the specified state. When both termination conditions are tested, the cause of a repeat termination can be determined either by testing the count register with a JECXZ instruction or by testing the ZF flag (with a JZ, JNZ, or JNE instruction).

When the REPE/REPZ and REPNE/REPNZ prefixes are used, the ZF flag does not require initialization because both the CMPS and SCAS instructions affect the ZF flag according to the results of the comparisons they make.

A repeating string operation can be suspended by an exception or interrupt. When this happens, the state of the registers is preserved to allow the string operation to be resumed upon a return from the exception or interrupt handler. The source and destination registers point to the next string elements to be operated on, the EIP register points to the string instruction, and the ECX register has the value it held following the last successful iteration of the instruction. This mechanism allows long string operations to proceed without affecting the interrupt response time of the system.

When a fault occurs during the execution of a CMPS or SCAS instruction that is prefixed with REPE or REPNE, the EFLAGS value is restored to the state prior to the execution of the instruction. Since the SCAS and CMPS instructions do not use EFLAGS as an input, the processor can resume the instruction after the page fault handler.

Use the REP INS and REP OUTS instructions with caution. Not all I/O ports can handle the rate at which these instructions execute. Note that a REP STOS instruction is the fastest way to initialize a large block of memory.

In 64-bit mode, the operand size of the count register is associated with the address size attribute. Thus the default count register is RCX; REX.W has no effect on the address size and the count register. In 64-bit mode, if 67H is used to override address size attribute, the count register is ECX and any implicit source/destination operand will use the corresponding 32-bit index register. See the summary chart at the beginning of this section for encoding data and limits.

### Table 4-16. Repeat Prefixes

<table>
<thead>
<tr>
<th>Repeat Prefix</th>
<th>Termination Condition 1</th>
<th>Termination Condition 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>REP</td>
<td>RCX or (E)CX = 0</td>
<td>None</td>
</tr>
<tr>
<td>REPE/REPZ</td>
<td>RCX or (E)CX = 0</td>
<td>ZF = 0</td>
</tr>
<tr>
<td>REPNE/REPNZ</td>
<td>RCX or (E)CX = 0</td>
<td>ZF = 1</td>
</tr>
</tbody>
</table>

NOTES:

* Count register is CX, ECX or RCX by default, depending on attributes of the operating modes.
**Operation**

IF AddressSize = 16  
THEN  
Use CX for CountReg;  
Implicit Source/Dest operand for memory use of SI/DI;  
ELSE IF AddressSize = 64  
THEN Use RCX for CountReg;  
Implicit Source/Dest operand for memory use of RSI/RDI;  
ELSE  
Use ECX for CountReg;  
Implicit Source/Dest operand for memory use of ESI/EDI;  
FI;  
WHILE CountReg ≠ 0  
DO  
Service pending interrupts (if any);  
Execute associated string instruction;  
CountReg ← (CountReg – 1);  
IF CountReg = 0  
THEN exit WHILE loop; FI;  
IF (Repeat prefix is REPZ or REPE) and (ZF = 0)  
or (Repeat prefix is REPNZ or REPNE) and (ZF = 1)  
THEN exit WHILE loop; Fi;  
OD;

**Flags Affected**

None; however, the CMPS and SCAS instructions do set the status flags in the EFLAGS register.

**Exceptions (All Operating Modes)**

Exceptions may be generated by an instruction associated with the prefix.

**64-Bit Mode Exceptions**

#GP(0)  
If the memory address is in a non-canonical form.
RET—Return from Procedure

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>I</td>
<td>imm16</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Transfers program control to a return address located on the top of the stack. The address is usually placed on the stack by a CALL instruction, and the return is made to the instruction that follows the CALL instruction.

The optional source operand specifies the number of stack bytes to be released after the return address is popped; the default is none. This operand can be used to release parameters from the stack that were passed to the called procedure and are no longer needed. It must be used when the CALL instruction used to switch to a new procedure uses a call gate with a non-zero word count to access the new procedure. Here, the source operand for the RET instruction must specify the same number of bytes as is specified in the word count field of the call gate.

The RET instruction can be used to execute three different types of returns:

- **Near return** — A return to a calling procedure within the current code segment (the segment currently pointed to by the CS register), sometimes referred to as an intrasegment return.
- **Far return** — A return to a calling procedure located in a different segment than the current code segment, sometimes referred to as an intersegment return.
- **Inter-privilege-level far return** — A far return to a different privilege level than that of the currently executing program or procedure.
The inter-privilege-level return type can only be executed in protected mode. See the section titled “Calling Procedures Using Call and RET” in Chapter 6 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for detailed information on near, far, and inter-privilege-level returns.

When executing a near return, the processor pops the return instruction pointer (offset) from the top of the stack into the EIP register and begins program execution at the new instruction pointer. The CS register is unchanged.

When executing a far return, the processor pops the return instruction pointer from the top of the stack into the EIP register, then pops the segment selector from the top of the stack into the CS register. The processor then begins program execution in the new code segment at the new instruction pointer.

The mechanics of an inter-privilege-level far return are similar to an intersegment return, except that the processor examines the privilege levels and access rights of the code and stack segments being returned to determine if the control transfer is allowed to be made. The DS, ES, FS, and GS segment registers are cleared by the RET instruction during an inter-privilege-level return if they refer to segments that are not allowed to be accessed at the new privilege level. Since a stack switch also occurs on an inter-privilege level return, the ESP and SS registers are loaded from the stack.

If parameters are passed to the called procedure during an inter-privilege level call, the optional source operand must be used with the RET instruction to release the parameters on the return. Here, the parameters are released both from the called procedure’s stack and the calling procedure’s stack (that is, the stack being returned to).

In 64-bit mode, the default operation size of this instruction is the stack-address size, i.e. 64 bits.

**Operation**

(* Near return *)

IF instruction = near return

THEN;

IF OperandSize = 32

THEN

IF top 4 bytes of stack not within stack limits

THEN #SS(0); Fl;

EIP ← Pop();

ELSE

IF OperandSize = 64

THEN

IF top 8 bytes of stack not within stack limits

THEN #SS(0); Fl;

RIP ← Pop();

ELSE (* OperandSize = 16 *)
IF top 2 bytes of stack not within stack limits
THEN #SS(0); FI;
tempEIP ← Pop();
tempEIP ← tempEIP AND 0000FFFFH;
IF tempEIP not within code segment limits
THEN #GP(0); FI;
EIP ← tempEIP;
FI;
FI;
IF instruction has immediate operand
THEN (* Release parameters from stack *)
IF StackAddressSize = 32
THEN
    ESP ← ESP + SRC;
ELSE
    IF StackAddressSize = 64
    THEN
        RSP ← RSP + SRC;
    ELSE (* StackAddressSize = 16 *)
        SP ← SP + SRC;
    FI;
    FI;
FI;
FI;

(* Real-address mode or virtual-8086 mode *)
IF ((PE = 0) or (PE = 1 AND VM = 1)) and instruction = far return
THEN
IF OperandSize = 32
THEN
    IF top 8 bytes of stack not within stack limits
    THEN #SS(0); FI;
    EIP ← Pop();
    CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded *)
ELSE (* OperandSize = 16 *)
    IF top 4 bytes of stack not within stack limits
    THEN #SS(0); FI;
    tempEIP ← Pop();
    tempEIP ← tempEIP AND 0000FFFFH;
    IF tempEIP not within code segment limits
    THEN #GP(0); FI;
    EIP ← tempEIP;
    CS ← Pop(); (* 16-bit pop *)
INSTRUCTION SET REFERENCE, M-Z

IF instruction has immediate operand
THEN (* Release parameters from stack *)
    SP ← SP + (SRC AND FFFFH);
FI;
FI;

(* Protected mode, not virtual-8086 mode *)
IF (PE = 1 and VM = 0 and IA32_EFER.LMA = 0) and instruction = far return
THEN
    IF OperandSize = 32
        THEN
            IF second doubleword on stack is not within stack limits
                THEN #SS(0); FI;
            ELSE (* OperandSize = 16 *)
                IF second word on stack is not within stack limits
                    THEN #SS(0); FI;
            FI;
        FI;
    IF return code segment selector is NULL
        THEN #GP(0); FI;
    IF return code segment selector addresses descriptor beyond descriptor table limit
        THEN #GP(selector); FI;
    Obtain descriptor to which return code segment selector points from descriptor table;
    IF return code segment descriptor is not a code segment
        THEN #GP(selector); FI;
    IF return code segment selector RPL < CPL
        THEN #GP(selector); FI;
    IF return code segment descriptor is conforming
        and return code segment DPL > return code segment selector RPL
        THEN #GP(selector); FI;
    IF return code segment descriptor is non-conforming and return code segment DPL ≠ return code segment selector RPL
        THEN #GP(selector); FI;
    IF return code segment descriptor is not present
        THEN #NP(selector); FI;
    IF return code segment selector RPL > CPL
        THEN GOTO RETURN-OUTER-PRIVILEGE-LEVEL;
    ELSE GOTO RETURN-TO-SAME-PRIVILEGE-LEVEL;
    FI;
FI;
RETURN-SAME-PRIVILEGE-LEVEL:
    IF the return instruction pointer is not within the return code segment limit
        THEN #GP(0); FI;

4-472  Vol. 2B    RET—Return from Procedure
IF OperandSize = 32  
THEN  
  EIP ← Pop();  
  CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded *)  
ELSE (* OperandSize = 16 *)  
  EIP ← Pop();  
  EIP ← EIP AND 0000FFFFH;  
  CS ← Pop(); (* 16-bit pop *)  
FI;  
IF instruction has immediate operand  
THEN (* Release parameters from stack *)  
  IF StackAddressSize = 32  
    THEN  
      ESP ← ESP + SRC;  
    ELSE (* StackAddressSize = 16 *)  
      SP ← SP + SRC;  
    FI;  
  FI;  
RETURN-OUTER-PRIVILEGE-LEVEL:  
  IF top (16 + SRC) bytes of stack are not within stack limits (OperandSize = 32)  
  or top (8 + SRC) bytes of stack are not within stack limits (OperandSize = 16)  
    THEN #SS(0); FI;  
  Read return segment selector;  
  IF stack segment selector is NULL  
    THEN #GP(0); FI;  
  IF return stack segment selector index is not within its descriptor table limits  
    THEN #GP(selector); FI;  
  Read segment descriptor pointed to by return segment selector;  
  IF stack segment selector RPL ≠ RPL of the return code segment selector  
  or stack segment is not a writable data segment  
  or stack segment descriptor DPL ≠ RPL of the return code segment selector  
    THEN #GP(selector); FI;  
  IF stack segment not present  
    THEN #SS(StackSegmentSelector); FI;  
  IF the return instruction pointer is not within the return code segment limit  
    THEN #GP(0); FI;  
  CPL ← ReturnCodeSegmentSelector(RPL);  
  IF OperandSize = 32  
    THEN  
      EIP ← Pop();  
      CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded; segment descriptor loaded *)  
      CS(RPL) ← CPL;
IF instruction has immediate operand
THEN (* Release parameters from called procedure’s stack *)
  IF StackAddressSize = 32
  THEN
    ESP ← ESP + SRC;
  ELSE (* StackAddressSize = 16 *)
    SP ← SP + SRC;
  FI;
  FI;
  tempESP ← Pop();
  tempSS ← Pop(); (* 32-bit pop, high-order 16 bits discarded; seg. descriptor loaded *)
  ESP ← tempESP;
  SS ← tempSS;
ELSE (* OperandSize = 16 *)
  EIP ← Pop();
  EIP ← EIP AND 0000FFFFH;
  CS ← Pop(); (* 16-bit pop; segment descriptor loaded *)
  CS(RPL) ← CPL;
  IF instruction has immediate operand
  THEN (* Release parameters from called procedure’s stack *)
    IF StackAddressSize = 32
    THEN
      ESP ← ESP + SRC;
    ELSE (* StackAddressSize = 16 *)
      SP ← SP + SRC;
    FI;
    FI;
    tempESP ← Pop();
    tempSS ← Pop(); (* 16-bit pop; segment descriptor loaded *)
    ESP ← tempESP;
    SS ← tempSS;
  FI;
FOR each of segment register (ES, FS, GS, and DS)
  DO
    IF segment register points to data or non-conforming code segment
    and CPL > segment descriptor DPL (* DPL in hidden part of segment register *)
    THEN SegmentSelector ← 0; (* Segment selector invalid *)
    FI;
  OD;
IF instruction has immediate operand
THEN (* Release parameters from calling procedure’s stack *)
IF StackAddressSize = 32
THEN
    ESP ← ESP + SRC;
ELSE (* StackAddressSize = 16 *)
    SP ← SP + SRC;
FI;
FI;

(* IA-32e Mode *)
IF (PE = 1 and VM = 0 and IA32_EFER.LMA = 1) and instruction = far return
THEN
    IF OperandSize = 32
    THEN
        IF second doubleword on stack is not within stack limits
            THEN #SS(0); FI;
        IF first or second doubleword on stack is not in canonical space
            THEN #SS(0); FI;
    ELSE
        IF OperandSize = 16
        THEN
            IF second word on stack is not within stack limits
                THEN #SS(0); FI;
            IF first or second word on stack is not in canonical space
                THEN #SS(0); FI;
        ELSE (* OperandSize = 64 *)
            IF first or second quadword on stack is not in canonical space
                THEN #SS(0); FI;
        FI
    FI
    IF return code segment selector is NULL
    THEN GP(0); FI;
    IF return code segment selector addresses descriptor beyond descriptor table limit
    THEN GP(selector); FI;
    IF return code segment selector addresses descriptor in non-canonical space
    THEN GP(selector); FI;
    Obtain descriptor to which return code segment selector points from descriptor table;
    IF return code segment descriptor is not a code segment
    THEN #GP(selector); FI;
    IF return code segment descriptor has L-bit = 1 and D-bit = 1
    THEN #GP(selector); FI;
    IF return code segment selector RPL < CPL
    THEN #GP(selector); FI;
    IF return code segment descriptor is conforming
and return code segment DPL > return code segment selector RPL
    THEN #GP(selector); Fl;
IF return code segment descriptor is non-conforming
and return code segment DPL ≠ return code segment selector RPL
    THEN #GP(selector); Fl;
IF return code segment descriptor is not present
    THEN #NP(selector); Fl;
IF return code segment selector RPL > CPL
    THEN GOTO IA-32E-MODE-RETURN-OUTER-PRIVILEGE-LEVEL;
ELSE GOTO IA-32E-MODE-RETURN-SAME-PRIVILEGE-LEVEL;
FI;
FI;
IA-32E-MODE-RETURN-SAME-PRIVILEGE-LEVEL:
IF the return instruction pointer is not within the return code segment limit
    THEN #GP(0); Fl;
IF the return instruction pointer is not within canonical address space
    THEN #GP(0); Fl;
IF OperandSize = 32
    THEN
        EIP ← Pop();
        CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded *)
ELSE
    IF OperandSize = 16
        THEN
            EIP ← Pop();
            EIP ← EIP AND 0000FFFFH;
            CS ← Pop(); (* 16-bit pop *)
        ELSE (* OperandSize = 64 *)
            RIP ← Pop();
            CS ← Pop(); (* 64-bit pop, high-order 48 bits discarded *)
        FI;
    FI;
IF instruction has immediate operand
    THEN (* Release parameters from stack *)
        IF StackAddressSize = 32
            THEN
                ESP ← ESP + SRC;
        ELSE
            IF StackAddressSize = 16
                THEN
                    SP ← SP + SRC;
            ELSE (* StackAddressSize = 64 *)
        FI;
RSP ← RSP + SRC;
FI;
FI;
FI;

IA-32E-MODE-RETURN-OUTER-PRIVILEGE-LEVEL:
IF top (16 + SRC) bytes of stack are not within stack limits (OperandSize = 32)
or top (8 + SRC) bytes of stack are not within stack limits (OperandSize = 16)
THEN #SS(0); FI;
IF top (16 + SRC) bytes of stack are not in canonical address space (OperandSize = 32)
or top (8 + SRC) bytes of stack are not in canonical address space (OperandSize = 16)
or top (32 + SRC) bytes of stack are not in canonical address space (OperandSize = 64)
THEN #SS(0); FI;
Read return stack segment selector;
IF stack segment selector is NULL
THEN
IF new CS descriptor L-bit = 0
THEN #GP(selector);
IF stack segment selector RPL = 3
THEN #GP(selector);
FI;
IF return stack segment descriptor is not within descriptor table limits
THEN #GP(selector); FI;
IF return stack segment descriptor is in non-canonical address space
THEN #GP(selector); FI;
Read segment descriptor pointed to by return segment selector;
IF stack segment selector RPL ≠ RPL of the return code segment selector
or stack segment is not a writable data segment
or stack segment descriptor DPL ≠ RPL of the return code segment selector
THEN #GP(selector); FI;
IF stack segment not present
THEN #SS(StackSegmentSelector); FI;
IF the return instruction pointer is not within the return code segment limit
THEN #GP(0); FI;
IF the return instruction pointer is not within canonical address space
THEN #GP(0); FI;
CPL ← ReturnCodeSegmentSelector(RPL);
IF OperandSize = 32
THEN
EIP ← Pop();
CS ← Pop(); (* 32-bit pop, high-order 16 bits discarded, segment descriptor loaded *)
CS(RPL) ← CPL;
IF instruction has immediate operand
THEN (* Release parameters from called procedure's stack *)
IF StackAddressSize = 32
THEN
    ESP ← ESP + SRC;
ELSE
    IF StackAddressSize = 16
        THEN
            SP ← SP + SRC;
        ELSE (* StackAddressSize = 64 *)
            RSP ← RSP + SRC;
        FI;
    FI;
    FI;
    tempESP ← Pop();
    tempSS ← Pop(); (* 32-bit pop, high-order 16 bits discarded, segment descriptor loaded *)
    ESP ← tempESP;
    SS ← tempSS;
ELSE
    IF OperandSize = 16
        THEN
            EIP ← Pop();
            EIP ← EIP AND 0000FFFFH;
            CS ← Pop(); (* 16-bit pop; segment descriptor loaded *)
            CS(RPL) ← CPL;
            IF instruction has immediate operand
                THEN (* Release parameters from called procedure's stack *)
                    IF StackAddressSize = 32
                        THEN
                            ESP ← ESP + SRC;
                        ELSE
                            IF StackAddressSize = 16
                                THEN
                                    SP ← SP + SRC;
                                ELSE (* StackAddressSize = 64 *)
                                    RSP ← RSP + SRC;
                                FI;
                            FI;
            FI;
    FI;
    tempESP ← Pop();
    tempSS ← Pop(); (* 16-bit pop; segment descriptor loaded *)
    ESP ← tempESP;
    SS ← tempSS;
ELSE (* OperandSize = 64 *)
RET—Return from Procedure

RIP ← Pop();
CS ← Pop(); (* 64-bit pop; high-order 48 bits discarded; seg. descriptor loaded *)
CS(RPL) ← CPL;
IF instruction has immediate operand
    THEN (* Release parameters from called procedure's stack *)
        RSP ← RSP + SRC;
        FI;
    tempESP ← Pop();
    tempSS ← Pop(); (* 64-bit pop; high-order 48 bits discarded; seg. desc. loaded *)
    ESP ← tempESP;
    SS ← tempSS;
    FI;
FI;

FOR each of segment register (ES, FS, GS, and DS)
    DO
        IF segment register points to data or non-conforming code segment
            and CPL > segment descriptor DPL; (* DPL in hidden part of segment register *)
            THEN SegmentSelector ← 0; (* SegmentSelector invalid *)
            FI;
    OD;
IF instruction has immediate operand
    THEN (* Release parameters from calling procedure's stack *)
        IF StackAddressSize = 32
            THEN
                ESP ← ESP + SRC;
            ELSE
                IF StackAddressSize = 16
                    THEN
                        SP ← SP + SRC;
                    ELSE (* StackAddressSize = 64 *)
                        RSP ← RSP + SRC;
                    FI;
                FI;
        FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the return code or stack segment selector NULL.
INSTRUCTION SET REFERENCE, M-Z

If the return instruction pointer is not within the return code segment limit

#GP(selector) If the RPL of the return code segment selector is less than the CPL.
If the return code or stack segment selector index is not within its descriptor table limits.
If the return code segment descriptor does not indicate a code segment.
If the return code segment is non-conforming and the segment selector’s DPL is not equal to the RPL of the code segment’s segment selector.
If the return code segment is conforming and the segment selector’s DPL greater than the RPL of the code segment’s segment selector.
If the stack segment is not a writable data segment.
If the stack segment selector RPL is not equal to the RPL of the return code segment selector.
If the stack segment descriptor DPL is not equal to the RPL of the return code segment selector.

#SS(0) If the top bytes of stack are not within stack limits.
If the return stack segment is not present.

#NP(selector) If the return code segment is not present.

#PF(fault-code) If a page fault occurs.

#AC(0) If an unaligned memory access occurs when the CPL is 3 and alignment checking is enabled.

Real-Address Mode Exceptions

#GP If the return instruction pointer is not within the return code segment limit
#SS If the top bytes of stack are not within stack limits.

Virtual-8086 Mode Exceptions

#GP(0) If the return instruction pointer is not within the return code segment limit
#SS(0) If the top bytes of stack are not within stack limits.
#PF(fault-code) If a page fault occurs.
#AC(0) If an unaligned memory access occurs when alignment checking is enabled.

Compatibility Mode Exceptions

Same as 64-bit mode exceptions.
64-Bit Mode Exceptions

#GP(0)  
If the return instruction pointer is non-canonical.
If the return instruction pointer is not within the return code segment limit.
If the stack segment selector is NULL going back to compatibility mode.
If the stack segment selector is NULL going back to CPL3 64-bit mode.
If a NULL stack segment selector RPL is not equal to CPL going back to non-CPL3 64-bit mode.
If the return code segment selector is NULL.

#GP(selector)  
If the proposed segment descriptor for a code segment does not indicate it is a code segment.
If the proposed new code segment descriptor has both the D-bit and L-bit set.
If the DPL for a nonconforming-code segment is not equal to the RPL of the code segment selector.
If CPL is greater than the RPL of the code segment selector.
If the DPL of a conforming-code segment is greater than the return code segment selector RPL.
If a segment selector index is outside its descriptor table limits.
If a segment descriptor memory address is non-canonical.
If the stack segment is not a writable data segment.
If the stack segment descriptor DPL is not equal to the RPL of the return code segment selector.
If the stack segment selector RPL is not equal to the RPL of the return code segment selector.

#SS(0)  
If an attempt to pop a value off the stack violates the SS limit.
If an attempt to pop a value off the stack causes a non-canonical address to be referenced.

#NP(selector)  
If the return code or stack segment is not present.

#PF(fault-code)  
If a page fault occurs.

#AC(0)  
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
ROUNDPD — Round Packed Double Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode*/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 09 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Round packed double precision floating-point values in xmm2/m128 and place the result in xmm1. The rounding mode is determined by imm8.</td>
</tr>
<tr>
<td>VEX.128.66.0F3A.WIG 09 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Round packed double-precision floating-point values in xmm2/m128 and place the result in xmm1. The rounding mode is determined by imm8.</td>
</tr>
<tr>
<td>VEX.256.66.0F3A.WIG 09 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Round packed double-precision floating-point values in ymm2/m256 and place the result in ymm1. The rounding mode is determined by imm8.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Round the 2 double-precision floating-point values in the source operand (second operand) using the rounding mode specified in the immediate operand (third operand) and place the results in the destination operand (first operand). The rounding process rounds each input floating-point value to an integer value and returns the integer result as a single-precision floating-point value.

The immediate operand specifies control fields for the rounding operation, three bit fields are defined and shown in Figure 4-17. Bit 3 of the immediate byte controls processor behavior for a precision exception, bit 2 selects the source of rounding mode control. Bits 1:0 specify a non-sticky rounding-mode value (Table 4-17 lists the encoded values for rounding-mode field).

The Precision Floating-Point Exception is signaled according to the immediate operand. If any source operand is an SNaN then it will be converted to a QNaN. If DAZ is set to 1 then denormals will be converted to zero before rounding.
ROUNDPD — Round Packed Double Precision Floating-Point Values

128-bit Legacy SSE version: The second source can be an XMM register or 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the source operand second source operand or a 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

\[
\text{Figure 4-17. Bit Control Fields of Immediate Byte for ROUNDxx Instruction}
\]

\[
\begin{array}{cccc}
8 & \text{Reserved} & 3 & 2 & 1 & 0 \\
\end{array}
\]

- **P** — Precision Mask; 0: normal, 1: inexact
- **RS** — Rounding select; 1: MXCSR.RC, 0: Imm8.RC
- **RC** — Rounding mode

\[
\text{Table 4-17. Rounding Modes and Encoding of Rounding Control (RC) Field}
\]

<table>
<thead>
<tr>
<th>Rounding Mode</th>
<th>RC Field Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Round to nearest (even)</td>
<td>00B</td>
<td>Rounded result is the closest to the infinitely precise result. If two values are equally close, the result is the even value (i.e., the integer value with the least-significant bit of zero).</td>
</tr>
<tr>
<td>Round down (toward (-\infty))</td>
<td>01B</td>
<td>Rounded result is closest to but no greater than the infinitely precise result.</td>
</tr>
<tr>
<td>Round up (toward (+\infty))</td>
<td>10B</td>
<td>Rounded result is closest to but no less than the infinitely precise result.</td>
</tr>
<tr>
<td>Round toward zero (Truncate)</td>
<td>11B</td>
<td>Rounded result is closest to but no greater in absolute value than the infinitely precise result.</td>
</tr>
</tbody>
</table>

**Operation**

\[
\text{IF (imm[2] = '1)} \\
\text{THEN /} \text{ rounding mode is determined by MXCSR.RC} \\
\text{DEST}[63:0] \leftarrow \text{ConvertDPFPToInteger}_M[\text{SRC}[63:0]]; \\
\text{DEST}[127:64] \leftarrow \text{ConvertDPFPToInteger}_M[\text{SRC}[127:64]]; \\
\]
ELSE // rounding mode is determined by IMM8.RC
    DEST[63:0] ← ConvertDPFPToInteger_Imm(SRC[63:0]);
    DEST[127:64] ← ConvertDPFPToInteger_Imm(SRC[127:64]);
FI

ROUNDPD (128-bit Legacy SSE version)
DEST[63:0] ← RoundToInteger(SRC[63:0], ROUND_CONTROL)
DEST[127:64] ← RoundToInteger(SRC[127:64], ROUND_CONTROL)
DEST[VLMAX-1:128] (Unmodified)

VROUNDPD (VEX.128 encoded version)
DEST[63:0] ← RoundToInteger(SRC[63:0], ROUND_CONTROL)
DEST[127:64] ← RoundToInteger(SRC[127:64], ROUND_CONTROL)
DEST[VLMAX-1:128] ← 0

VROUNDPD (VEX.256 encoded version)
DEST[63:0] ← RoundToInteger(SRC[63:0], ROUND_CONTROL)
DEST[127:64] ← RoundToInteger(SRC[127:64], ROUND_CONTROL)
DEST[191:128] ← RoundToInteger(SRC[191:128], ROUND_CONTROL)
DEST[255:192] ← RoundToInteger(SRC[255:192], ROUND_CONTROL)

Intel C/C++ Compiler Intrinsic Equivalent
__m128 _mm_round_pd(__m128d s1, int iRoundMode);
__m128 _mm_floor_pd(__m128d s1);
__m128 _mm ceil_pd(__m128d s1)
__m256 _mm256_round_pd(__m256d s1, int iRoundMode);
__m256 _mm256_floor_pd(__m256d s1);
__m256 _mm256 ceil_pd(__m256d s1)

SIMD Floating-Point Exceptions
Invalid (signaled only if SRC = SNaN)
Precision (signaled only if imm[3] = '0; if imm[3] = '1, then the Precision Mask in the M8XCSR is ignored and precision exception is not signaled.)
Note that Denormal is not signaled by ROUNDPD.

Other Exceptions
See Exceptions Type 2; additionally
#UD If VEX.vvvv != 1111B.
### ROUNDPS — Round Packed Single Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 08</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Round packed single precision floating-point values in <code>xmm2/m128</code> and place the result in <code>xmm1</code>. The rounding mode is determined by <code>imm8</code>.</td>
</tr>
<tr>
<td>VEX.128.66.0F3A.WIG 08</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Round packed single-precision floating-point values in <code>xmm2/m128</code> and place the result in <code>xmm1</code>. The rounding mode is determined by <code>imm8</code>.</td>
</tr>
<tr>
<td>VEX.256.66.0F3A.WIG 08</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Round packed single-precision floating-point values in <code>ymm2/m256</code> and place the result in <code>ymmm1</code>. The rounding mode is determined by <code>imm8</code>.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Round the 4 single-precision floating-point values in the source operand (second operand) using the rounding mode specified in the immediate operand (third operand) and place the results in the destination operand (first operand). The rounding process rounds each input floating-point value to an integer value and returns the integer result as a single-precision floating-point value.

The immediate operand specifies control fields for the rounding operation, three bit fields are defined and shown in Figure 4-17. Bit 3 of the immediate byte controls processor behavior for a precision exception, bit 2 selects the source of rounding mode control. Bits 1:0 specify a non-sticky rounding-mode value (Table 4-17 lists the encoded values for rounding-mode field).

The Precision Floating-Point Exception is signaled according to the immediate operand. If any source operand is an SNaN then it will be converted to a QNaN. If DAZ is set to `1` then denormals will be converted to zero before rounding.
128-bit Legacy SSE version: The second source can be an XMM register or 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the source operand second source operand or a 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

\[ \text{IF (imm[2] = '1') } \]
\[ \text{THEN // rounding mode is determined by MXCSR.RC} \]
\[ \text{DEST}[31:0] \leftarrow \text{ConvertSPFPTointeger}_M(SRC[31:0]); \]
\[ \text{DEST}[63:32] \leftarrow \text{ConvertSPFPTointeger}_M(SRC[63:32]); \]
\[ \text{DEST}[95:64] \leftarrow \text{ConvertSPFPTointeger}_M(SRC[95:64]); \]
\[ \text{DEST}[127:96] \leftarrow \text{ConvertSPFPTointeger}_M(SRC[127:96]); \]
\[ \text{ELSE // rounding mode is determined by IMM8.RC} \]
\[ \text{DEST}[31:0] \leftarrow \text{ConvertSPFPTointeger}_Imm(SRC[31:0]); \]
\[ \text{DEST}[63:32] \leftarrow \text{ConvertSPFPTointeger}_Imm(SRC[63:32]); \]
\[ \text{DEST}[95:64] \leftarrow \text{ConvertSPFPTointeger}_Imm(SRC[95:64]); \]
\[ \text{DEST}[127:96] \leftarrow \text{ConvertSPFPTointeger}_Imm(SRC[127:96]); \]
\[ \text{FI;} \]

**ROUNDPS (128-bit Legacy SSE version)**

\[ \text{DEST}[31:0] \leftarrow \text{RoundToInteger}(SRC[31:0], \text{ROUND}\_\text{CONTROL}) \]
\[ \text{DEST}[63:32] \leftarrow \text{RoundToInteger}(SRC[63:32], \text{ROUND}\_\text{CONTROL}) \]
\[ \text{DEST}[95:64] \leftarrow \text{RoundToInteger}(SRC[95:64], \text{ROUND}\_\text{CONTROL}) \]
\[ \text{DEST}[127:96] \leftarrow \text{RoundToInteger}(SRC[127:96], \text{ROUND}\_\text{CONTROL}) \]
\[ \text{DEST}[\text{VLMAX-1:128}] \leftarrow 0 \]

**VROUNDPS (VEX.128 encoded version)**

\[ \text{DEST}[31:0] \leftarrow \text{RoundToInteger}(SRC[31:0], \text{ROUND}\_\text{CONTROL}) \]
\[ \text{DEST}[63:32] \leftarrow \text{RoundToInteger}(SRC[63:32], \text{ROUND}\_\text{CONTROL}) \]
\[ \text{DEST}[95:64] \leftarrow \text{RoundToInteger}(SRC[95:64], \text{ROUND}\_\text{CONTROL}) \]
\[ \text{DEST}[127:96] \leftarrow \text{RoundToInteger}(SRC[127:96], \text{ROUND}\_\text{CONTROL}) \]
\[ \text{DEST}[\text{VLMAX-1:128}] \leftarrow 0 \]

**VROUNDPS (VEX.256 encoded version)**

\[ \text{DEST}[31:0] \leftarrow \text{RoundToInteger}(SRC[31:0], \text{ROUND}\_\text{CONTROL}) \]
ROUNDPS — Round Packed Single Precision Floating-Point Values

**INSTRUCTION SET REFERENCE, M-Z**

DEST[63:32] ← RoundToInteger(SRC[63:32], ROUND_CONTROL)
DEST[95:64] ← RoundToInteger(SRC[95:64], ROUND_CONTROL)
DEST[127:96] ← RoundToInteger(SRC[127:96], ROUND_CONTROL)
DEST[159:128] ← RoundToInteger(SRC[159:128], ROUND_CONTROL)
DEST[191:160] ← RoundToInteger(SRC[191:160], ROUND_CONTROL)
DEST[223:192] ← RoundToInteger(SRC[223:192], ROUND_CONTROL)
DEST[255:224] ← RoundToInteger(SRC[255:224], ROUND_CONTROL)

**Intel C/C++ Compiler Intrinsic Equivalent**

__m128 _mm_round_ps(__m128 s1, int iRoundMode);
__m128 _mm_floor_ps(__m128 s1);
__m128 _mm_ceil_ps(__m128 s1)
__m256 _mm256_round_ps(__m256 s1, int iRoundMode);
__m256 _mm256_floor_ps(__m256 s1);
__m256 _mm256_ceil_ps(__m256 s1)

**SIMD Floating-Point Exceptions**

Invalid (signaled only if SRC = SNaN)
Precision (signaled only if imm[3] = '0; if imm[3] = '1, then the Precision Mask in the MXCSR is ignored and precision exception is not signaled.)
Note that Denormal is not signaled by ROUNDPS.

**Other Exceptions**

See Exceptions Type 2; additionally
#UD If VEX.vvvv != 1111B.
ROUNDSD — Round Scalar Double Precision Floating-Point Values

### Instruction Encoding

<table>
<thead>
<tr>
<th>Opcode*/* Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 0B /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Round the low packed double precision floating-point value in xmm2/m64 and place the result in xmm1. The rounding mode is determined by imm8.</td>
</tr>
<tr>
<td>VEX.NDS.LIG.66.0F3A.WIG 0B /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Round the low packed double precision floating-point value in xmm3/m64 and place the result in xmm1. The rounding mode is determined by imm8. Upper packed double precision floating-point value (bits[127:64]) from xmm2 is copied to xmm1[127:64].</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

### Description

Round the DP FP value in the lower qword of the source operand (second operand) using the rounding mode specified in the immediate operand (third operand) and place the result in the destination operand (first operand). The rounding process rounds a double-precision floating-point input to an integer value and returns the integer result as a double precision floating-point value in the lowest position. The upper double precision floating-point value in the destination is retained.

The immediate operand specifies control fields for the rounding operation, three bit fields are defined and shown in Figure 4-17. Bit 3 of the immediate byte controls processor behavior for a precision exception, bit 2 selects the source of rounding mode control. Bits 1:0 specify a non-sticky rounding-mode value (Table 4-17 lists the encoded values for rounding-mode field).

The Precision Floating-Point Exception is signaled according to the immediate operand. If any source operand is an SNaN then it will be converted to a QNaN. If DAZ is set to ‘1 then denormals will be converted to zero before rounding.
128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

IF (imm[2] = '1')
   THEN  // rounding mode is determined by MXCSR.RC
         DEST[63:0] ← ConvertDPFPToInteger_M(SRC[63:0]);
   ELSE  // rounding mode is determined by IMM8.RC
         DEST[63:0] ← ConvertDPFPToInteger_Imm(SRC[63:0]);
  FI;
DEST[127:63] remains unchanged;

**ROUNDSD (128-bit Legacy SSE version)**
DEST[63:0] ← RoundToInteger(SRC[63:0], ROUND_CONTROL)
DEST[VLMAX-1:64] (Unmodified)

**VROUNDSD (VEX.128 encoded version)**
DEST[63:0] ← RoundToInteger(SRC2[63:0], ROUND_CONTROL)
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

ROUNDSD: __m128d mm_round_sd(__m128d dst, __m128d s1, int iRoundMode);
          __m128d mm_floor_sd(__m128d dst, __m128d s1);
          __m128d mm_ceil_sd(__m128d dst, __m128d s1);

**SIMD Floating-Point Exceptions**

Invalid (signaled only if SRC = SNaN)
Precision (signaled only if imm[3] = '0; if imm[3] = '1, then the Precision Mask in the MXCSR is ignored and precision exception is not signaled.)
Note that Denormal is not signaled by ROUNDSD.

**Other Exceptions**

See Exceptions Type 3.
ROUNDSS — Round Scalar Single Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode*/* Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 3A 0A /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE4_1</td>
<td>Round the low packed single precision floating-point value in xmm2/m32 and place the result in xmm1. The rounding mode is determined by imm8.</td>
</tr>
<tr>
<td>VEX.NDS.LIG.66.0F3A,W IG 0A ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Round the low packed single precision floating-point value in xmm3/m32 and place the result in xmm1. The rounding mode is determined by imm8. Also, upper packed single precision floating-point values (bits[127:32]) from xmm2 are copied to xmm1[127:32].</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Round the single-precision floating-point value in the lowest dword of the source operand (second operand) using the rounding mode specified in the immediate operand (third operand) and place the result in the destination operand (first operand). The rounding process rounds a single-precision floating-point input to an integer value and returns the result as a single-precision floating-point value in the lowest position. The upper three single-precision floating-point values in the destination are retained.

The immediate operand specifies control fields for the rounding operation, three bit fields are defined and shown in Figure 4-17. Bit 3 of the immediate byte controls processor behavior for a precision exception, bit 2 selects the source of rounding mode control. Bits 1:0 specify a non-sticky rounding-mode value (Table 4-17 lists the encoded values for rounding-mode field).
The Precision Floating-Point Exception is signaled according to the immediate operand. If any source operand is an SNaN then it will be converted to a QNaN. If DAZ is set to '1 then denormals will be converted to zero before rounding.

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

**Operation**

IF (imm[2] = '1')
  THEN // rounding mode is determined by MXCSR.RC
    DEST[31:0] ← ConvertSPFPToInteger_M(SRC[31:0]);
  ELSE // rounding mode is determined by IMM8.RC
    DEST[31:0] ← ConvertSPFPToInteger_Imm(SRC[31:0]);
FI;
DEST[127:32] remains unchanged;

**ROUNDSS (128-bit Legacy SSE version)**
DEST[31:0] ← RoundToInteger(SRC[31:0], ROUND_CONTROL)
DEST[VLMAX-1:32] (Unmodified)

**VROUNDSS (VEX.128 encoded version)**
DEST[31:0] ← RoundToInteger(SRC2[31:0], ROUND_CONTROL)
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

ROUNDSS:  __m128 mm_round_ss(__m128 dst, __m128 s1, int iRoundMode);
          __m128 mm_floor_ss(__m128 dst, __m128 s1);
          __m128 mm_ceil_ss(__m128 dst, __m128 s1);

**SIMD Floating-Point Exceptions**

Invalid (signaled only if SRC = SNaN)
Precision (signaled only if imm[3] = '0; if imm[3] = '1, then the Precision Mask in the MXCSR is ignored and precision exception is not signaled.)
Note that Denormal is not signaled by ROUNDSS.

**Other Exceptions**

See Exceptions Type 3.
RSM—Resume from System Management Mode

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Log Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AA</td>
<td>RSM</td>
<td>NP</td>
<td>Invalid</td>
<td>Valid</td>
<td>Resume operation of interrupted program.</td>
</tr>
</tbody>
</table>

**Description**

Returns program control from system management mode (SMM) to the application program or operating-system procedure that was interrupted when the processor received an SMM interrupt. The processor’s state is restored from the dump created upon entering SMM. If the processor detects invalid state information during state restoration, it enters the shutdown state. The following invalid information can cause a shutdown:

- Any reserved bit of CR4 is set to 1.
- Any illegal combination of bits in CR0, such as (PG=1 and PE=0) or (NW=1 and CD=0).
- (Intel Pentium and Intel486™ processors only.) The value stored in the state dump base field is not a 32-KByte aligned address.

The contents of the model-specific registers are not affected by a return from SMM.

The SMM state map used by RSM supports resuming processor context for non-64-bit modes and 64-bit mode.


**Operation**

ReturnFromSMM;
IF (IA-32e mode supported) or (CPUID DisplayFamily_DisplayModel = 06H_0CH )
THEN
   ProcessorState ← Restore(SMMDump(IA-32e SMM STATE MAP));
Else
   ProcessorState ← Restore(SMMDump(Non-32-Bit-Mode SMM STATE MAP));
FI
Flags Affected
All.

Protected Mode Exceptions
#UD If an attempt is made to execute this instruction when the processor is not in SMM.
If the LOCK prefix is used.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
RSQRTPS—Compute Reciprocals of Square Roots of Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode*/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 52 /r RSRQRTPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Computes the approximate reciprocals of the square roots of the packed single-precision floating-point values in xmm2/m128 and stores the results in xmm1.</td>
</tr>
<tr>
<td>VEX.128.0F.WIG 52 /r VRSQRTPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes the approximate reciprocals of the square roots of packed single-precision values in xmm2/mem and stores the results in xmm1.</td>
</tr>
<tr>
<td>VEX.256.0F.WIG 52 /r VRSQRTPS ymm1, ymm2/m256</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes the approximate reciprocals of the square roots of packed single-precision values in ymm2/mem and stores the results in ymm1.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD computation of the approximate reciprocals of the square roots of the four packed single-precision floating-point values in the source operand (second operand) and stores the packed single-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 10-5 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for an illustration of a SIMD single-precision floating-point operation.

The relative error for this approximation is:

\[ |\text{Relative Error}| \leq 1.5 \times 2^{-12} \]

The RSQRTPS instruction is not affected by the rounding control bits in the MXCSR register. When a source value is a 0.0, an \( \infty \) of the sign of the source value is returned. A denormal source value is treated as a 0.0 (of the same sign). When a
source value is a negative value (other than −0.0), a floating-point indefinite is returned. When a source value is an SNaN or QNaN, the SNaN is converted to a QNaN or the source QNaN is returned.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

VEX.128 encoded version: The first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

Operation

**RSQRTPS (128-bit Legacy SSE version)**

\[
\begin{align*}
\text{DEST}[31:0] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[31:0]}) \\
\text{DEST}[63:32] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[63:32]}) \\
\text{DEST}[95:64] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[95:64]}) \\
\text{DEST}[127:96] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[127:96]}) \\
\text{DEST}[\text{VLMAX-1:128}] &\leftarrow 0
\end{align*}
\]

**VRSQRTPS (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[31:0]}) \\
\text{DEST}[63:32] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[63:32]}) \\
\text{DEST}[95:64] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[95:64]}) \\
\text{DEST}[127:96] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[127:96]}) \\
\text{DEST}[\text{VLMAX-1:128}] &\leftarrow 0
\end{align*}
\]

**VRSQRTPS (VEX.256 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[31:0]}) \\
\text{DEST}[63:32] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[63:32]}) \\
\text{DEST}[95:64] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[95:64]}) \\
\text{DEST}[127:96] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[127:96]}) \\
\text{DEST}[159:128] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[159:128]}) \\
\text{DEST}[191:160] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[191:160]}) \\
\text{DEST}[223:192] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[223:192]}) \\
\text{DEST}[255:224] &\leftarrow \text{APPROXIMATE}(1/\sqrt{\text{SRC}[255:224]})
\end{align*}
\]
RSQRTPS—Compute Reciprocals of Square Roots of Packed Single-Precision Floating-Point Values

**INSTRUCTION SET REFERENCE, M-Z**

**Intel C/C++ Compiler Intrinsic Equivalent**

RSQRTPS: \[ \texttt{\_m128 \_mm\_rsqrt\_ps(\_m128 a)} \]
RSQRTPS: \[ \texttt{\_m256 \_mm256\_rsqrt\_ps (\_m256 a)}; \]

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4; additionally

#UD If VEX.vvvv != 1111B.
RSQRTSS—Compute Reciprocal of Square Root of Scalar Single-Precision Floating-Point Value

<table>
<thead>
<tr>
<th>Opcode*/ Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 52 /r RSQRTSS xmm1, xmm2/m32</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Computes the approximate reciprocal of the square root of the low single-precision floating-point value in xmm2/m32 and stores the results in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.WIG 52 /r VRSQRTSS xmm1, xmm2, xmm3/m32</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes the approximate reciprocal of the square root of the low single precision floating-point value in xmm3/m32 and stores the results in xmm1. Also, upper single precision floating-point values (bits[127:32]) from xmm2 are copied to xmm1[127:32].</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Computes an approximate reciprocal of the square root of the low single-precision floating-point value in the source operand (second operand) stores the single-precision floating-point result in the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The three high-order doublewords of the destination operand remain unchanged. See Figure 10-6 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1*, for an illustration of a scalar single-precision floating-point operation.

The relative error for this approximation is:

$$|\text{Relative Error}| \leq 1.5 \times 2^{-12}$$

The RSQRTSS instruction is not affected by the rounding control bits in the MXCSR register. When a source value is a 0.0, an $\infty$ of the sign of the source value is returned. A denormal source value is treated as a 0.0 (of the same sign). When a
source value is a negative value (other than −0.0), a floating-point indefinite is returned. When a source value is an SNaN or QNaN, the SNaN is converted to a QNaN or the source QNaN is returned.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.

Operation

RSQRTSS (128-bit Legacy SSE version)
DEST[31:0] ← APPROXIMATE(1/SQRT(SRC2[31:0]))
DEST[VLMAX-1:32] (Unmodified)

VRSQRTSS (VEX.128 encoded version)
DEST[31:0] ← APPROXIMATE(1/SQRT(SRC2[31:0]))
DEST[127:32] ← SRC1[31:0]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
RSQRTSS:  __m128 _mm_rsqrt_ss(__m128 a)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5.
**SAHF—Store AH into Flags**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9E</td>
<td>SAHF</td>
<td>NP</td>
<td>Invalid*</td>
<td>Valid</td>
<td>Loads SF, ZF, AF, PF, and CF from AH into EFLAGS register.</td>
</tr>
</tbody>
</table>

**NOTES:**
* Valid in specific stepping. See Description section.

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**
Loads the SF, ZF, AF, PF, and CF flags of the EFLAGS register with values from the corresponding bits in the AH register (bits 7, 6, 4, 2, and 0, respectively). Bits 1, 3, and 5 of register AH are ignored; the corresponding reserved bits (1, 3, and 5) in the EFLAGS register remain as shown in the “Operation” section below.

This instruction executes as described above in compatibility mode and legacy mode. It is valid in 64-bit mode only if CPUID.80000001H:ECX.LAHF-SAHF[bit 0] = 1.

**Operation**

IF IA-64 Mode
THEN
  IF CPUID.80000001H.ECX[0] = 1;
  THEN
    RFLAGS(SF:ZF:0:AF:0:PF:1:CF) ← AH;
  ELSE
    #UD;
  FI
ELSE
  EFLAGS(SF:ZF:0:AF:0:PF:1:CF) ← AH;
FI

**Flags Affected**
The SF, ZF, AF, PF, and CF flags are loaded with values from the AH register. Bits 1, 3, and 5 of the EFLAGS register are unaffected, with the values remaining 1, 0, and 0, respectively.
Protected Mode Exceptions
None.

Real-Address Mode Exceptions
None.

Virtual-8086 Mode Exceptions
None.

Compatibility Mode Exceptions
None.

64-Bit Mode Exceptions
#UD If CPUID.80000001H.ECX[0] = 0.
If the LOCK prefix is used.
**SAL/SAR/SHL/SHR—Shift**

<table>
<thead>
<tr>
<th>Opcode***</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0 /4</td>
<td>SAL r/m8, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m8 by 2, once.</td>
</tr>
<tr>
<td>REX + D0 /4</td>
<td>SAL r/m8**, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m8 by 2, once.</td>
</tr>
<tr>
<td>D2 /4</td>
<td>SAL r/m8, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m8 by 2, CL times.</td>
</tr>
<tr>
<td>REX + D2 /4</td>
<td>SAL r/m8**, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m8 by 2, CL times.</td>
</tr>
<tr>
<td>C0 /4 ib</td>
<td>SAL r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m8 by 2, imm8 times.</td>
</tr>
<tr>
<td>REX + C0 /4 ib</td>
<td>SAL r/m8**, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m8 by 2, imm8 times.</td>
</tr>
<tr>
<td>D1 /4</td>
<td>SAL r/m16, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m16 by 2, once.</td>
</tr>
<tr>
<td>D3 /4</td>
<td>SAL r/m16, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m16 by 2, CL times.</td>
</tr>
<tr>
<td>C1 /4 ib</td>
<td>SAL r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m16 by 2, imm8 times.</td>
</tr>
<tr>
<td>D1 /4</td>
<td>SAL r/m32, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m32 by 2, once.</td>
</tr>
<tr>
<td>REX + D1 /4</td>
<td>SAL r/m64, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m64 by 2, once.</td>
</tr>
<tr>
<td>D3 /4</td>
<td>SAL r/m32, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m32 by 2, CL times.</td>
</tr>
<tr>
<td>REX.W + D3 /4</td>
<td>SAL r/m64, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m64 by 2, CL times.</td>
</tr>
<tr>
<td>C1 /4 ib</td>
<td>SAL r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m32 by 2, imm8 times.</td>
</tr>
<tr>
<td>REX.W + C1 /4 ib</td>
<td>SAL r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m64 by 2, imm8 times.</td>
</tr>
<tr>
<td>D0 /7</td>
<td>SAR r/m8, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m8 by 2, once.</td>
</tr>
<tr>
<td>REX + D0 /7</td>
<td>SAR r/m8**, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Signed divide* r/m8 by 2, once.</td>
</tr>
<tr>
<td>D2 /7</td>
<td>SAR r/m8, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m8 by 2, CL times.</td>
</tr>
<tr>
<td>REX + D2 /7</td>
<td>SAR r/m8**, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Signed divide* r/m8 by 2, CL times.</td>
</tr>
<tr>
<td>C0 /7 ib</td>
<td>SAR r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m8 by 2, imm8 time.</td>
</tr>
<tr>
<td>REX + C0 /7 ib</td>
<td>SAR r/m8**, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Signed divide* r/m8 by 2, imm8 times.</td>
</tr>
</tbody>
</table>
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<th>Instruction</th>
<th>Op/En</th>
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<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1 /7</td>
<td>SAR r/m16,1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m16 by 2, once.</td>
</tr>
<tr>
<td>D3 /7</td>
<td>SAR r/m16, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m16 by 2, CL times.</td>
</tr>
<tr>
<td>C1 /7 ib</td>
<td>SAR r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m16 by 2, imm8 times.</td>
</tr>
<tr>
<td>D1 /7</td>
<td>SAR r/m32, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m32 by 2, once.</td>
</tr>
<tr>
<td>REX.w + D1 /7</td>
<td>SAR r/m64, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Signed divide* r/m64 by 2, once.</td>
</tr>
<tr>
<td>D3 /7</td>
<td>SAR r/m32, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m32 by 2, CL times.</td>
</tr>
<tr>
<td>REX.w + D3 /7</td>
<td>SAR r/m64, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Signed divide* r/m64 by 2, CL times.</td>
</tr>
<tr>
<td>C1 /7 ib</td>
<td>SAR r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Signed divide* r/m32 by 2, imm8 times.</td>
</tr>
<tr>
<td>REX.w + C1 /7 ib</td>
<td>SAR r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Signed divide* r/m64 by 2, imm8 times.</td>
</tr>
<tr>
<td>D0 /4</td>
<td>SHL r/m8, 1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m8 by 2, once.</td>
</tr>
<tr>
<td>REX + D0 /4</td>
<td>SHL r/m8**, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m8 by 2, once.</td>
</tr>
<tr>
<td>D2 /4</td>
<td>SHL r/m8, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m8 by 2, CL times.</td>
</tr>
<tr>
<td>REX + D2 /4</td>
<td>SHL r/m8**, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m8 by 2, CL times.</td>
</tr>
<tr>
<td>C0 /4 ib</td>
<td>SHL r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m8 by 2, imm8 times.</td>
</tr>
<tr>
<td>REX + C0 /4 ib</td>
<td>SHL r/m8**, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m8 by 2, imm8 times.</td>
</tr>
<tr>
<td>D1 /4</td>
<td>SHL r/m16,1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m16 by 2, once.</td>
</tr>
<tr>
<td>D3 /4</td>
<td>SHL r/m16, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m16 by 2, CL times.</td>
</tr>
<tr>
<td>C1 /4 ib</td>
<td>SHL r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m16 by 2, imm8 times.</td>
</tr>
<tr>
<td>D1 /4</td>
<td>SHL r/m32,1</td>
<td>M1</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m32 by 2, once.</td>
</tr>
<tr>
<td>REX.w + D1 /4</td>
<td>SHL r/m64,1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m64 by 2, once.</td>
</tr>
<tr>
<td>D3 /4</td>
<td>SHL r/m32, CL</td>
<td>MC</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m32 by 2, CL times.</td>
</tr>
<tr>
<td>REX.w + D3 /4</td>
<td>SHL r/m64, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m64 by 2, CL times.</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>Op/En</td>
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<td>Compat/ Leg Mode</td>
<td>Description</td>
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<td>-------------</td>
<td>------------------</td>
<td>------------------------------------------</td>
</tr>
<tr>
<td>C1 /4 ib</td>
<td>SHL r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Multiply r/m32 by 2, imm8 times.</td>
</tr>
<tr>
<td>REX.W + C1 ib /4</td>
<td>SHL r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Multiply r/m64 by 2, imm8 times.</td>
</tr>
<tr>
<td>D0 /5</td>
<td>SHR r/m8,1</td>
<td>M1</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m8 by 2, once.</td>
</tr>
<tr>
<td>REX + D0 /5</td>
<td>SHR r/m8**, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide r/m8 by 2, once.</td>
</tr>
<tr>
<td>D2 /5</td>
<td>SHR r/m8, CL</td>
<td>MC</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m8 by 2, CL times.</td>
</tr>
<tr>
<td>REX + D2 /5</td>
<td>SHR r/m8**, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide r/m8 by 2, CL times.</td>
</tr>
<tr>
<td>C0 /5 ib</td>
<td>SHR r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m8 by 2, imm8 times.</td>
</tr>
<tr>
<td>REX + C0 /5 ib</td>
<td>SHR r/m8**, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide r/m8 by 2, imm8 times.</td>
</tr>
<tr>
<td>D1 /5</td>
<td>SHR r/m16, 1</td>
<td>M1</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m16 by 2, once.</td>
</tr>
<tr>
<td>D3 /5</td>
<td>SHR r/m16, CL</td>
<td>MC</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m16 by 2, CL times</td>
</tr>
<tr>
<td>C1 /5 ib</td>
<td>SHR r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m16 by 2, imm8 times.</td>
</tr>
<tr>
<td>D1 /5</td>
<td>SHR r/m32, 1</td>
<td>M1</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m32 by 2, once.</td>
</tr>
<tr>
<td>REX.W + D1 /5</td>
<td>SHR r/m64, 1</td>
<td>M1</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide r/m64 by 2, once.</td>
</tr>
<tr>
<td>D3 /5</td>
<td>SHR r/m32, CL</td>
<td>MC</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m32 by 2, CL times.</td>
</tr>
<tr>
<td>REX.W + D3 /5</td>
<td>SHR r/m64, CL</td>
<td>MC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide r/m64 by 2, CL times.</td>
</tr>
<tr>
<td>C1 /5 ib</td>
<td>SHR r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td></td>
<td>Unsigned divide r/m32 by 2, imm8 times.</td>
</tr>
<tr>
<td>REX.W + C1 ib /5</td>
<td>SHR r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Unsigned divide r/m64 by 2, imm8 times.</td>
</tr>
</tbody>
</table>
INSTRUCTION SET REFERENCE, M-Z

NOTES:
* Not the same form of division as IDIV; rounding is toward negative infinity.
** In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
***See IA-32 Architecture Compatibility section below.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>ModRMr/m (r, w)</td>
<td>1</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MC</td>
<td>ModRMr/m (r, w)</td>
<td>CL</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRMr/m (r, w)</td>
<td>imm8</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
Shifts the bits in the first operand (destination operand) to the left or right by the number of bits specified in the second operand (count operand). Bits shifted beyond the destination operand boundary are first shifted into the CF flag, then discarded. At the end of the shift operation, the CF flag contains the last bit shifted out of the destination operand.

The destination operand can be a register or a memory location. The count operand can be an immediate value or the CL register. The count is masked to 5 bits (or 6 bits if in 64-bit mode and REX.W is used). The count range is limited to 0 to 31 (or 63 if 64-bit mode and REX.W is used). A special opcode encoding is provided for a count of 1.

The shift arithmetic left (SAL) and shift logical left (SHL) instructions perform the same operation; they shift the bits in the destination operand to the left (toward more significant bit locations). For each shift count, the most significant bit of the destination operand is shifted into the CF flag, and the least significant bit is cleared (see Figure 7-7 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1).

The shift arithmetic right (SAR) and shift logical right (SHR) instructions shift the bits of the destination operand to the right (toward less significant bit locations). For each shift count, the least significant bit of the destination operand is shifted into the CF flag, and the most significant bit is either set or cleared depending on the instruction type. The SHR instruction clears the most significant bit (see Figure 7-8 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1); the SAR instruction sets or clears the most significant bit to correspond to the sign (most significant bit) of the original value in the destination operand. In effect, the SAR instruction fills the empty bit position’s shifted value with the sign of the unshifted value (see Figure 7-9 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1).
The SAR and SHR instructions can be used to perform signed or unsigned division, respectively, of the destination operand by powers of 2. For example, using the SAR instruction to shift a signed integer 1 bit to the right divides the value by 2.

Using the SAR instruction to perform a division operation does not produce the same result as the IDIV instruction. The quotient from the IDIV instruction is rounded toward zero, whereas the “quotient” of the SAR instruction is rounded toward negative infinity. This difference is apparent only for negative numbers. For example, when the IDIV instruction is used to divide -9 by 4, the result is -2 with a remainder of -1. If the SAR instruction is used to shift -9 right by two bits, the result is -3 and the “remainder” is +3; however, the SAR instruction stores only the most significant bit of the remainder (in the CF flag).

The OF flag is affected only on 1-bit shifts. For left shifts, the OF flag is set to 0 if the most-significant bit of the result is the same as the CF flag (that is, the top two bits of the original operand were the same); otherwise, it is set to 1. For the SAR instruction, the OF flag is cleared for all 1-bit shifts. For the SHR instruction, the OF flag is set to the most-significant bit of the original operand.

In 64-bit mode, the instruction’s default operation size is 32 bits and the mask width for CL is 5 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64-bits and sets the mask width for CL to 6 bits. See the summary chart at the beginning of this section for encoding data and limits.

**IA-32 Architecture Compatibility**

The 8086 does not mask the shift count. However, all other IA-32 processors (starting with the Intel 286 processor) do mask the shift count to 5 bits, resulting in a maximum count of 31. This masking is done in all operating modes (including the virtual-8086 mode) to reduce the maximum execution time of the instructions.

**Operation**

IF 64-Bit Mode and using REX.W
THEN
countMASK ← 3FH;
ELSE
countMASK ← 1FH;
FI

tempCOUNT ← (COUNT AND countMASK);
tempDEST ← DEST;
WHILE (tempCOUNT ≠ 0)
DO
IF instruction is SAL or SHL
THEN
CF ← MSB(DEST);

SAL/SAR/SHL/SHR—Shift
ELSE (* Instruction is SAR or SHR *)
   CF ← LSB(DEST);
Fl;
IF instruction is SAL or SHL
   THEN
      DEST ← DEST * 2;
ELSE
   IF instruction is SAR
      THEN
         DEST ← DEST / 2; (* Signed divide, rounding toward negative infinity *)
   ELSE (* Instruction is SHR *)
      DEST ← DEST / 2; (* Unsigned divide *)
   Fi;
Fl;
   tempCOUNT ← tempCOUNT - 1;
OD;

(* Determine overflow for the various instructions *)
IF (COUNT and countMASK) = 1
   THEN
      IF instruction is SAL or SHL
         THEN
            OF ← MSB(DEST) XOR CF;
      ELSE
         IF instruction is SAR
            THEN
               OF ← 0;
         ELSE (* Instruction is SHR *)
            OF ← MSB(tempDEST);
      Fi;
Fl;
ELSE IF (COUNT AND countMASK) = 0
   THEN
      All flags unchanged;
ELSE (* COUNT not 1 or 0 *)
   OF ← undefined;
Fi;
Fi;

**Flags Affected**
The CF flag contains the value of the last bit shifted out of the destination operand; it
is undefined for SHL and SHR instructions where the count is greater than or equal to
the size (in bits) of the destination operand. The OF flag is affected only for 1-bit
shifts (see “Description” above); otherwise, it is undefined. The SF, ZF, and PF flags are set according to the result. If the count is 0, the flags are not affected. For a non-zero count, the AF flag is undefined.

**Protected Mode Exceptions**

- **#GP(0)** If the destination is located in a non-writable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS** If a memory operand effective address is outside the SS segment limit.
- **#UD** If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made.
- **#UD** If the LOCK prefix is used.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- **#SS(0)** If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)** If the memory address is in a non-canonical form.
INSTRUCTION SET REFERENCE, M-Z

#PF(fault-code)    If a page fault occurs.
#AC(0)             If alignment checking is enabled and an unaligned memory
                   reference is made while the current privilege level is 3.
#UD                 If the LOCK prefix is used.
## SBB—Integer Subtraction with Borrow

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1C ib</td>
<td>SBB AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow $imm8$ from AL.</td>
</tr>
<tr>
<td>1D iw</td>
<td>SBB AX, imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow $imm16$ from AX.</td>
</tr>
<tr>
<td>1D id</td>
<td>SBB EAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow $imm32$ from EAX.</td>
</tr>
<tr>
<td>REX.W + 1D id</td>
<td>SBB RAX, imm32</td>
<td>I</td>
<td>N.E.</td>
<td></td>
<td>Subtract with borrow sign-extended $imm32$ to 64-bits from RAX.</td>
</tr>
<tr>
<td>80 /3 ib</td>
<td>SBB r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow $imm8$ from $r/m8$.</td>
</tr>
<tr>
<td>REX + 80 /3 ib</td>
<td>SBB r/m8*, imm8</td>
<td>MI</td>
<td>N.E.</td>
<td></td>
<td>Subtract with borrow $imm8$ from $r/m8$.</td>
</tr>
<tr>
<td>81 /3 iw</td>
<td>SBB r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow $imm16$ from $r/m16$.</td>
</tr>
<tr>
<td>81 /3 id</td>
<td>SBB r/m32, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow $imm32$ from $r/m32$.</td>
</tr>
<tr>
<td>REX.W + 81 /3 id</td>
<td>SBB r/m64, imm32</td>
<td>MI</td>
<td>N.E.</td>
<td></td>
<td>Subtract with borrow sign-extended $imm32$ to 64-bits from $r/m64$.</td>
</tr>
<tr>
<td>83 /3 ib</td>
<td>SBB r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow sign-extended $imm8$ from $r/m16$.</td>
</tr>
<tr>
<td>83 /3 ib</td>
<td>SBB r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow sign-extended $imm8$ from $r/m32$.</td>
</tr>
<tr>
<td>REX.W + 83 /3 ib</td>
<td>SBB r/m64, imm8</td>
<td>MI</td>
<td>N.E.</td>
<td></td>
<td>Subtract with borrow sign-extended $imm8$ from $r/m64$.</td>
</tr>
<tr>
<td>18 /r</td>
<td>SBB r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td></td>
<td>Subtract with borrow $r8$ from $r/m8$.</td>
</tr>
<tr>
<td>REX + 18 /r</td>
<td>SBB r/m8*, r8</td>
<td>MR</td>
<td>N.E.</td>
<td></td>
<td>Subtract with borrow $r8$ from $r/m8$.</td>
</tr>
<tr>
<td>19 /r</td>
<td>SBB r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td></td>
<td>Subtract with borrow $r16$ from $r/m16$.</td>
</tr>
<tr>
<td>19 /r</td>
<td>SBB r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td></td>
<td>Subtract with borrow $r32$ from $r/m32$.</td>
</tr>
<tr>
<td>REX.W + 19 /r</td>
<td>SBB r/m64, r64</td>
<td>MR</td>
<td>N.E.</td>
<td></td>
<td>Subtract with borrow $r64$ from $r/m64$.</td>
</tr>
</tbody>
</table>
SBB—Integer Subtraction with Borrow

INSTRUCTION SET REFERENCE, M-Z

**InstructionOperand Encoding**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1A /r</td>
<td>SBB r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow r/m8 from r8.</td>
</tr>
<tr>
<td>REX + 1A /r</td>
<td>SBB r8*, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract with borrow r/m8 from r8.</td>
</tr>
<tr>
<td>1B /r</td>
<td>SBB r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow r/m16 from r16.</td>
</tr>
<tr>
<td>1B /r</td>
<td>SBB r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract with borrow r/m32 from r32.</td>
</tr>
<tr>
<td>REX.W + 1B /r</td>
<td>SBB r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract with borrow r/m64 from r64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Description**

Adds the source operand (second operand) and the carry (CF) flag, and subtracts the result from the destination operand (first operand). The result of the subtraction is stored in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. (However, two memory operands cannot be used in one instruction.) The state of the CF flag represents a borrow from a previous subtraction.

When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The SBB instruction does not distinguish between signed or unsigned operands. Instead, the processor evaluates the result for both data types and sets the OF and CF flags to indicate a borrow in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

The SBB instruction is usually executed as part of a multibyte or multiword subtraction in which a SUB instruction is followed by a SBB instruction.
This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation

\[
\text{DEST} \leftarrow (\text{DEST} - (\text{SRC} + \text{CF}));
\]

Flags Affected

The OF, SF, ZF, AF, PF, and CF flags are set according to the result.

Protected Mode Exceptions

- **#GP(0)**: If the destination is located in a non-writable segment.
- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#GP(0)**: If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD**: If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions

- **#GP**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS**: If a memory operand effective address is outside the SS segment limit.
- **#UD**: If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
INSTRUCTION SET REFERENCE, M-Z

#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
#UD  If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used but the destination is not a memory operand.
SCAS/SCASB/SCASW/SCASD—Scan String

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AE</td>
<td>SCAS m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare AL with byte at ES:(E)DI or RDI, then set status flags.*</td>
</tr>
<tr>
<td>AF</td>
<td>SCAS m16</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare AX with word at ES:(E)DI or RDI, then set status flags.*</td>
</tr>
<tr>
<td>AF</td>
<td>SCAS m32</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare EAX with doubleword at ES:(E)DI or RDI then set status flags.*</td>
</tr>
<tr>
<td>REX.W + AF</td>
<td>SCAS m64</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare RAX with quadword at ES:(E)DI or RDI then set status flags.</td>
</tr>
<tr>
<td>AE</td>
<td>SCASB</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare AL with byte at ES:(E)DI or RDI then set status flags.*</td>
</tr>
<tr>
<td>AF</td>
<td>SCASW</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare AX with word at ES:(E)DI or RDI then set status flags.*</td>
</tr>
<tr>
<td>AF</td>
<td>SCASD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Compare EAX with doubleword at ES:(E)DI or RDI then set status flags.*</td>
</tr>
<tr>
<td>REX.W + AF</td>
<td>SCASQ</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Compare RAX with quadword at RDI or EDI then set status flags.</td>
</tr>
</tbody>
</table>

NOTES:
* In 64-bit mode, only 64-bit (RDI) and 32-bit (EDI) address sizes are supported. In non-64-bit mode, only 32-bit (EDI) and 16-bit (DI) address sizes are supported.

Instruction Operand Encoding

<table>
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<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
In non-64-bit modes and in default 64-bit mode: this instruction compares a byte, word, doubleword or quadword specified using a memory operand with the value in AL, AX, or EAX. It then sets status flags in EFLAGS recording the results. The memory operand address is read from ES:(E)DI register (depending on the address-size
attribute of the instruction and the current operational mode). Note that ES cannot be overridden with a segment override prefix.

At the assembly-code level, two forms of this instruction are allowed. The explicit-operand form and the no-operands form. The explicit-operand form (specified using the SCAS mnemonic) allows a memory operand to be specified explicitly. The memory operand must be a symbol that indicates the size and location of the operand value. The register operand is then automatically selected to match the size of the memory operand (AL register for byte comparisons, AX for word comparisons, EAX for doubleword comparisons). The explicit-operand form is provided to allow documentation. Note that the documentation provided by this form can be misleading. That is, the memory operand symbol must specify the correct type (size) of the operand (byte, word, or doubleword) but it does not have to specify the correct location. The location is always specified by ES:(E)DI.

The no-operands form of the instruction uses a short form of SCAS. Again, ES:(E)DI is assumed to be the memory operand and AL, AX, or EAX is assumed to be the register operand. The size of operands is selected by the mnemonic: SCASB (byte comparison), SCASW (word comparison), or SCASD (doubleword comparison).

After the comparison, the (E)DI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. If the DF flag is 0, the (E)DI register is incremented; if the DF flag is 1, the (E)DI register is decremented. The register is incremented or decremented by 1 for byte operations, by 2 for word operations, and by 4 for doubleword operations.

SCAS, SCASB, SCASW, SCASD, and SCASQ can be preceded by the REP prefix for block comparisons of ECX bytes, words, doublewords, or quadwords. Often, however, these instructions will be used in a LOOP construct that takes some action based on the setting of status flags. See "REP/REPE/REPZ /REPN/REPNZ—Repeat String Operation Prefix" in this chapter for a description of the REP prefix.

In 64-bit mode, the instruction’s default address size is 64-bits, 32-bit address size is supported using the prefix 67H. Using a REX prefix in the form of REX.W promotes operation on doubleword operand to 64 bits. The 64-bit no-operand mnemonic is SCASQ. Address of the memory operand is specified in either RDI or EDI, and AL/AX/EAX/RAX may be used as the register operand. After a comparison, the destination register is incremented or decremented by the current operand size (depending on the value of the DF flag). See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

Non-64-bit Mode:

IF (Byte comparison)
    THEN
        temp ← AL − SRC;
        SetStatusFlags(temp);
        THEN IF DF = 0
THEN (E)DI ← (E)DI + 1;
ELSE (E)DI ← (E)DI - 1; FI;
ELSE IF (Word comparison)
    THEN
        temp ← AX - SRC;
        SetStatusFlags(temp);
        IF DF = 0
            THEN (E)DI ← (E)DI + 2;
            ELSE (E)DI ← (E)DI - 2; FI;
        FI;
    ELSE IF (Doubleword comparison)
        THEN
            temp ← EAX - SRC;
            SetStatusFlags(temp);
            IF DF = 0
                THEN (E)DI ← (E)DI + 4;
                ELSE (E)DI ← (E)DI - 4; FI;
            FI;
        FI;
    FI;

64-bit Mode:

IF (Byte comparison)
    THEN
        temp ← AL - SRC;
        SetStatusFlags(temp);
        THEN IF DF = 0
            THEN (R|E)DI ← (R|E)DI + 1;
            ELSE (R|E)DI ← (R|E)DI - 1; FI;
        ELSE IF (Word comparison)
            THEN
                temp ← AX - SRC;
                SetStatusFlags(temp);
                IF DF = 0
                    THEN (R|E)DI ← (R|E)DI + 2;
                    ELSE (R|E)DI ← (R|E)DI - 2; FI;
                FI;
            ELSE IF (Doubleword comparison)
                THEN
                    temp ← EAX - SRC;
                    SetStatusFlags(temp);
                    IF DF = 0
                        THEN (R|E)DI ← (R|E)DI + 4;
                        ELSE (R|E)DI ← (R|E)DI - 4; FI;
INSTRUCTION SET REFERENCE, M-Z

IF;
ELSE IF (Quadword comparison using REX.W)
THEN
  temp ← RAX − SRC;
  SetStatusFlags(temp);
  IF DF = 0
  THEN (R|E)DI ← (R|E)DI + 8;
  ELSE (R|E)DI ← (R|E)DI − 8;
  Fl;
FI;

Flags Affected
The OF, SF, ZF, AF, PF, and CF flags are set according to the temporary result of the comparison.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the limit of the ES segment.
If the ES register contains a NULL segment selector.
If an illegal memory operand effective address in the ES segment is given.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
**SETcc—Set Byte on Condition**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 97</td>
<td>SETA r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>REX + 0F 97</td>
<td>SETA r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if above (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>0F 93</td>
<td>SETAE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if above or equal (CF=0).</td>
</tr>
<tr>
<td>REX + 0F 93</td>
<td>SETAE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if above or equal (CF=0).</td>
</tr>
<tr>
<td>0F 92</td>
<td>SETB r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if below (CF=1).</td>
</tr>
<tr>
<td>REX + 0F 92</td>
<td>SETB r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if below (CF=1).</td>
</tr>
<tr>
<td>0F 96</td>
<td>SETE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>REX + 0F 96</td>
<td>SETE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if below or equal (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>0F 92</td>
<td>SETC r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if carry (CF=1).</td>
</tr>
<tr>
<td>REX + 0F 92</td>
<td>SETC r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if carry (CF=1).</td>
</tr>
<tr>
<td>0F 94</td>
<td>SETE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if equal (ZF=1).</td>
</tr>
<tr>
<td>REX + 0F 94</td>
<td>SETE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if equal (ZF=1).</td>
</tr>
<tr>
<td>0F 9F</td>
<td>SETG r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>REX + 0F 9F</td>
<td>SETG r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if greater (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>0F 9D</td>
<td>SETGE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if greater or equal (SF=OF).</td>
</tr>
<tr>
<td>REX + 0F 9D</td>
<td>SETGE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if greater or equal (SF=OF).</td>
</tr>
<tr>
<td>0F 9C</td>
<td>SETL r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if less (SF≠ OF).</td>
</tr>
<tr>
<td>REX + 0F 9C</td>
<td>SETL r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if less (SF≠ OF).</td>
</tr>
<tr>
<td>0F 9E</td>
<td>SETLE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if less or equal (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>REX + 0F 9E</td>
<td>SETLE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if less or equal (ZF=1 or SF≠ OF).</td>
</tr>
<tr>
<td>0F 96</td>
<td>SETNA r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not above (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>Opcode</td>
<td>Instruction</td>
<td>Op/En</td>
<td>64-Bit Mode</td>
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<tr>
<td>------------</td>
<td>-------------</td>
<td>-------</td>
<td>-------------</td>
<td>------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>REX + 0F 96</td>
<td>SETNA r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not above (CF=1 or ZF=1).</td>
</tr>
<tr>
<td>OF 92</td>
<td>SETNAE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not above or equal (CF=1).</td>
</tr>
<tr>
<td>REX + 0F 92</td>
<td>SETNAE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not above or equal (CF=1).</td>
</tr>
<tr>
<td>OF 93</td>
<td>SETNB r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not below (CF=0).</td>
</tr>
<tr>
<td>REX + 0F 93</td>
<td>SETNB r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not below (CF=0).</td>
</tr>
<tr>
<td>OF 97</td>
<td>SETNBE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not below or equal (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>REX + 0F 97</td>
<td>SETNBE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not below or equal (CF=0 and ZF=0).</td>
</tr>
<tr>
<td>OF 93</td>
<td>SETNC r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not carry (CF=0).</td>
</tr>
<tr>
<td>REX + 0F 93</td>
<td>SETNC r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not carry (CF=0).</td>
</tr>
<tr>
<td>OF 95</td>
<td>SETNE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not equal (ZF=0).</td>
</tr>
<tr>
<td>REX + 0F 95</td>
<td>SETNE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not equal (ZF=0).</td>
</tr>
<tr>
<td>OF 9E</td>
<td>SETNG r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not greater (ZF=1 or SF≠ OF)</td>
</tr>
<tr>
<td>REX + 0F 9E</td>
<td>SETNG r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not greater (ZF=1 or SF≠ OF)</td>
</tr>
<tr>
<td>OF 9C</td>
<td>SETNGE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not greater or equal (SF≠ OF).</td>
</tr>
<tr>
<td>REX + 0F 9C</td>
<td>SETNGE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not greater or equal (SF≠ OF).</td>
</tr>
<tr>
<td>OF 9D</td>
<td>SETNL r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not less (SF=OF).</td>
</tr>
<tr>
<td>REX + 0F 9D</td>
<td>SETNL r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not less (SF=OF).</td>
</tr>
<tr>
<td>OF 9F</td>
<td>SETNLE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not less or equal (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>REX + 0F 9F</td>
<td>SETNLE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not less or equal (ZF=0 and SF=OF).</td>
</tr>
<tr>
<td>OF 91</td>
<td>SETNO r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not overflow (OF=0).</td>
</tr>
<tr>
<td>REX + 0F 91</td>
<td>SETNO r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not overflow (OF=0).</td>
</tr>
<tr>
<td>OF 9B</td>
<td>SETNP r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not parity (PF=0).</td>
</tr>
</tbody>
</table>
**INSTRUCTION SET REFERENCE, M-Z**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>REX + 0F 9B</td>
<td>SETNP r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not parity (PF=0).</td>
</tr>
<tr>
<td>0F 99</td>
<td>SETNS r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not sign (SF=0).</td>
</tr>
<tr>
<td>REX + 0F 99</td>
<td>SETNS r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not sign (SF=0).</td>
</tr>
<tr>
<td>0F 95</td>
<td>SETNZ r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if not zero (ZF=0).</td>
</tr>
<tr>
<td>REX + 0F 95</td>
<td>SETNZ r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if not zero (ZF=0).</td>
</tr>
<tr>
<td>0F 90</td>
<td>SE7O r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if overflow (OF=1).</td>
</tr>
<tr>
<td>REX + 0F 90</td>
<td>SETO r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if overflow (OF=1).</td>
</tr>
<tr>
<td>0F 9A</td>
<td>SETP r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if parity (PF=1).</td>
</tr>
<tr>
<td>REX + 0F 9A</td>
<td>SETP r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if parity (PF=1).</td>
</tr>
<tr>
<td>0F 9A</td>
<td>SETPE r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if parity even (PF=1).</td>
</tr>
<tr>
<td>REX + 0F 9A</td>
<td>SETPE r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if parity even (PF=1).</td>
</tr>
<tr>
<td>0F 9B</td>
<td>SETPO r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if parity odd (PF=0).</td>
</tr>
<tr>
<td>REX + 0F 9B</td>
<td>SETPO r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if parity odd (PF=0).</td>
</tr>
<tr>
<td>0F 9B</td>
<td>SETS r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if sign (SF=1).</td>
</tr>
<tr>
<td>REX + 0F 9B</td>
<td>SETS r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if sign (SF=1).</td>
</tr>
<tr>
<td>0F 94</td>
<td>SETZ r/m8</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set byte if zero (ZF=1).</td>
</tr>
<tr>
<td>REX + 0F 94</td>
<td>SETZ r/m8*</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set byte if zero (ZF=1).</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Sets the destination operand to 0 or 1 depending on the settings of the status flags (CF, SF, OF, ZF, and PF) in the EFLAGS register. The destination operand points to a byte register or a byte in memory. The condition code suffix (cc) indicates the condition being tested for.
The terms “above” and “below” are associated with the CF flag and refer to the relationship between two unsigned integer values. The terms “greater” and “less” are associated with the SF and OF flags and refer to the relationship between two signed integer values.

Many of the SETcc instruction opcodes have alternate mnemonics. For example, SETG (set byte if greater) and SETNLE (set if not less or equal) have the same opcode and test for the same condition: ZF equals 0 and SF equals OF. These alternate mnemonics are provided to make code more intelligible. Appendix B, “EFLAGS Condition Codes,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, shows the alternate mnemonics for various test conditions.

Some languages represent a logical one as an integer with all bits set. This representation can be obtained by choosing the logically opposite condition for the SETcc instruction, then decrementing the result. For example, to test for overflow, use the SETNO instruction, then decrement the result.

In IA-64 mode, the operand size is fixed at 8 bits. Use of REX prefix enable uniform addressing to additional byte registers. Otherwise, this instruction’s operation is the same as in legacy mode and compatibility mode.

**Operation**

IF condition
   THEN DEST ← 1;
   ELSE DEST ← 0;
FI;

**Flags Affected**

None.

**Protected Mode Exceptions**

- **#GP(0)** If the destination is located in a non-writable segment.
  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  If the DS, ES, FS, or GS register contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
INSTRUCTION SET REFERENCE, M-Z

#SS           If a memory operand effective address is outside the SS segment limit.
#UD           If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0)        If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)        If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD           If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)        If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)        If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#UD           If the LOCK prefix is used.
SFENCE—Store Fence

**Op/En** Operand 1 Operand 2 Operand 3 Operand 4

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a serializing operation on all store-to-memory instructions that were issued prior the SFENCE instruction. This serializing operation guarantees that every store instruction that precedes the SFENCE instruction in program order becomes globally visible before any store instruction that follows the SFENCE instruction. The SFENCE instruction is ordered with respect to store instructions, other SFENCE instructions, any LFENCE and MFENCE instructions, and any serializing instructions (such as the CPUID instruction). It is not ordered with respect to load instructions.

Weakly ordered memory types can be used to achieve higher processor performance through such techniques as out-of-order issue, write-combining, and write-collapsing. The degree to which a consumer of data recognizes or knows that the data is weakly ordered varies among applications and may be unknown to the producer of this data. The SFENCE instruction provides a performance-efficient way of ensuring store ordering between routines that produce weakly-ordered results and routines that consume this data.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

```
Wait_On_Following_Stores_Until(preceding_stores_globally_visible);
```

**Intel C/C++ Compiler Intrinsic Equivalent**

```
void _mm_sfence(void)
```

**Exceptions (All Operating Modes)**

- **#UD** If CPUID.01H:EDX.SSE2[bit 26] = 0.
  
  If the LOCK prefix is used.
SGDT—Store Global Descriptor Table Register

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/T Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 /0</td>
<td>SGDT m</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Store GDTR to m.</td>
</tr>
</tbody>
</table>

**NOTES:**
* See IA-32 Architecture Compatibility section below.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Stores the content of the global descriptor table register (GDTR) in the destination operand. The destination operand specifies a memory location.

In legacy or compatibility mode, the destination operand is a 6-byte memory location. If the operand-size attribute is 16 bits, the limit is stored in the low 2 bytes and the 24-bit base address is stored in bytes 3-5, and byte 6 is zero-filled. If the operand-size attribute is 32 bits, the 16-bit limit field of the register is stored in the low 2 bytes of the memory location and the 32-bit base address is stored in the high 4 bytes.

In IA-32e mode, the operand size is fixed at 8+2 bytes. The instruction stores an 8-byte base and a 2-byte limit.

SGDT is useful only by operating-system software. However, it can be used in application programs without causing an exception to be generated. See "LGD/LIDT—Load Global/Interrupt Descriptor Table Register" in Chapter 3, *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A*, for information on loading the GDTR and IDTR.

**IA-32 Architecture Compatibility**

The 16-bit form of the SGDT is compatible with the Intel 286 processor if the upper 8 bits are not referenced. The Intel 286 processor fills these bits with 1s; the Pentium 4, Intel Xeon, P6 processor family, Pentium, Intel486, and Intel386™ processors fill these bits with 0s.

**Operation**

IF instruction is SGDT

IF OperandSize = 16

THEN

DEST[0:15] ← GDTR(Limit);
DEST[16:39] ← GDTR(Base); (* 24 bits of base address stored *)
DEST[40:47] ← 0;
ELSE IF (32-bit Operand Size)
  DEST[0:15] ← GDTR(Limit);
  DEST[16:47] ← GDTR(Base); (* Full 32-bit base address stored *)
FI;
ELSE (* 64-bit Operand Size *)
  DEST[0:15] ← GDTR(Limit);
  DEST[16:79] ← GDTR(Base); (* Full 64-bit base address stored *)
FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#UD If the destination operand is a register.
  If the LOCK prefix is used.
#GP(0) If the destination is located in a non-writable segment.
  If a memory operand effective address is outside the CS, DS,
  ES, FS, or GS segment limit.
  If the DS, ES, FS, or GS register is used to access memory and it
  contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS
  segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory
  reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
#UD If the destination operand is a register.
  If the LOCK prefix is used.
#GP If a memory operand effective address is outside the CS, DS,
  ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS
  segment limit.

Virtual-8086 Mode Exceptions
#UD If the destination operand is a register.
  If the LOCK prefix is used.

SGDT—Store Global Descriptor Table Register
INSTRUCTION SET REFERENCE, M-Z

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#UD If the destination operand is a register.
If the LOCK prefix is used.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
SHLD—Double Precision Shift Left

**Opcode**

- **0F A4**
  - **Instruction**: SHLD r/m16, r16, imm8
  - **Op/En**: MRI
  - **64-Bit Mode**: Valid
  - **Compat/Leg Mode**: Valid
  - **Description**: Shift r/m16 to left imm8 places while shifting bits from r16 in from the right.
- **0F A5**
  - **Instruction**: SHLD r/m16, r16, CL
  - **Op/En**: MRI
  - **64-Bit Mode**: Valid
  - **Compat/Leg Mode**: Valid
  - **Description**: Shift r/m16 to left CL places while shifting bits from r16 in from the right.
- **0F A4**
  - **Instruction**: SHLD r/m32, r32, imm8
  - **Op/En**: MRI
  - **64-Bit Mode**: Valid
  - **Compat/Leg Mode**: Valid
  - **Description**: Shift r/m32 to left imm8 places while shifting bits from r32 in from the right.
- **REX.W + 0F A4**
  - **Instruction**: SHLD r/m64, r64, imm8
  - **Op/En**: MRI
  - **64-Bit Mode**: Valid
  - **Compat/Leg Mode**: N.E.
  - **Description**: Shift r/m64 to left imm8 places while shifting bits from r64 in from the right.
- **0F A5**
  - **Instruction**: SHLD r/m32, r32, CL
  - **Op/En**: MRC
  - **64-Bit Mode**: Valid
  - **Compat/Leg Mode**: Valid
  - **Description**: Shift r/m32 to left CL places while shifting bits from r32 in from the right.
- **REX.W + 0F A5**
  - **Instruction**: SHLD r/m64, r64, CL
  - **Op/En**: MRC
  - **64-Bit Mode**: Valid
  - **Compat/Leg Mode**: N.E.
  - **Description**: Shift r/m64 to left CL places while shifting bits from r64 in from the right.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MRI</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>MRC</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>CL</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

The SHLD instruction is used for multi-precision shifts of 64 bits or more.

The instruction shifts the first operand (destination operand) to the left the number of bits specified by the third operand (count operand). The second operand (source operand) provides bits to shift in from the right (starting with bit 0 of the destination operand).

The destination operand can be a register or a memory location; the source operand is a register. The count operand is an unsigned integer that can be stored in an immediate byte or in the CL register. If the count operand is CL, the shift count is the logical AND of CL and a count mask. In non-64-bit modes and default 64-bit mode; only bits 0 through 4 of the count are used. This masks the count to a value between 0 and 31. If a count is greater than the operand size, the result is undefined.
If the count is 1 or greater, the CF flag is filled with the last bit shifted out of the destination operand. For a 1-bit shift, the OF flag is set if a sign change occurred; otherwise, it is cleared. If the count operand is 0, flags are not affected.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits (upgrading the count mask to 6 bits). See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF (In 64-Bit Mode and REX.W = 1)
    THEN COUNT ← COUNT MOD 64;
    ELSE COUNT ← COUNT MOD 32;
FI
SIZE ← OperandSize;
IF COUNT = 0
    THEN
        No operation;
    ELSE
        IF COUNT > SIZE
            THEN (* Bad parameters *)
                DEST is undefined;
                CF, OF, SF, ZF, AF, PF are undefined;
            ELSE (* Perform the shift *)
                CF ← BIT[DEST, SIZE – COUNT];
                (* Last bit shifted out on exit *)
                FOR i ← SIZE – 1 DOWN TO COUNT
                    DO
                        Bit(DEST, i) ← Bit(DEST, i – COUNT);
                        OD;
                FOR i ← COUNT – 1 DOWN TO 0
                    DO
                        BIT[DEST, i] ← BIT[SRC, i - COUNT + SIZE];
                        OD;
            FI;
        FI;

**Flags Affected**

If the count is 1 or greater, the CF flag is filled with the last bit shifted out of the destination operand and the SF, ZF, and PF flags are set according to the value of the result. For a 1-bit shift, the OF flag is set if a sign change occurred; otherwise, it is cleared. For shifts greater than 1 bit, the OF flag is undefined. If a shift occurs, the AF
flag is undefined. If the count operand is 0, the flags are not affected. If the count is greater than the operand size, the flags are undefined.

Protected Mode Exceptions

- **#GP(0)**
  - If the destination is located in a non-writable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a NULL segment selector.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

- **#UD**
  - If the LOCK prefix is used.

Real-Address Mode Exceptions

- **#GP**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS**
  - If a memory operand effective address is outside the SS segment limit.

- **#UD**
  - If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

- **#GP(0)**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made.

- **#UD**
  - If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

- **#SS(0)**
  - If a memory address referencing the SS segment is in a non-canonical form.

- **#GP(0)**
  - If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)        If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD             If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, M-Z

SHRD—Double Precision Shift Right

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/ En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AC</td>
<td>SHRD r/m16, r16, imm8</td>
<td>MRI</td>
<td>Valid</td>
<td>Valid</td>
<td>Shift r/m16 to right imm8 places while shifting bits from r16 in from the left.</td>
</tr>
<tr>
<td>0F AD</td>
<td>SHRD r/m16, r16, CL</td>
<td>MRC</td>
<td>Valid</td>
<td>Valid</td>
<td>Shift r/m16 to right CL places while shifting bits from r16 in from the left.</td>
</tr>
<tr>
<td>0F AC</td>
<td>SHRD r/m32, r32, imm8</td>
<td>MRI</td>
<td>Valid</td>
<td>Valid</td>
<td>Shift r/m32 to right imm8 places while shifting bits from r32 in from the left.</td>
</tr>
<tr>
<td>REX.W + 0F AC</td>
<td>SHRD r/m64, r64, imm8</td>
<td>MRI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Shift r/m64 to right imm8 places while shifting bits from r64 in from the left.</td>
</tr>
<tr>
<td>0F AD</td>
<td>SHRD r/m32, r32, CL</td>
<td>MRC</td>
<td>Valid</td>
<td>Valid</td>
<td>Shift r/m32 to right CL places while shifting bits from r32 in from the left.</td>
</tr>
<tr>
<td>REX.W + 0F AD</td>
<td>SHRD r/m64, r64, CL</td>
<td>MRC</td>
<td>Valid</td>
<td>N.E.</td>
<td>Shift r/m64 to right CL places while shifting bits from r64 in from the left.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MRI</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>MRC</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>CL</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

The SHRD instruction is useful for multi-precision shifts of 64 bits or more.

The instruction shifts the first operand (destination operand) to the right the number of bits specified by the third operand (count operand). The second operand (source operand) provides bits to shift in from the left (starting with the most significant bit of the destination operand).

The destination operand can be a register or a memory location; the source operand is a register. The count operand is an unsigned integer that can be stored in an immediate byte or the CL register. If the count operand is CL, the shift count is the logical AND of CL and a count mask. In non-64-bit modes and default 64-bit mode, the width of the count mask is 5 bits. Only bits 0 through 4 of the count register are used (masking the count to a value between 0 and 31). If the count is greater than the operand size, the result is undefined.
INSTRUCTION SET REFERENCE, M-Z

If the count is 1 or greater, the CF flag is filled with the last bit shifted out of the destination operand. For a 1-bit shift, the OF flag is set if a sign change occurred; otherwise, it is cleared. If the count operand is 0, flags are not affected.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits (upgrading the count mask to 6 bits). See the summary chart at the beginning of this section for encoding data and limits.

Operation

IF (In 64-Bit Mode and REX.W = 1)
    THEN COUNT ← COUNT MOD 64;
    ELSE COUNT ← COUNT MOD 32;
FI
SIZE ← OperandSize;
IF COUNT = 0
    THEN
        No operation;
    ELSE
        IF COUNT > SIZE
            THEN (* Bad parameters *)
                DEST is undefined;
                CF, OF, SF, ZF, AF, PF are undefined;
            ELSE (* Perform the shift *)
                CF ← BIT[DEST, COUNT - 1]; (* Last bit shifted out on exit *)
                FOR i ← 0 TO SIZE - 1 - COUNT
                    DO
                        BIT[DEST, i] ← BIT[DEST, i + COUNT];
                        OD;
                FOR i ← SIZE - COUNT TO SIZE - 1
                    DO
                        BIT[DEST,i] ← BIT[SRC, i + COUNT - SIZE];
                        OD;
        FI;
    FI;

Flags Affected

If the count is 1 or greater, the CF flag is filled with the last bit shifted out of the destination operand and the SF, ZF, and PF flags are set according to the value of the result. For a 1-bit shift, the OF flag is set if a sign change occurred; otherwise, it is cleared. For shifts greater than 1 bit, the OF flag is undefined. If a shift occurs, the AF flag is undefined. If the count operand is 0, the flags are not affected. If the count is greater than the operand size, the flags are undefined.
Protected Mode Exceptions
#GP(0)  If the destination is located in a non-writable segment.
        If a memory operand effective address is outside the CS, DS,
        ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register contains a NULL segment
        selector.
#SS(0)  If a memory operand effective address is outside the SS
        segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP  If a memory operand effective address is outside the CS, DS,
     ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS
     segment limit.
#UD  If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0)  If a memory operand effective address is outside the CS, DS,
        ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS
        segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made.
#UD  If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-
        canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory
        reference is made while the current privilege level is 3.
INSTRUCTION SET REFERENCE, M-Z

#UD If the LOCK prefix is used.
SHUFPD—Shuffle Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode*/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F C6 /r ib SHUFPD xmm1, xmm2/m128, imm8</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE2</td>
<td>Shuffle packed double-precision floating-point values selected by imm8 from xmm1 and xmm2/m128 to xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG C6 /r ib VSHUFPD xmm1, xmm2, xmm3/m128, imm8</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Shuffle Packed double-precision floating-point values selected by imm8 from xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG C6 /r ib VSHUFPD ymm1, ymm2, ymm3/m256, imm8</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Shuffle Packed double-precision floating-point values selected by imm8 from ymm2 and ymm3/mem.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Moves either of the two packed double-precision floating-point values from destination operand (first operand) into the low quadword of the destination operand; moves either of the two packed double-precision floating-point values from the source operand into to the high quadword of the destination operand (see Figure 4-18). The select operand (third operand) determines which values are moved to the destination operand.

128-bit Legacy SSE version: The source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The select operand is an 8-bit immediate: bit 0 selects which value is moved from the destination operand to the result (where 0 selects the low quadword and 1 selects the high quadword) and bit 1 selects which value is moved from the source operand to the result. Bits 2 through 7 of the select operand are reserved and must be set to 0.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

Operation

IF SELECT[0] = 0
    THEN DEST[63:0] ← DEST[63:0];
    ELSE DEST[63:0] ← DEST[127:64]; Fl;

IF SELECT[1] = 0
    THEN DEST[127:64] ← SRC[63:0];
    ELSE DEST[127:64] ← SRC[127:64]; Fl;

SHUFPD (128-bit Legacy SSE version)

IF IMM0[0] = 0
    THEN DEST[63:0] ← SRC1[63:0]
    ELSE DEST[63:0] ← SRC1[127:64] Fl;

IF IMM0[1] = 0
    THEN DEST[127:64] ← SRC2[63:0]
ELSE DEST[127:64] ← SRC2[127:64] Fl;
DEST[VLMAX-1:128] (Unmodified)

**VSHUFPD (VEX.128 encoded version)**

IF IMM0[0] = 0
  THEN DEST[63:0] ← SRC1[63:0]
ELSE DEST[63:0] ← SRC1[127:64] Fl;
IF IMM0[1] = 0
  THEN DEST[127:64] ← SRC2[63:0]
ELSE DEST[127:64] ← SRC2[127:64] Fl;
DEST[VLMAX-1:128] ← 0

**VSHUFPD (VEX.256 encoded version)**

IF IMM0[0] = 0
  THEN DEST[63:0] ← SRC1[63:0]
ELSE DEST[63:0] ← SRC1[127:64] Fl;
IF IMM0[1] = 0
  THEN DEST[127:64] ← SRC2[63:0]
ELSE DEST[127:64] ← SRC2[127:64] Fl;
IF IMM0[2] = 0
IF IMM0[3] = 0

**Intel C/C++ Compiler Intrinsic Equivalent**

SHUFPD: __m128d _mm_shuffle_pd(__m128d a, __m128d b, unsigned int imm8)
VSHUFPD: __m256d _mm256_shuffle_pd (__m256d a, __m256d b, const int select);

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4.
INSTRUCTION SET REFERENCE, M-Z

SHUFPS—Shuffle Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode*/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C6 /r ib SHUFPS xmm1, xmm2/m128, imm8</td>
<td>RMI</td>
<td>V/V</td>
<td>SSE</td>
<td>Shuffle packed single-precision floating-point values selected by <code>imm8</code> from <code>xmm1</code> and <code>xmm1/m128</code> to <code>xmm1</code>.</td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG C6 /r ib VSHUFPS xmm1, xmm2, xmm3/m128, imm8</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Shuffle Packed single-precision floating-point values selected by <code>imm8</code> from <code>xmm2</code> and <code>xmm3/mem</code>.</td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG C6 /r ib VSHUFPS ymm1, ymm2, ymm3/m256, imm8</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Shuffle Packed single-precision floating-point values selected by <code>imm8</code> from <code>ymm2</code> and <code>ymm3/mem</code>.</td>
</tr>
</tbody>
</table>

InstructionOperand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMI</td>
<td>ModRM reg (r, w)</td>
<td>ModRM r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
<tr>
<td>RVMI</td>
<td>ModRM reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Moves two of the four packed single-precision floating-point values from the destination operand (first operand) into the low quadword of the destination operand; moves two of the four packed single-precision floating-point values from the source operand (second operand) into to the high quadword of the destination operand (see Figure 4-19). The select operand (third operand) determines which values are moved to the destination operand.

128-bit Legacy SSE version: The source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed. determines which values are moved to the destination operand.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. The select operand is an 8-bit immediate: bits 0 and 1 select the value to be moved from the destination operand to the low doubleword of the result, bits 2 and 3 select the value to be moved from the destination operand to the second double word of the result, bits 4 and 5 select the value to be moved from the source operand to the third doubleword of the result, and bits 6 and 7 select the value to be moved from the source operand to the high doubleword of the result.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

**Operation**

```
CASE (SELECT[1:0]) OF
  0: DEST[31:0] ← DEST[31:0];
  1: DEST[31:0] ← DEST[63:32];
  2: DEST[31:0] ← DEST[95:64];
  3: DEST[31:0] ← DEST[127:96];
ESAC;

CASE (SELECT[3:2]) OF
  0: DEST[63:32] ← DEST[31:0];
  1: DEST[63:32] ← DEST[63:32];
  2: DEST[63:32] ← DEST[95:64];
```
ESAC;

CASE (SELECT[5:4]) OF
  0: DEST[95:64] ← SRC[31:0];
  1: DEST[95:64] ← SRC[63:32];
  2: DEST[95:64] ← SRC[95:64];
  3: DEST[95:64] ← SRC[127:96];
ESAC;

CASE (SELECT[7:6]) OF
  0: DEST[127:96] ← SRC[31:0];
  1: DEST[127:96] ← SRC[63:32];
  2: DEST[127:96] ← SRC[95:64];
  3: DEST[127:96] ← SRC[127:96];
ESAC;

SHUFPS (128-bit Legacy SSE version)
DEST[31:0] ← Select4(SRC1[127:0], imm8[1:0]);
DEST[63:32] ← Select4(SRC1[127:0], imm8[3:2]);
DEST[95:64] ← Select4(SRC2[127:0], imm8[5:4]);
DEST[127:96] ← Select4(SRC2[127:0], imm8[7:6]);
DEST[VLMAX-1:128] (Unmodified)

VSHUFPS (VEX.128 encoded version)
DEST[31:0] ← Select4(SRC1[127:0], imm8[1:0]);
DEST[63:32] ← Select4(SRC1[127:0], imm8[3:2]);
DEST[95:64] ← Select4(SRC2[127:0], imm8[5:4]);
DEST[127:96] ← Select4(SRC2[127:0], imm8[7:6]);
DEST[VLMAX-1:128] ← 0

VSHUFPS (VEX.256 encoded version)
DEST[31:0] ← Select4(SRC1[127:0], imm8[1:0]);
DEST[63:32] ← Select4(SRC1[127:0], imm8[3:2]);
DEST[95:64] ← Select4(SRC2[127:0], imm8[5:4]);
DEST[127:96] ← Select4(SRC2[127:0], imm8[7:6]);
DEST[159:128] ← Select4(SRC1[255:128], imm8[1:0]);
DEST[255:224] ← Select4(SRC2[255:128], imm8[7:6]);

Intel C/C++ Compiler Intrinsic Equivalent
SHUFPS:  __m128 _mm_shuffle_ps(__m128 a, __m128 b, unsigned int imm8)
VSHUFPS:  __m256 _mm256_shuffle_ps (__m256 a, __m256 b, const int select);
**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4.
SIDT—Store Interrupt Descriptor Table Register

Stores the content of the interrupt descriptor table register (IDTR) in the destination operand. The destination operand specifies a 6-byte memory location.

In non-64-bit modes, if the operand-size attribute is 32 bits, the 16-bit limit field of the register is stored in the low 2 bytes of the memory location and the 32-bit base address is stored in the high 4 bytes. If the operand-size attribute is 16 bits, the limit is stored in the low 2 bytes and the 24-bit base address is stored in the third, fourth, and fifth byte, with the sixth byte filled with 0s.

In 64-bit mode, the operand size is fixed at 8+2 bytes. The instruction stores 8-byte base and 2-byte limit values.

SIDT is only useful in operating-system software; however, it can be used in application programs without causing an exception to be generated. See “LGDT/LIDT—Load Global/Interrupt Descriptor Table Register” in Chapter 3, *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A*, for information on loading the GDTR and IDTR.

**IA-32 Architecture Compatibility**

The 16-bit form of SIDT is compatible with the Intel 286 processor if the upper 8 bits are not referenced. The Intel 286 processor fills these bits with 1s; the Pentium 4, Intel Xeon, P6 processor family, Pentium, Intel486, and Intel386 processors fill these bits with 0s.

**Operation**

If instruction is SIDT

Then

If OperandSize = 16

Then

DEST[0:15] ← IDTR(Limit);
DEST[16:39] ← IDTR(Base); (* 24 bits of base address stored; *)
DEST[40:47] ← 0;

Description

Stores the content of the interrupt descriptor table register (IDTR) in the destination operand. The destination operand specifies a 6-byte memory location.

In non-64-bit modes, if the operand-size attribute is 32 bits, the 16-bit limit field of the register is stored in the low 2 bytes of the memory location and the 32-bit base address is stored in the high 4 bytes. If the operand-size attribute is 16 bits, the limit is stored in the low 2 bytes and the 24-bit base address is stored in the third, fourth, and fifth byte, with the sixth byte filled with 0s.

In 64-bit mode, the operand size is fixed at 8+2 bytes. The instruction stores 8-byte base and 2-byte limit values.

SIDT is only useful in operating-system software; however, it can be used in application programs without causing an exception to be generated. See “LGDT/LIDT—Load Global/Interrupt Descriptor Table Register” in Chapter 3, *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A*, for information on loading the GDTR and IDTR.

**IA-32 Architecture Compatibility**

The 16-bit form of SIDT is compatible with the Intel 286 processor if the upper 8 bits are not referenced. The Intel 286 processor fills these bits with 1s; the Pentium 4, Intel Xeon, P6 processor family, Pentium, Intel486, and Intel386 processors fill these bits with 0s.

**Operation**

If instruction is SIDT

Then

If OperandSize = 16

Then

DEST[0:15] ← IDTR(Limit);
DEST[16:39] ← IDTR(Base); (* 24 bits of base address stored; *)
DEST[40:47] ← 0;
ELSE IF (32-bit Operand Size)
    DEST[0:15] ← IDTR(Limit);
    DEST[16:47] ← IDTR(Base); (* Full 32-bit base address stored *)
ELSE (* 64-bit Operand Size *)
    DEST[0:15] ← IDTR(Limit);
    DEST[16:79] ← IDTR(Base); (* Full 64-bit base address stored *)
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
     If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
     If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.
Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#UD If the destination operand is a register.
     If the LOCK prefix is used.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
SLDT—Store Local Descriptor Table Register

<table>
<thead>
<tr>
<th>Opcode*</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compartment Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /0</td>
<td>SLDT r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Stores segment selector from LDTR in r/m16.</td>
</tr>
<tr>
<td>REX.W + 0F 00 /0</td>
<td>SLDT r64/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Stores segment selector from LDTR in r64/m16.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRm/r/m (w)</td>
<td>LDTR</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Stores the segment selector from the local descriptor table register (LDTR) in the destination operand. The destination operand can be a general-purpose register or a memory location. The segment selector stored with this instruction points to the segment descriptor (located in the GDT) for the current LDT. This instruction can only be executed in protected mode.

Outside IA-32e mode, when the destination operand is a 32-bit register, the 16-bit segment selector is copied into the low-order 16 bits of the register. The high-order 16 bits of the register are cleared for the Pentium 4, Intel Xeon, and P6 family processors. They are undefined for Pentium, Intel486, and Intel386 processors. When the destination operand is a memory location, the segment selector is written to memory as a 16-bit quantity, regardless of the operand size.

In compatibility mode, when the destination operand is a 32-bit register, the 16-bit segment selector is copied into the low-order 16 bits of the register. The high-order 16 bits of the register are cleared. When the destination operand is a memory location, the segment selector is written to memory as a 16-bit quantity, regardless of the operand size.

In 64-bit mode, using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). The behavior of SLDT with a 64-bit register is to zero-extend the 16-bit selector and store it in the register. If the destination is memory and operand size is 64, SLDT will write the 16-bit selector to memory as a 16-bit quantity, regardless of the operand size.

Operation

DEST ← LDTR(SegmentSelector);

Flags Affected

None.

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Protected Mode Exceptions

#GP(0)  If the destination is located in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions

#UD  The SLDT instruction is not recognized in real-address mode.
If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#UD  The SLDT instruction is not recognized in virtual-8086 mode.
If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used.
SMSW—Store Machine Status Word

Stores the machine status word (bits 0 through 15 of control register CR0) into the destination operand. The destination operand can be a general-purpose register or a memory location.

In non-64-bit modes, when the destination operand is a 32-bit register, the low-order 16 bits of register CR0 are copied into the low-order 16 bits of the register and the high-order 16 bits are undefined. When the destination operand is a memory location, the low-order 16 bits of register CR0 are written to memory as a 16-bit quantity, regardless of the operand size.

In 64-bit mode, the behavior of the SMSW instruction is defined by the following examples:
- SMSW r16 operand size 16, store CR0[15:0] in r16
- SMSW r32 operand size 32, zero-extend CR0[31:0], and store in r32
- SMSW r64 operand size 64, zero-extend CR0[63:0], and store in r64
- SMSW m16 operand size 16, store CR0[15:0] in m16
- SMSW m16 operand size 32, store CR0[15:0] in m16 (not m32)
- SMSW m16 operands size 64, store CR0[15:0] in m16 (not m64)

SMSW is only useful in operating-system software. However, it is not a privileged instruction and can be used in application programs. The is provided for compatibility with the Intel 286 processor. Programs and procedures intended to run on the
Pentium 4, Intel Xeon, P6 family, Pentium, Intel486, and Intel386 processors should use the MOV (control registers) instruction to load the machine status word.

See "Changes to Instruction Behavior in VMX Non-Root Operation" in Chapter 25 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, for more information about the behavior of this instruction in VMX non-root operation.

**Operation**

\[
\text{DEST} \leftarrow \text{CR0}[15:0];
\]

(* Machine status word *)

**Flags Affected**

None.

**Protected Mode Exceptions**

- **#GP(0)** If the destination is located in a non-writable segment.
- If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#UD** If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
SQRTPD—Compute Square Roots of Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 51 /r SQRTPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Computes square roots of the packed double-precision floating-point values in xmm2/m128 and stores the results in xmm1.</td>
</tr>
<tr>
<td>VEX.128.66.0F:WIG 51 /r VSQRTPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes Square Roots of the packed double-precision floating-point values in xmm2/m128 and stores the result in xmm1.</td>
</tr>
<tr>
<td>VEX.256.66.0F:WIG 51/r VSQRTPD ymm1, ymm2/m256</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes Square Roots of the packed double-precision floating-point values in ymm2/m256 and stores the result in ymm1.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction Operand Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Op/En</td>
</tr>
<tr>
<td>RM</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD computation of the square roots of the two packed double-precision floating-point values in the source operand (second operand) stores the packed double-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 11-3 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a SIMD double-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.
SQRTPD—Compute Square Roots of Packed Double-Precision Floating-Point Values

VEX.128 encoded version: the source operand second source operand or a 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

Operation

**SQRTPD (128-bit Legacy SSE version)**

\[
\text{DEST}[63:0] \leftarrow \text{SQRT} (\text{SRC}[63:0]) \\
\text{DEST}[127:64] \leftarrow \text{SQRT} (\text{SRC}[127:64]) \\
\text{DEST}[VLMAX-1:128] \leftarrow \text{(Unmodified)}
\]

**VSQRTPD (VEX.128 encoded version)**

\[
\text{DEST}[63:0] \leftarrow \text{SQRT} (\text{SRC}[63:0]) \\
\text{DEST}[127:64] \leftarrow \text{SQRT} (\text{SRC}[127:64]) \\
\text{DEST}[VLMAX-1:128] \leftarrow 0
\]

**VSQRTPD (VEX.256 encoded version)**

\[
\text{DEST}[63:0] \leftarrow \text{SQRT} (\text{SRC}[63:0]) \\
\text{DEST}[127:64] \leftarrow \text{SQRT} (\text{SRC}[127:64]) \\
\text{DEST}[191:128] \leftarrow \text{SQRT} (\text{SRC}[191:128]) \\
\text{DEST}[255:192] \leftarrow \text{SQRT} (\text{SRC}[255:192])
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

\[
\text{SQRTPD: } \_\_m128d \_\_mm\_sqrt\_pd (m128d a) \\
\text{SQRTPD: } \_\_m256d \_\_mm256\_sqrt\_pd (\_\_m256d a);
\]

**SIMD Floating-Point Exceptions**

Invalid, Precision, Denormal.

**Other Exceptions**

See Exceptions Type 2; additionally

#UD If VEX.vvvv != 1111B.
SQRTPS—Compute Square Roots of Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode*/ Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 51 /r SQRTPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Computes square roots of the packed single-precision floating-point values in xmm2/m128 and stores the results in xmm1.</td>
</tr>
<tr>
<td>VEX.128.0F.WIG 51 /r VSQRTPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes Square Roots of the packed single-precision floating-point values in xmm2/m128 and stores the result in xmm1.</td>
</tr>
<tr>
<td>VEX.256.0F.WIG 51/r VSQRTPS ymm1, ymm2/m256</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes Square Roots of the packed single-precision floating-point values in ymm2/m256 and stores the result in ymm1.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a SIMD computation of the square roots of the four packed single-precision floating-point values in the source operand (second operand) stores the packed single-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 10-5 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an illustration of a SIMD single-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.
VEX.128 encoded version: the source operand second source operand or a 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The source operand is a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

**Operation**

**SQRTPS (128-bit Legacy SSE version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{SQRT}(\text{SRC}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{SQRT}(\text{SRC}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{SQRT}(\text{SRC}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{SQRT}(\text{SRC}[127:96]) \\
\text{DEST}[\text{VLMAX}-1:128] & \leftarrow 0
\end{align*}
\]

**VSQRTPS (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{SQRT}(\text{SRC}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{SQRT}(\text{SRC}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{SQRT}(\text{SRC}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{SQRT}(\text{SRC}[127:96]) \\
\text{DEST}[\text{VLMAX}-1:128] & \leftarrow 0
\end{align*}
\]

**VSQRTPS (VEX.256 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{SQRT}(\text{SRC}[31:0]) \\
\text{DEST}[63:32] & \leftarrow \text{SQRT}(\text{SRC}[63:32]) \\
\text{DEST}[95:64] & \leftarrow \text{SQRT}(\text{SRC}[95:64]) \\
\text{DEST}[127:96] & \leftarrow \text{SQRT}(\text{SRC}[127:96]) \\
\text{DEST}[159:128] & \leftarrow \text{SQRT}(\text{SRC}[159:128]) \\
\text{DEST}[191:160] & \leftarrow \text{SQRT}(\text{SRC}[191:160]) \\
\text{DEST}[223:192] & \leftarrow \text{SQRT}(\text{SRC}[223:192]) \\
\text{DEST}[255:224] & \leftarrow \text{SQRT}(\text{SRC}[255:224])
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

\begin{align*}
\text{SQRTPS:} & \quad \_m128 \_mm\_sqrt\_ps(\_m128 \text{a}) \\
\text{SQRTPS:} & \quad \_m256 \_mm256\_sqrt\_ps(\_m256 \text{a})
\end{align*}

**SIMD Floating-Point Exceptions**

Invalid, Precision, Denormal.
Other Exceptions
See Exceptions Type 2; additionally
#UD If VEX.vvvv != 1111B.
**SQRTSD—Compute Square Root of Scalar Double-Precision Floating-Point Value**

<table>
<thead>
<tr>
<th>Opcode* Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 51 /r SQRTSD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>xmm1, xmm2/m64</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Computes square root of the low double-precision floating-point value in xmm2/m64 and stores the results in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F.WIG 51/V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSQRTSD xmm1,xmm2, xmm3/m64</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes square root of the low double-precision floating-point value in xmm3/m64 and stores the results in xmm2. Also, upper double precision floating-point value (bits[127:64]) from xmm2 is copied to xmm1[127:64].</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv v</td>
<td>ModRMreg/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Computes the square root of the low double-precision floating-point value in the source operand (second operand) and stores the double-precision floating-point result in the destination operand. The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. The high quad-word of the destination operand remains unchanged. See Figure 11-4 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an illustration of a scalar double-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.
Operation

**SQRTSD (128-bit Legacy SSE version)**
DEST[63:0] ← SQRT(SRC[63:0])
DEST[VLMAX-1:64] (Unmodified)

**VSQRTSD (VEX.128 encoded version)**
DEST[63:0] ← SQRT(SRC2[63:0])
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**
SQRTSD: __m128d _mm_sqrt_sd (m128d a, m128d b)

**SIMD Floating-Point Exceptions**
Invalid, Precision, Denormal.

**Other Exceptions**
See Exceptions Type 3.
INSTRUCTION SET REFERENCE, M-Z

**SQRTSS—Compute Square Root of Scalar Single-Precision Floating-Point Value**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode</th>
<th>CPUID Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F 51 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Computes square root of the low single-precision floating-point value in xmm2/m32 and stores the results in xmm1.</td>
</tr>
<tr>
<td>SQRTSS xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F3.0F.WIG 51</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Computes square root of the low single-precision floating-point value in xmm3/m32 and stores the results in xmm1. Also, upper single precision floating-point values (bits[127:32]) from xmm2 are copied to xmm1[127:32].</td>
</tr>
<tr>
<td>VSQRTSS xmm1, xmm2, xmm3/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Computes the square root of the low single-precision floating-point value in the source operand (second operand) and stores the single-precision floating-point result in the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The three high-order doublewords of the destination operand remain unchanged. See Figure 10-6 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a scalar single-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The first source operand and the destination operand are the same. Bits (VLMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (VLMAX-1:128) of the destination YMM register are zeroed.
Operation

SQRTSS (128-bit Legacy SSE version)
DEST[31:0] ← SQRT(SRC2[31:0])
DEST[VLMAX-1:32] (Unmodified)

VSQRTSS (VEX.128 encoded version)
DEST[31:0] ← SQRT(SRC2[31:0])
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
SQRTSS: __m128 _mm_sqrt_ss(__m128 a)

SIMD Floating-Point Exceptions
Invalid, Precision, Denormal.

Other Exceptions
See Exceptions Type 3.
STC—Set Carry Flag

**Description**
Sets the CF flag in the EFLAGS register.
This instruction's operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

\[ CF \leftarrow 1; \]

**Flags Affected**
The CF flag is set. The OF, ZF, SF, AF, and PF flags are unaffected.

**Exceptions (All Operating Modes)**

#UD If the LOCK prefix is used.
**STD—Set Direction Flag**

<table>
<thead>
<tr>
<th>Operation</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FD</td>
<td>STD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Set DF flag.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Sets the DF flag in the EFLAGS register. When the DF flag is set to 1, string operations decrement the index registers (ESI and/or EDI).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

DF ← 1;

**Flags Affected**

The DF flag is set. The CF, OF, ZF, SF, AF, and PF flags are unaffected.

**Exceptions (All Operating Modes)**

#UD If the LOCK prefix is used.
STI—Set Interrupt Flag

If protected-mode virtual interrupts are not enabled, STI sets the interrupt flag (IF) in the EFLAGS register. After the IF flag is set, the processor begins responding to external, maskable interrupts after the next instruction is executed. The delayed effect of this instruction is provided to allow interrupts to be enabled just before returning from a procedure (or subroutine). For instance, if an STI instruction is followed by an RET instruction, the RET instruction is allowed to execute before external interrupts are recognized. If the STI instruction is followed by a CLI instruction (which clears the IF flag), the effect of the STI instruction is negated.

The IF flag and the STI and CLI instructions do not prohibit the generation of exceptions and NMI interrupts. NMI interrupts (and SMIs) may be blocked for one macro-instruction following an STI.

When protected-mode virtual interrupts are enabled, CPL is 3, and IOPL is less than 3; STI sets the VIF flag in the EFLAGS register, leaving IF unaffected.

Table 4-18 indicates the action of the STI instruction depending on the processor’s mode of operation and the CPL/IOPL settings of the running program or procedure.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

1. The STI instruction delays recognition of interrupts only if it is executed with EFLAGS.IF = 0. In a sequence of STI instructions, only the first instruction in the sequence is guaranteed to delay interrupts.

In the following instruction sequence, interrupts may be recognized before RET executes:

   STI
   STI
   RET
STI—Set Interrupt Flag

Operation

IF PE = 0 (* Executing in real-address mode *)
   THEN
       IF ← 1; (* Set Interrupt Flag *)
   ELSE (* Executing in protected mode or virtual-8086 mode *)
       IF VM = 0 (* Executing in protected mode*)
           THEN
               IF IOPL ≥ CPL
                   THEN
                       IF ← 1; (* Set Interrupt Flag *)
                   ELSE
                       IF (IOPL < CPL) and (CPL = 3) and (VIP = 0)
                           THEN
                               VIF ← 1; (* Set Virtual Interrupt Flag *)
                           ELSE
                               #GP(0);
                   FI;
               FI;
       ELSE (* Executing in virtual-8086 mode *)
           IF IOPL = 3
               THEN
                   IF ← 1; (* Set Interrupt Flag *)
           ELSE
               IF ((IOPL < 3) and (VIP = 0) and (VME = 1))
                   THEN

Table 4-18. Decision Table for STI Results

<table>
<thead>
<tr>
<th>PE</th>
<th>VM</th>
<th>IOPL</th>
<th>CPL</th>
<th>PVI</th>
<th>VIP</th>
<th>VME</th>
<th>STI Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>≥ CPL</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>VIF = 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>GP Fault</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>GP Fault</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>&lt; CPL</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>GP Fault</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>IF = 1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>VIF = 1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>GP Fault</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>&lt; 3</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>GP Fault</td>
</tr>
</tbody>
</table>

NOTES:
X = This setting has no impact.
STI—Set Interrupt Flag

```
STI—Set Interrupt Flag

VIF ← 1; (* Set Virtual Interrupt Flag *)
ELSE
#GP(0); (* Trap to virtual-8086 monitor *)
FI;
FI;
FI;
FI;
FI;
```

**Flags Affected**
The IF flag is set to 1; or the VIF flag is set to 1.

**Protected Mode Exceptions**

- **#GP(0)** If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#UD** If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**
Same exceptions as in protected mode.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
Same exceptions as in protected mode.
STMXCSR—Store MXCSR Register State

<table>
<thead>
<tr>
<th>Opcode*/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /3 STMXCSR m32</td>
<td>M</td>
<td>V/V</td>
<td>SSE</td>
<td>Store contents of MXCSR register to m32.</td>
</tr>
<tr>
<td>VEX.LZ.0F:WIG AE /3</td>
<td>M</td>
<td>V/V</td>
<td>AVX</td>
<td>Store contents of MXCSR register to m32.</td>
</tr>
<tr>
<td>VSTMXCSR m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Description
Stores the contents of the MXCSR control and status register to the destination operand. The destination operand is a 32-bit memory location. The reserved bits in the MXCSR register are stored as 0s.
This instruction’s operation is the same in non-64-bit modes and 64-bit mode.
VEX.L must be 0, otherwise instructions will #UD.
Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

Operation
m32 ← MXCSR;

Intel C/C++ Compiler Intrinsic Equivalent
_mm_getcsr(void)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 5; additionally
#UD If VEX.L= 1,
   If VEX.vvvv != 1111B.
## STOS/STOSB/STOSW/STOSD/STOSQ—Store String

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA</td>
<td>STOS (m8)</td>
<td>NA</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, store AL at address ES:(E)DI; For 64-bit mode store AL at address RDI or EDI.</td>
</tr>
<tr>
<td>AB</td>
<td>STOS (m16)</td>
<td>NA</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, store AX at address ES:(E)DI; For 64-bit mode store AX at address RDI or EDI.</td>
</tr>
<tr>
<td>AB</td>
<td>STOS (m32)</td>
<td>NA</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, store EAX at address ES:(E)DI; For 64-bit mode store EAX at address RDI or EDI.</td>
</tr>
<tr>
<td>REX.W + AB</td>
<td>STOS (m64)</td>
<td>NA</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store RAX at address RDI or EDI.</td>
</tr>
<tr>
<td>AA</td>
<td>STOSB</td>
<td>NA</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, store AL at address ES:(E)DI; For 64-bit mode store AL at address RDI or EDI.</td>
</tr>
<tr>
<td>AB</td>
<td>STOSW</td>
<td>NA</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, store AX at address ES:(E)DI; For 64-bit mode store AX at address RDI or EDI.</td>
</tr>
<tr>
<td>AB</td>
<td>STOSD</td>
<td>NA</td>
<td>Valid</td>
<td>Valid</td>
<td>For legacy mode, store EAX at address ES:(E)DI; For 64-bit mode store EAX at address RDI or EDI.</td>
</tr>
<tr>
<td>REX.W + AB</td>
<td>STOSQ</td>
<td>NA</td>
<td>Valid</td>
<td>N.E.</td>
<td>Store RAX at address RDI or EDI.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

In non-64-bit and default 64-bit mode; stores a byte, word, or doubleword from the AL, AX, or EAX register (respectively) into the destination operand. The destination operand is a memory location, the address of which is read from either the ES:EDI or ES:DI register (depending on the address-size attribute of the instruction and the
mode of operation). The ES segment cannot be overridden with a segment override prefix.

At the assembly-code level, two forms of the instruction are allowed: the "explicit-operands" form and the "no-operands" form. The explicit-operands form (specified with the STOS mnemonic) allows the destination operand to be specified explicitly. Here, the destination operand should be a symbol that indicates the size and location of the destination value. The source operand is then automatically selected to match the size of the destination operand (the AL register for byte operands, AX for word operands, EAX for doubleword operands). The explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the destination operand symbol must specify the correct type (size) of the operand (byte, word, or doubleword), but it does not have to specify the correct location. The location is always specified by the ES:(E)DI register. These must be loaded correctly before the store string instruction is executed.

The no-operands form provides "short forms" of the byte, word, doubleword, and quadword versions of the STOS instructions. Here also ES:(E)DI is assumed to be the destination operand and AL, AX, or EAX is assumed to be the source operand. The size of the destination and source operands is selected by the mnemonic: STOSB (byte read from register AL), STOSW (word from AX), STOSD (doubleword from EAX).

After the byte, word, or doubleword is transferred from the register to the memory location, the (E)DI register is incremented or decremented according to the setting of the DF flag in the EFLAGS register. If the DF flag is 0, the register is incremented; if the DF flag is 1, the register is decremented (the register is incremented or decremented by 1 for byte operations, by 2 for word operations, by 4 for doubleword operations).

In 64-bit mode, the default address size is 64 bits, 32-bit address size is supported using the prefix 67H. Using a REX prefix in the form of REX.W promotes operation on doubleword operand to 64 bits. The promoted no-operand mnemonic is STOSQ. STOSQ (and its explicit operands variant) store a quadword from the RAX register into the destination addressed by RDI or EDI. See the summary chart at the beginning of this section for encoding data and limits.

The STOS, STOSB, STOSW, STOSD, STOSQ instructions can be preceded by the REP prefix for block loads of ECX bytes, words, or doublewords. More often, however, these instructions are used within a LOOP construct because data needs to be moved into the AL, AX, or EAX register before it can be stored. See "REP/REPE/REPZ /REPNE/REPNZ—Repeat String Operation Prefix" in this chapter for a description of the REP prefix.

**Operation**

Non-64-bit Mode:

IF (Byte store)
THEN
DEST ← AL;
THEN IF DF = 0
THEN (E)DI ← (E)DI + 1;
ELSE (E)DI ← (E)DI − 1;
FI;
ELSE IF (Word store)
THEN
DEST ← AX;
THEN IF DF = 0
THEN (E)DI ← (E)DI + 2;
ELSE (E)DI ← (E)DI − 2;
FI;
ELSE IF (Doubleword store)
THEN
DEST ← EAX;
THEN IF DF = 0
THEN (E)DI ← (E)DI + 4;
ELSE (E)DI ← (E)DI − 4;
FI;
FI;

64-bit Mode:
IF (Byte store)
THEN
DEST ← AL;
THEN IF DF = 0
THEN (R|E)DI ← (R|E)DI + 1;
ELSE (R|E)DI ← (R|E)DI − 1;
FI;
ELSE IF (Word store)
THEN
DEST ← AX;
THEN IF DF = 0
THEN (R|E)DI ← (R|E)DI + 2;
ELSE (R|E)DI ← (R|E)DI − 2;
FI;
ELSE IF (Doubleword store)
THEN
DEST ← EAX;
THEN IF DF = 0
THEN (R|E)DI ← (R|E)DI + 4;
ELSE (R|E)DI ← (R|E)DI - 4;
FI;
ELSE IF (Quadword store using REX.W )
THEN
DEST ← RAX;
THEN IF DF = 0
THEN (R|E)DI ← (R|E)DI + 8;
ELSE (R|E)DI ← (R|E)DI - 8;
FI;
FI;
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the destination is located in a non-writable segment.
If a memory operand effective address is outside the limit of the ES segment.
If the ES register contains a NULL segment selector.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the ES segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the ES segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If the LOCK prefix is used.
**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
- **#GP(0)** If the memory address is in a non-canonical form.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- **#UD** If the LOCK prefix is used.
STR—Store Task Register

Stores the segment selector from the task register (TR) in the destination operand. The destination operand can be a general-purpose register or a memory location. The segment selector stored with this instruction points to the task state segment (TSS) for the currently running task.

When the destination operand is a 32-bit register, the 16-bit segment selector is copied into the lower 16 bits of the register and the upper 16 bits of the register are cleared. When the destination operand is a memory location, the segment selector is written to memory as a 16-bit quantity, regardless of operand size.

In 64-bit mode, operation is the same. The size of the memory operand is fixed at 16 bits. In register stores, the 2-byte TR is zero extended if stored to a 64-bit register.

The STR instruction is useful only in operating-system software. It can only be executed in protected mode.

Operation

\[
\text{DEST} \leftarrow \text{TR} \left( \text{SegmentSelector} \right);
\]

Flags Affected

None.

Protected Mode Exceptions

- #GP(0) If the destination is a memory operand that is located in a non-writable segment or if the effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0) If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.
- #PF(fault-code) If a page fault occurs.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Stores segment selector from the task register (TR) in the destination operand.
STR—Store Task Register

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD  The STR instruction is not recognized in real-address mode.

Virtual-8086 Mode Exceptions
#UD  The STR instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#GP(0)  If the memory address is in a non-canonical form.
#SS(U)  If the stack address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD  If the LOCK prefix is used.
## SUB—Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2C ib</td>
<td>SUB AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract imm8 from AL.</td>
</tr>
<tr>
<td>2D iw</td>
<td>SUB AX, imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract imm16 from AX.</td>
</tr>
<tr>
<td>2D id</td>
<td>SUB EAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract imm32 from EAX.</td>
</tr>
<tr>
<td>REX.W + 2D id</td>
<td>SUB RAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract imm32 sign-extended to 64-bits from RAX.</td>
</tr>
<tr>
<td>80 /5 ib</td>
<td>SUB r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract imm8 from r/m8.</td>
</tr>
<tr>
<td>REX + 80 /5 ib</td>
<td>SUB r/m8*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract imm8 from r/m8.</td>
</tr>
<tr>
<td>81 /5 iw</td>
<td>SUB r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract imm16 from r/m16.</td>
</tr>
<tr>
<td>81 /5 id</td>
<td>SUB r/m32, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract imm32 from r/m32.</td>
</tr>
<tr>
<td>REX.W + 81 /5 id</td>
<td>SUB r/m64, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract imm32 sign-extended to 64-bits from r/m64.</td>
</tr>
<tr>
<td>83 /5 ib</td>
<td>SUB r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract sign-extended imm8 from r/m16.</td>
</tr>
<tr>
<td>83 /5 ib</td>
<td>SUB r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract sign-extended imm8 from r/m32.</td>
</tr>
<tr>
<td>REX.W + 83 /5 ib</td>
<td>SUB r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract sign-extended imm8 from r/m64.</td>
</tr>
<tr>
<td>28 /r</td>
<td>SUB r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract r8 from r/m8.</td>
</tr>
<tr>
<td>REX + 28 /r</td>
<td>SUB r/m8*, r8*</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract r8 from r/m8.</td>
</tr>
<tr>
<td>29 /r</td>
<td>SUB r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract r16 from r/m16.</td>
</tr>
<tr>
<td>29 /r</td>
<td>SUB r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract r32 from r/m32.</td>
</tr>
<tr>
<td>REX.W + 29 /r</td>
<td>SUB r/m64, r32</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract r32 from r/m64.</td>
</tr>
<tr>
<td>2A /r</td>
<td>SUB r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract r/m8 from r8.</td>
</tr>
<tr>
<td>REX + 2A /r</td>
<td>SUB r8*, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract r/m8 from r8.</td>
</tr>
<tr>
<td>2B /r</td>
<td>SUB r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract r/m16 from r16.</td>
</tr>
<tr>
<td>2B /r</td>
<td>SUB r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Subtract r/m32 from r32.</td>
</tr>
<tr>
<td>REX.W + 2B /r</td>
<td>SUB r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Subtract r/m64 from r64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
INSTRUCTION SET REFERENCE, M-Z

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>AL/AX/EAX/RAX</td>
<td>imm8/26/32</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>M</td>
<td>ModRM:r/m (r, w)</td>
<td>imm8/26/32</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>R</td>
<td>ModRM:r/m (r, w)</td>
<td>ModRM/reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Subtracts the second operand (source operand) from the first operand (destination operand) and stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, register, or memory location. (However, two memory operands cannot be used in one instruction.) When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The SUB instruction performs integer subtraction. It evaluates the result for both signed and unsigned integer operands and sets the OF and CF flags to indicate an overflow in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

### Operation

\[
\text{DEST} \leftarrow (\text{DEST} - \text{SRC});
\]

### Flags Affected

The OF, SF, ZF, AF, PF, and CF flags are set according to the result.

### Protected Mode Exceptions

- **#GP(0)**: If the destination is located in a non-writable segment.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#PF(0)**: If the DS, ES, FS, or GS register contains a NULL segment selector.

### SUB—Subtract
INSTRUCTION SET REFERENCE, M-Z

#PF(fault-code)    If a page fault occurs.
#AC(0)             If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD                 If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions

#GP             If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS             If a memory operand effective address is outside the SS segment limit.
#UD              If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions

#GP(0)        If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)        If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)   If a page fault occurs.
#AC(0)        If alignment checking is enabled and an unaligned memory reference is made.
#UD              If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0)        If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)        If the memory address is in a non-canonical form.
#PF(fault-code)   If a page fault occurs.
#AC(0)        If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD              If the LOCK prefix is used but the destination is not a memory operand.
### SUBPD—Subtract Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 5C /r SUBPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtract packed double-precision floating-point values in xmm2/m128 from xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 5C /r VSUBPD xmm1,xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed double-precision floating-point values in xmm3/mem from xmm2 and stores result in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 5C /r VSUBPD ymm1, ymm2, ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed double-precision floating-point values in ymm3/mem from ymm2 and stores result in ymm1.</td>
</tr>
</tbody>
</table>

#### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRM/r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM/r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Description

Performs a SIMD subtract of the two packed double-precision floating-point values in the source operand (second operand) from the two packed double-precision floating-point values in the destination operand (first operand), and stores the packed double-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 11-3 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a SIMD double-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: T second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified.
INSTRUCTION SET REFERENCE, M-Z

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

Operation

**SUBPD (128-bit Legacy SSE version)**

DEST[63:0] ← DEST[63:0] - SRC[63:0]
DEST[VLMAX-1:128] (Unmodified)

**VSUBPD (VEX.128 encoded version)**

DEST[63:0] ← SRC1[63:0] - SRC2[63:0]
DEST[127:64] ← SRC1[127:64] - SRC2[127:64]
DEST[VLMAX-1:128] ← 0

**VSUBPD (VEX.256 encoded version)**

DEST[63:0] ← SRC1[63:0] - SRC2[63:0]
DEST[127:64] ← SRC1[127:64] - SRC2[127:64]

Intel C/C++ Compiler Intrinsic Equivalent

SUBPD: __m128d _mm_sub_pd (m128d a, m128d b)
VSUBPD: __m256d _mm256_sub_pd (__m256d a, __m256d b);

SIMD Floating-Point Exceptions

Overflow, Underflow, Invalid, Precision, Denormal.

Other Exceptions

See Exceptions Type 2.
## SUBPS—Subtract Packed Single-Precision Floating-Point Values

### Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode</th>
<th>CPUID Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 5C /r SUBPS xmm1 xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Subtract packed single-precision floating-point values in xmm2/mem from xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 5C /r VSUBPS xmm1,xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed single-precision floating-point values in xmm3/mem from xmm2 and stores result in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 5C /r VSUBPS ymm1, ymm2, ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract packed single-precision floating-point values in ymm3/mem from ymm2 and stores result in ymm1.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Performs a SIMD subtract of the four packed single-precision floating-point values in the source operand (second operand) from the four packed single-precision floating-point values in the destination operand (first operand), and stores the packed single-precision floating-point results in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register. See Figure 10-5 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an illustration of a SIMD double-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified.
VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**SUBPS (128-bit Legacy SSE version)**

\[
\begin{align*}
\text{DEST}[31:0] &\leftarrow \text{SRC1}[31:0] - \text{SRC2}[31:0] \\
\text{DEST}[95:64] &\leftarrow \text{SRC1}[95:64] - \text{SRC2}[95:64] \\
\text{DEST}[127:96] &\leftarrow \text{SRC1}[127:96] - \text{SRC2}[127:96] \\
\text{DEST}[\text{VLMAX}-1:128] &\text{(Unmodified)}
\end{align*}
\]

**VSUBPS (VEX.128 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] &\leftarrow \text{SRC1}[31:0] - \text{SRC2}[31:0] \\
\text{DEST}[95:64] &\leftarrow \text{SRC1}[95:64] - \text{SRC2}[95:64] \\
\text{DEST}[127:96] &\leftarrow \text{SRC1}[127:96] - \text{SRC2}[127:96] \\
\text{DEST}[\text{VLMAX}-1:128] &\leftarrow 0
\end{align*}
\]

**VSUBPS (VEX.256 encoded version)**

\[
\begin{align*}
\text{DEST}[31:0] &\leftarrow \text{SRC1}[31:0] - \text{SRC2}[31:0] \\
\text{DEST}[95:64] &\leftarrow \text{SRC1}[95:64] - \text{SRC2}[95:64] \\
\text{DEST}[127:96] &\leftarrow \text{SRC1}[127:96] - \text{SRC2}[127:96] \\
\text{DEST}[159:128] &\leftarrow \text{SRC1}[159:128] - \text{SRC2}[159:128] \\
\text{DEST[223:192]} &\leftarrow \text{SRC1}[223:192] - \text{SRC2}[223:192] \\
\end{align*}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

SUBPS: \[
\_\_\_m128 \_\_mm_sub_ps(\_\_m128 a, \_\_m128 b)
\]

VSUBPS: \[
\_\_\_m256 \_\_mm256_sub_ps (\_\_m256 a, \_\_m256 b);
\]

**SIMD Floating-Point Exceptions**

Overflow, Underflow, Invalid, Precision, Denormal.
Other Exceptions
See Exceptions Type 2.
**SUBSD—Subtract Scalar Double-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2 0F 5C /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Subtracts the low double-precision floating-point values in <code>xmm2/mem64</code> from <code>xmm1</code>.</td>
</tr>
<tr>
<td>SUBSD <code>xmm1, xmm2/m64</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.LIG.F2.0F.WIG 5C /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Subtract the low double-precision floating-point value in <code>xmm3/mem</code> from <code>xmm2</code> and store the result in <code>xmm1</code>.</td>
</tr>
<tr>
<td>VSUBSD <code>xmm1,xmm2, xmm3/m64</code></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Subtracts the low double-precision floating-point value in the source operand (second operand) from the low double-precision floating-point value in the destination operand (first operand), and stores the double-precision floating-point result in the destination operand. The source operand can be an XMM register or a 64-bit memory location. The destination operand is an XMM register. The high quadword of the destination operand remains unchanged. See Figure 11-4 in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for an illustration of a scalar double-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VMAX-1:64) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:64) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VMAX-1:128) of the destination YMM register are zeroed.

### Operation

**SUBSD (128-bit Legacy SSE version)**

\[
\text{DEST}[63:0] \leftarrow \text{DEST}[63:0] - \text{SRC}[63:0]
\]

\[
\text{DEST}[\text{VMAX}-1:64] \text{ (Unmodified)}
\]
VSUBSD (VEX.128 encoded version)
DEST[63:0] ← SRC1[63:0] - SRC2[63:0]
DEST[127:64] ← SRC1[127:64]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
SUBSD: __m128d _mm_sub_sd (m128d a, m128d b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Other Exceptions
See Exceptions Type 3.
SUBSS—Subtract Scalar Single-Precision Floating-Point Values

**Description**
Subtracts the low single-precision floating-point value in the source operand (second operand) from the low single-precision floating-point value in the destination operand (first operand), and stores the single-precision floating-point result in the destination operand. The source operand can be an XMM register or a 32-bit memory location. The destination operand is an XMM register. The three high-order double-words of the destination operand remain unchanged. See Figure 10-6 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1, for an illustration of a scalar single-precision floating-point operation.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The destination and first source operand are the same. Bits (VMAX-1:32) of the corresponding YMM destination register remain unchanged.

VEX.128 encoded version: Bits (127:32) of the XMM register destination are copied from corresponding bits in the first source operand. Bits (VMAX-1:128) of the destination YMM register are zeroed.

**Operation**

**SUBSS (128-bit Legacy SSE version)**
DEST[31:0] ← DEST[31:0] - SRC[31:0]
DEST[VMAX-1:32] (Unmodified)
VSUBSS (VEX.128 encoded version)
DEST[31:0] ← SRC1[31:0] - SRC2[31:0]
DEST[VLMAX-1:128] ← 0

Intel C/C++ Compiler Intrinsic Equivalent
SUBSS: __m128 _mm_sub_ss(__m128 a, __m128 b)

SIMD Floating-Point Exceptions
Overflow, Underflow, Invalid, Precision, Denormal.

Other Exceptions
See Exceptions Type 3.
**SWAPGS—Swap GS Base Register**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compal/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 01 /7</td>
<td>SWAPGS</td>
<td>NP</td>
<td>Valid</td>
<td>Invalid</td>
<td>Exchanges the current GS base register value with the value contained in MSR address C0000102H.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

SWAPGS exchanges the current GS base register value with the value contained in MSR address C0000102H (MSR KERNELGSbase). KernelGSbase is guaranteed to be canonical; so SWAPGS does not perform a canonical check. The SWAPGS instruction is a privileged instruction intended for use by system software.

When using SYSCALL to implement system calls, there is no kernel stack at the OS entry point. Neither is there a straightforward method to obtain a pointer to kernel structures from which the kernel stack pointer could be read. Thus, the kernel can't save general purpose registers or reference memory.

By design, SWAPGS does not require any general purpose registers or memory operands. No registers need to be saved before using the instruction. SWAPGS exchanges the CPL 0 data pointer from the KernelGSbase MSR with the GS base register. The kernel can then use the GS prefix on normal memory references to access kernel data structures. Similarly, when the OS kernel is entered using an interrupt or exception (where the kernel stack is already set up), SWAPGS can be used to quickly get a pointer to the kernel data structures.

The KernelGSbase MSR itself is only accessible using RDMSR/WRMSR instructions. Those instructions are only accessible at privilege level 0. WRMSR will cause a #GP(0) if the value to be written to KernelGSbase MSR is non-canonical.

See Table 4-19.

### Table 4-19. SWAPGS Operation Parameters

<table>
<thead>
<tr>
<th>Opcode</th>
<th>ModR/M Byte</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOD</td>
<td>REG</td>
<td>R/M</td>
</tr>
<tr>
<td>OF 01</td>
<td>MOD ≠ 11</td>
<td>111</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>111</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>111</td>
</tr>
</tbody>
</table>
Operation

IF CS.L ≠ 1 (* Not in 64-Bit Mode *)
    THEN #UD; Fl;

IF CPL ≠ 0
    THEN #GP(0); Fl;

tmp ← GS(BASE);
GS(BASE) ← KERNELGSbase;
KERNELGSbase ← tmp;

Flags Affected

None

Protected Mode Exceptions

#UD If Mode ≠ 64-Bit.

Real-Address Mode Exceptions

#UD If Mode ≠ 64-Bit.

Virtual-8086 Mode Exceptions

#UD If Mode ≠ 64-Bit.

Compatibility Mode Exceptions

#UD If Mode ≠ 64-Bit.

64-Bit Mode Exceptions

#GP(0) If CPL ≠ 0.
    If the LOCK prefix is used.
**SYSCALL—Fast System Call**

**Description**

SYSCALL saves the RIP of the instruction following SYSCALL to RCX and loads a new RIP from the IA32_LSTAR (64-bit mode). Upon return, SYSRET copies the value saved in RCX to the RIP.

SYSCALL saves RFLAGS (lower 32 bit only) in R11. It then masks RFLAGS with an OS-defined value using the IA32_FMASK (MSR C000_0084). The actual mask value used by the OS is the complement of the value written to the IA32_FMASK MSR. None of the bits in RFLAGS are automatically cleared (except for RF). SYSRET restores RFLAGS from R11 (the lower 32 bits only).

Software should not alter the CS or SS descriptors in a manner that violates the following assumptions made by SYSCALL/SYSRET:

- The CS and SS base and limit remain the same for all processes, including the operating system (the base is 0H and the limit is 0FFFFFFFFH).
- The CS of the SYSCALL target has a privilege level of 0.
- The CS of the SYSRET target has a privilege level of 3.

SYSCALL/SYSRET do not check for violations of these assumptions.

**Operation**

IF (CS.L ≠ 1) or (IA32_EFER.LMA ≠ 1) or (IA32_EFER.SCE ≠ 1)
(* Not in 64-Bit Mode or SYSCALL/SYSRET not enabled in IA32_EFER *)

THEN #UD; FI;

RCX ← RIP;
RIP ← LSTAR_MSR;
R11 ← EFLAGS;
EFLAGS ← (EFLAGS MASKED BY IA32_FMASK);
CPL ← 0;
CS(SEL) ← IA32_STAR_MSR[47:32];
CS(DPL) ← 0;
CS(BASE) ← 0;
CS(LIMIT) ← 0xFFFFF;
CS(GRANULAR) ← 1;
SS(SEL) ← IA32_STAR_MSR[47:32] + 8;
SS(DPL) ← 0;
SS(BASE) ← 0;
SS(LIMIT) ← 0xFFFFF;
SS(GRANULAR) ← 1;

Flags Affected
All.

Protected Mode Exceptions
#UD If Mode ≠ 64-bit.

Real-Address Mode Exceptions
#UD If Mode ≠ 64-bit.

Virtual-8086 Mode Exceptions
#UD If Mode ≠ 64-bit.

Compatibility Mode Exceptions
#UD If Mode ≠ 64-bit.

64-Bit Mode Exceptions
#UD If IA32_EFER.SCE = 0.
If the LOCK prefix is used.

SYSENTER—Fast System Call

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Log Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 34</td>
<td>SYSENTER</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Fast call to privilege level 0 system procedures.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Executes a fast call to a level 0 system procedure or routine. SYSENTER is a companion instruction to SYSEXIT. The instruction is optimized to provide the maximum performance for system calls from user code running at privilege level 3 to operating system or executive procedures running at privilege level 0.

Prior to executing the SYSENTER instruction, software must specify the privilege level 0 code segment and code entry point, and the privilege level 0 stack segment and stack pointer by writing values to the following MSRs:

- **IA32_SYSENTER_CS** — Contains a 32-bit value, of which the lower 16 bits are the segment selector for the privilege level 0 code segment. This value is also used to compute the segment selector of the privilege level 0 stack segment.
- **IA32_SYSENTER_EIP** — Contains the 32-bit offset into the privilege level 0 code segment to the first instruction of the selected operating procedure or routine.
- **IA32_SYSENTER_ESP** — Contains the 32-bit stack pointer for the privilege level 0 stack.

These MSRs can be read from and written to using RDMSR/WRMSR. Register addresses are listed in Table 4-20. The addresses are defined to remain fixed for future Intel 64 and IA-32 processors.

**Table 4-20. MSRs Used By the SYSENTER and SYSEXIT Instructions**

<table>
<thead>
<tr>
<th>MSR</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>IA32_SYSENTER_CS</td>
<td>174H</td>
</tr>
<tr>
<td>IA32_SYSENTER_ESP</td>
<td>175H</td>
</tr>
<tr>
<td>IA32_SYSENTER_EIP</td>
<td>176H</td>
</tr>
</tbody>
</table>

When SYSENTER is executed, the processor:

1. Loads the segment selector from the IA32_SYSENTER_CS into the CS register.
2. Loads the instruction pointer from the IA32_SYSENTER_EIP into the EIP register.
3. Adds 8 to the value in IA32_SYSENTER_CS and loads it into the SS register.
4. Loads the stack pointer from the IA32_SYSENTER_ESP into the ESP register.
5. Switches to privilege level 0.
6. Clears the VM flag in the EFLAGS register, if the flag is set.
7. Begins executing the selected system procedure.

The processor does not save a return IP or other state information for the calling procedure.

The SYSENTER instruction always transfers program control to a protected-mode code segment with a DPL of 0. The instruction requires that the following conditions are met by the operating system:

- The segment descriptor for the selected system code segment selects a flat, 32-bit code segment of up to 4 GBytes, with execute, read, accessed, and non-conforming permissions.
- The segment descriptor for selected system stack segment selects a flat 32-bit stack segment of up to 4 GBytes, with read, write, accessed, and expand-up permissions.

The SYSENTER instruction can be invoked from all operating modes except real-address mode.

The SYSENTER and SYSEXIT instructions are companion instructions, but they do not constitute a call/return pair. When executing a SYSENTER instruction, the processor does not save state information for the user code, and neither the SYSENTER nor the SYSEXIT instruction supports passing parameters on the stack.

To use the SYSENTER and SYSEXIT instructions as companion instructions for transitions between privilege level 3 code and privilege level 0 operating system procedures, the following conventions must be followed:

- The segment descriptors for the privilege level 0 code and stack segments and for the privilege level 3 code and stack segments must be contiguous in the global descriptor table. This convention allows the processor to compute the segment selectors from the value entered in the SYSENTER_CS_MSR MSR.
- The fast system call "stub" routines executed by user code (typically in shared libraries or DLLs) must save the required return IP and processor state information if a return to the calling procedure is required. Likewise, the operating system or executive procedures called with SYSENTER instructions must have access to and use this saved return and state information when returning to the user code.

The SYSENTER and SYSEXIT instructions were introduced into the IA-32 architecture in the Pentium II processor. The availability of these instructions on a processor is indicated with the SYSENTER/SYSEXIT present (SEP) feature flag returned to the EDX register by the CPUID instruction. An operating system that qualifies the SEP flag must also qualify the processor family and model to ensure that the SYSENTER/SYSEXIT instructions are actually present. For example:

IF CPUID SEP bit is set
THEN IF (Family = 6) and (Model < 3) and (Stepping < 3) THEN
    SYSENTER/SYSEXIT_Not_Supported; Fl;
ELSE
    SYSENTER/SYSEXIT_Supported; Fl;
FI;

When the CPUID instruction is executed on the Pentium Pro processor (model 1), the processor returns a the SEP flag as set, but does not support the SYSENTER/SYSEXIT instructions.

**Operation**

IF CR0.PE = 0 THEN #GP(0); Fl;
IF SYSENTER_CS_MSR[15:2] = 0 THEN #GP(0); Fl;
EFLAGS.VM ← 0; (* ensures protected mode execution *)
EFLAGS.IF ← 0; (* Mask interrupts *)
EFLAGS.RF ← 0;
CS.SEL ← SYSENTER_CS_MSR (* Operating system provides CS *)
(* Set rest of CS to a fixed value *)
CS.SEL.RPL ← 0;
CS.BASE ← 0; (* Flat segment *)
CS.ARbyte.G ← 1; (* 4-KByte granularity *)
CS.ARbyte.S ← 1;
CS.ARbyte.TYPE ← 1011B; (* Execute + Read, Accessed *)
CS.ARbyte.D ← 1; (* 32-bit code segment*)
CS.ARbyte.DPL ← 0;
CS.ARbyte.P ← 1;
CS.LIMIT ← FFFFFFFH; (* with 4-KByte granularity, implies a 4-GByte limit *)
CPL ← 0;
SS.SEL ← CS.SEL + 8;
(* Set rest of SS to a fixed value *)
SS.SEL.RPL ← 0;
SS.BASE ← 0; (* Flat segment *)
SS.ARbyte.G ← 1; (* 4-KByte granularity *)
SS.ARbyte.S ← 1;
SS.ARbyte.TYPE ← 0011B; (* Read/Write, Accessed *)
SS.ARbyte.D ← 1; (* 32-bit stack segment*)
SS.ARbyte.DPL ← 0;
SS.ARbyte.P ← 1;
SS.LIMIT ← FFFFFFFH; (* with 4-KByte granularity, implies a 4-GByte limit *)
ESP ← SYSENTER_ESP_MSR;
SYSENTER—Fast System Call

EIP ← SYSENTER_EIP MSR;

**IA-32e Mode Operation**

In IA-32e mode, SYSENTER executes a fast system calls from user code running at privilege level 3 (in compatibility mode or 64-bit mode) to 64-bit executive procedures running at privilege level 0. This instruction is a companion instruction to the SYSEXIT instruction.

In IA-32e mode, the IA32_SYSENTER_EIP and IA32_SYSENTER_ESP MSRs hold 64-bit addresses and must be in canonical form; IA32_SYSENTER_CS must not contain a NULL selector.

When SYSENTER transfers control, the following fields are generated and bits set:

- **Target code segment** — Reads non-NULL selector from IA32_SYSENTER_CS.
- **New CS attributes** — L-bit = 1 (go to 64-bit mode); CS base = 0, CS limit = FFFFFFFH.
- **Target instruction** — Reads 64-bit canonical address from IA32_SYSENTER_EIP.
- **Stack segment** — Computed by adding 8 to the value from IA32_SYSENTER_CS.
- **Stack pointer** — Reads 64-bit canonical address from IA32_SYSENTER_ESP.
- **New SS attributes** — SS base = 0, SS limit = FFFFFFFH.

**Flags Affected**

VM, IF, RF (see Operation above)

**Protected Mode Exceptions**

- **#GP(0)** If IA32_SYSENTER_CS[15:2] = 0.
- **#UD** If the LOCK prefix is used.

**Real-Address Mode Exceptions**

- **#GP** If protected mode is not enabled.
- **#UD** If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

Same exceptions as in protected mode.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.
64-Bit Mode Exceptions
Same exceptions as in protected mode.
SYSEXT—Fast Return from Fast System Call

### Opcode Instruction

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 35</td>
<td>SYSEXIT</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Fast return to privilege level 3 user code.</td>
</tr>
<tr>
<td>REX.W + 0F 35</td>
<td>SYSEXIT</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Fast return to 64-bit mode privilege level 3 user code.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Executes a fast return to privilege level 3 user code. SYSEXIT is a companion instruction to the SYSENTER instruction. The instruction is optimized to provide the maximum performance for returns from system procedures executing at protections levels 0 to user procedures executing at protection level 3. It must be executed from code executing at privilege level 0.

Prior to executing SYSEXIT, software must specify the privilege level 3 code segment and code entry point, and the privilege level 3 stack segment and stack pointer by writing values into the following MSR and general-purpose registers:

- **IA32_SYSENTER_CS** — Contains a 32-bit value, of which the lower 16 bits are the segment selector for the privilege level 0 code segment in which the processor is currently executing. This value is used to compute the segment selectors for the privilege level 3 code and stack segments.
- **EDX** — Contains the 32-bit offset into the privilege level 3 code segment to the first instruction to be executed in the user code.
- **ECX** — Contains the 32-bit stack pointer for the privilege level 3 stack.

The IA32_SYSENTER_CS MSR can be read from and written to using RDMSR/WRMSR. The register address is listed in Table 4-20. This address is defined to remain fixed for future Intel 64 and IA-32 processors.

When SYSEXIT is executed, the processor:

1. Adds 16 to the value in IA32_SYSENTER_CS and loads the sum into the CS selector register.
2. Loads the instruction pointer from the EDX register into the EIP register.
3. Adds 24 to the value in IA32_SYSENTER_CS and loads the sum into the SS selector register.
4. Loads the stack pointer from the ECX register into the ESP register.
5. Switches to privilege level 3.
6. Begins executing the user code at the EIP address.

See “SWAPGS—Swap GS Base Register” in this chapter for information about using the SYSENTER and SYSEXIT instructions as companion call and return instructions.

The SYSEXIT instruction always transfers program control to a protected-mode code segment with a DPL of 3. The instruction requires that the following conditions are met by the operating system:

- The segment descriptor for the selected user code segment selects a flat, 32-bit code segment of up to 4 GBytes, with execute, read, accessed, and non-conforming permissions.
- The segment descriptor for selected user stack segment selects a flat, 32-bit stack segment of up to 4 GBytes, with expand-up, read, write, and accessed permissions.

The SYSEXIT instruction can be invoked from all operating modes except real-address mode and virtual 8086 mode.

The SYSENTER and SYSEXIT instructions were introduced into the IA-32 architecture in the Pentium II processor. The availability of these instructions on a processor is indicated with the SYSENTER/SYSEXIT present (SEP) feature flag returned to the EDX register by the CPUID instruction. An operating system that qualifies the SEP flag must also qualify the processor family and model to ensure that the SYSENTER/SYSEXIT instructions are actually present. For example:

```
IF CPUID SEP bit is set
    THEN IF (Family = 6) and (Model < 3) and (Stepping < 3)
        THEN
            SYSENTER/SYSEXIT_Not_Supported; Fl;
        ELSE
            SYSENTER/SYSEXIT_Supported; Fl;
    Fl;
```

When the CPUID instruction is executed on the Pentium Pro processor (model 1), the processor returns the SEP flag as set, but does not support the SYSENTER/SYSEXIT instructions.

**Operation**

```
IF SYSENTER_CS_MSR[15:2] = 0 THEN #GP(0); Fl;
IF CRO.PE = 0 THEN #GP(0); Fl;
IF CPL ≠ 0 THEN #GP(0); Fl;
CS.SEL ← (SYSENTER_CS_MSR + 16); (* Segment selector for return CS *)
CS.SEL.RPL ← 3; (* Set rest of CS to a fixed value *)
CS.BASE ← 0; (* Flat segment *)
```
In IA-32e mode, SYSEXIT executes a fast system calls from a 64-bit executive procedures running at privilege level 0 to user code running at privilege level 3 (in compatibility mode or 64-bit mode). This instruction is a companion instruction to the SYSENTER instruction.

In IA-32e mode, the IA32_SYSENTER_CS, IA32_SYSENTER_EIP, and IA32_SYSENTER_ESP MSRs hold 64-bit addresses and must be in canonical form; IA32_SYSENTER_CS must not contain a NULL selector.

When the SYSEXIT instruction transfers control to 64-bit mode user code using REX.W, the following fields are generated and bits set:

- **Target code segment** — Computed by adding 32 to the value in the IA32_SYSENTER_CS.
- **New CS attributes** — L-bit = 1 (go to 64-bit mode).
- **Target instruction** — Reads 64-bit canonical address in RDX.
- **Stack segment** — Computed by adding 8 to the value of CS selector.
- **Stack pointer** — Update RSP using 64-bit canonical address in RCX.

When SYSEXIT transfers control to compatibility mode user code when the operand size attribute is 32 bits, the following fields are generated and bits set:
**Target code segment** — Computed by adding 16 to the value in IA32_SYSENTER_CS.

**New CS attributes** — L-bit = 0 (go to compatibility mode).

**Target instruction** — Fetch the target instruction from 32-bit address in EDX.

**Stack segment** — Computed by adding 24 to the value in IA32_SYSENTER_CS.

**Stack pointer** — Update ESP from 32-bit address in ECX.

**Flags Affected**

None.

**Protected Mode Exceptions**

#GP(0) If IA32_SYSENTER_CS[15:2] = 0.

If CPL ≠ 0.

#UD If the LOCK prefix is used.

**Real-Address Mode Exceptions**

#GP If protected mode is not enabled.

#UD If the LOCK prefix is used.

**Virtual-8086 Mode Exceptions**

#GP(0) Always.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#GP(0) If IA32_SYSENTER_CS = 0.

If CPL ≠ 0.

If ECX or EDX contains a non-canonical address.

#UD If the LOCK prefix is used.
SYSRET—Return From Fast System Call

**Description**

SYSCALL saves the RIP of the instruction following the SYSCALL into RCX and loads the new RIP from the LSTAR (64-bit mode only). Upon return, SYSRET copies the value saved in RCX to the RIP.

In a return to 64-bit mode using Osize 64, SYSRET sets the CS selector value to MSR IA32_STAR[63:48] +16. The SS is set to IA32_STAR[63:48] + 8.

SYSRET transfer control to compatibility mode using Osize 32. The CS selector value is set to MSR IA32_STAR[63:48]. The SS is set to IA32_STAR[63:48] + 8.

It is the responsibility of the OS to keep descriptors in the GDT/LDT that correspond to selectors loaded by SYSCALL/SYSRET consistent with the base, limit and attribute values forced by the these instructions.

Software should not alter the CS or SS descriptors in a manner that violates the following assumptions made by SYSCALL/SYSRET:

- CS and SS base and limit remain the same for all processes, including the operating system.
- CS of the SYSCALL target has a privilege level of 0.
- CS of the SYSRET target has a privilege level of 3.

SYSCALL/SYSRET do not check for violations of these assumptions.

**Operation**

IF (CS.L ≠ 1) or (IA32_EFER.LMA ≠ 1) or (IA32_EFER.SCE ≠ 1)
(*) Not in 64-Bit Mode or SYSCALL/SYSRET not enabled in IA32_EFER *

    THEN #UD; Fl;

IF (CPL ≠ 0)

    THEN #GP(0); Fl;

IF (RCX ≠ CANONICAL_ADDRESS)

---

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 07</td>
<td>SYSRET</td>
<td>NP</td>
<td>Valid</td>
<td>Invalid</td>
<td>Return to compatibility mode from fast system call</td>
</tr>
<tr>
<td>REX.W + 0F 07</td>
<td>SYSRET</td>
<td>NP</td>
<td>Valid</td>
<td>Invalid</td>
<td>Return to 64-bit mode from fast system call</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
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<th>Op/En</th>
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<th>Operand 4</th>
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<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
THEN #GP(0); Fl;
IF (OPERAND_SIZE = 64)
THEN (* Return to 64-Bit Mode *)
   EFLAGS ← R11;
   CPL ← 0x3;
   CS(SEL) ← IA32_STAR[63:48] + 16;
   CS(PL) ← 0x3;
   SS(SEL) ← IA32_STAR[63:48] + 8;
   SS(PL) ← 0x3;
   RIP ← RCX;
ELSE (* Return to Compatibility Mode *)
   EFLAGS ← R11;
   CPL ← 0x3;
   CS(SEL) ← IA32_STAR[63:48];
   CS(PL) ← 0x3;
   SS(SEL) ← IA32_STAR[63:48] + 8;
   SS(PL) ← 0x3;
   EIP ← ECX;
FI;

Flags Affected
VM, IF, RF.

Protected Mode Exceptions
#UD If Mode ≠ 64-Bit.

Real-Address Mode Exceptions
#UD If Mode ≠ 64-Bit.

Virtual-8086 Mode Exceptions
#UD If Mode ≠ 64-Bit.

Compatibility Mode Exceptions
#UD If Mode ≠ 64-Bit.

64-Bit Mode Exceptions
#UD If IA32_EFER.SCE bit = 0.
   If the LOCK prefix is used.
#GP(0) If CPL ≠ 0.
   If ECX contains a non-canonical address.
## TEST—Logical Compare

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<th>Opcode</th>
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<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Eg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A8 ib</td>
<td>TEST AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>AND imm8 with AL; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td>A9 iw</td>
<td>TEST AX, imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>AND imm16 with AX; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td>A9 id</td>
<td>TEST EAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>AND imm32 with EAX; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td></td>
<td>REX.W + A9 id</td>
<td></td>
<td></td>
<td></td>
<td>AND imm32 sign-extended to 64-bits with RAX; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td>F6 /0 ib</td>
<td>TEST r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>AND imm8 with r/m8; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td></td>
<td>REX + F6 /0 ib</td>
<td></td>
<td></td>
<td></td>
<td>AND imm8 with r/m8; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td>F7 /0 iw</td>
<td>TEST r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>AND imm16 with r/m16; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td></td>
<td>F7 /0 id</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>AND imm32 with r/m32; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td></td>
<td>REX.W + F7 /0 id</td>
<td></td>
<td></td>
<td></td>
<td>AND imm32 sign-extended to 64-bits with r/m64; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td>84 /r</td>
<td>TEST r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>AND r8 with r/m8; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td></td>
<td>REX + 84 /r</td>
<td></td>
<td></td>
<td></td>
<td>AND r8 with r/m8; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td>85 /r</td>
<td>TEST r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>AND r16 with r/m16; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td></td>
<td>TEST r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>AND r32 with r/m32; set SF, ZF, PF according to result.</td>
</tr>
<tr>
<td></td>
<td>REX.W + 85 /r</td>
<td></td>
<td></td>
<td></td>
<td>AND r64 with r/m64; set SF, ZF, PF according to result.</td>
</tr>
</tbody>
</table>
**NOTES:**
* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

### Instruction Operand Encoding

<table>
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<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>AL/AX/EAX/RAX</td>
<td>imm8/16/32</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM:r/m (r)</td>
<td>imm8/16/32</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (r)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description
Computes the bit-wise logical AND of first operand (source 1 operand) and the second operand (source 2 operand) and sets the SF, ZF, and PF status flags according to the result. The result is then discarded.

In 64-bit mode, using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

### Operation

\[
\begin{align*}
TEMP & \leftarrow SRC1 \text{ AND } SRC2; \\
SF & \leftarrow \text{MSB}(TEMP); \\
\text{IF } TEMP = 0 \\
\quad \text{THEN } ZF & \leftarrow 1; \\
\quad \text{ELSE } ZF & \leftarrow 0; \\
\text{FI:} \\
PF & \leftarrow \text{BitwiseXNOR}(TEMP[0:7]); \\
CF & \leftarrow 0; \\
OF & \leftarrow 0; \\
\text{(* AF is undefined *)}
\end{align*}
\]

### Flags Affected
The OF and CF flags are set to 0. The SF, ZF, and PF flags are set according to the result (see the “Operation” section above). The state of the AF flag is undefined.

### Protected Mode Exceptions

- **#GP(0)**
  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.
UCOMISD—Unordered Compare Scalar Double-Precision Floating-Point Values and Set EFLAGS

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 2E /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Compares (unordered) the low double-precision floating-point values in ( xmm1 ) and ( xmm2/m64 ) and set the EFLAGS accordingly.</td>
</tr>
<tr>
<td>UCOMISD ( xmm1, xmm2/m64 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.66.0F.WIG 2E /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare low double precision floating-point values in ( xmm1 ) and ( xmm2/mem64 ) and set the EFLAGS flags accordingly.</td>
</tr>
<tr>
<td>VUCOMISD ( xmm1, xmm2/m64 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r)</td>
<td>ModRM:rm/r (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs and unordered compare of the double-precision floating-point values in the low quadwords of source operand 1 (first operand) and source operand 2 (second operand), and sets the ZF, PF, and CF flags in the EFLAGS register according to the result (unordered, greater than, less than, or equal). The OF, SF and AF flags in the EFLAGS register are set to 0. The unordered result is returned if either source operand is a NaN (QNaN or SNaN).

Source operand 1 is an XMM register; source operand 2 can be an XMM register or a 64 bit memory location.

The UCOMISD instruction differs from the COMISD instruction in that it signals a SIMD floating-point invalid operation exception (#I) only when a source operand is an SNaN. The COMISD instruction signals an invalid operation exception if a source operand is either a QNaN or an SNaN.

The EFLAGS register is not updated if an unmasked SIMD floating-point exception is generated.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.
Operation

RESULT ← UnorderedCompare(SRC1[63:0] < > SRC2[63:0]) {
(* Set EFLAGS *)
CASE (RESULT) OF
    UNORDERED: ZF, PF, CF ← 111;
    GREATER_THAN: ZF, PF, CF ← 000;
    LESS_THAN: ZF, PF, CF ← 001;
    EQUAL: ZF, PF, CF ← 100;
ESAC;
    OF, AF, SF ← 0;

Intel C/C++ Compiler Intrinsic Equivalent

int _mm_ucomieq_sd(__m128d a, __m128d b)
int _mm_ucomilt_sd(__m128d a, __m128d b)
int _mm_ucomile_sd(__m128d a, __m128d b)
int _mm_ucomigt_sd(__m128d a, __m128d b)
int _mm_ucomige_sd(__m128d a, __m128d b)
int _mm_ucomineq_sd(__m128d a, __m128d b)

SIMD Floating-Point Exceptions
Invalid (if SNaN operands), Denormal.

Other Exceptions
See Exceptions Type 3; additionally
#UD If VEX.vvvv != 1111B.
UCOMISS—Unordered Compare Scalar Single-Precision Floating-Point Values and Set EFLAGS

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF 2E /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Compare lower single-precision floating-point value in xmm1 register with lower single-precision floating-point value in xmm2/mem and set the status flags accordingly.</td>
</tr>
<tr>
<td>UCOMISS xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.LIG.0F.WIG 2E /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Compare low single precision floating-point values in xmm1 and xmm2/mem32 and set the EFLAGS flags accordingly.</td>
</tr>
<tr>
<td>VUCOMISS xmm1, xmm2/m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

**Instruction Operand Encoding**

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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs and unordered compare of the single-precision floating-point values in the low doublewords of the source operand 1 (first operand) and the source operand 2 (second operand), and sets the ZF, PF, and CF flags in the EFLAGS register according to the result (unordered, greater than, less than, or equal). In The OF, SF and AF flags in the EFLAGS register are set to 0. The unordered result is returned if either source operand is a NaN (QNaN or SNaN).

Source operand 1 is an XMM register; source operand 2 can be an XMM register or a 32 bit memory location.

The UCOMISS instruction differs from the COMISS instruction in that it signals a SIMD floating-point invalid operation exception (#I) only when a source operand is an SNaN. The COMISS instruction signals an invalid operation exception if a source operand is either a QNaN or an SNaN.

The EFLAGS register is not updated if an unmasked SIMD floating-point exception is generated.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.
**Operation**

RESULT ← UnorderedCompare(SRC1[31:0] <> SRC2[31:0])

(* Set EFLAGS *)

CASE (RESULT) OF

- UNORDERED: ZF,PF,CF ← 111;
- GREATER_THAN: ZF,PF,CF ← 000;
- LESS_THAN: ZF,PF,CF ← 001;
- EQUAL: ZF,PF,CF ← 100;

ESAC;

OF,AF,SF ← 0;

**Intel C/C++ Compiler Intrinsic Equivalent**

int _mm_ucomieq_ss(__m128 a, __m128 b)
int _mm_ucomilt_ss(__m128 a, __m128 b)
int _mm_ucomile_ss(__m128 a, __m128 b)
int _mm_ucomigt_ss(__m128 a, __m128 b)
int _mm_ucomige_ss(__m128 a, __m128 b)
int _mm_ucomineq_ss(__m128 a, __m128 b)

**SIMD Floating-Point Exceptions**

Invalid (if SNaN operands), Denormal.

**Other Exceptions**

See Exceptions Type 3; additionally

#UD If VEX.vvvv != 1111B.
## UD2—Undefined Instruction

### Description
Generates an invalid opcode exception. This instruction is provided for software testing to explicitly generate an invalid opcode exception. The opcode for this instruction is reserved for this purpose.

Other than raising the invalid opcode exception, this instruction has no effect on processor state or memory.

Even though it is the execution of the UD2 instruction that causes the invalid opcode exception, the instruction pointer saved by delivery of the exception references the UD2 instruction (and not the following instruction).

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

### Operation

```plaintext
#UD (* Generates invalid opcode exception *);
```

### Flags Affected
None.

### Exceptions (All Operating Modes)

- **#UD** Raises an invalid opcode exception in all operating modes.
UNPCKHPD—Unpack and Interleave High Packed Double-Precision Floating-Point Values

**Opcode/Instruction** | **Op/En** | **64/32 bit Mode Support** | **CPUID Feature Flag** | **Description** |
---|---|---|---|---|
66 0F 15 /r | RM | V/V | SSE2 | Unpacks and Interleaves double-precision floating-point values from high quadwords of xmm1 and xmm2/m128. |
VEX.NDS.128.66.0F.WIG 15 /r | RVM | V/V | AVX | Unpacks and Interleaves double precision floating-point values from high quadwords of xmm2 and xmm3/m128. |
VEX.NDS.256.66.0F.WIG 15 /r | RVM | V/V | AVX | Unpacks and Interleaves double precision floating-point values from high quadwords of ymm2 and ymm3/m256. |

**Instruction Operand Encoding**

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</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an interleaved unpack of the high double-precision floating-point values from the source operand (second operand) and the destination operand (first operand). See Figure 4-20.
When unpacking from a memory operand, an implementation may fetch only the appropriate 64 bits; however, alignment to 16-byte boundary and normal segment checking will still be enforced.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

**Operation**

**UNPCKHPD (128-bit Legacy SSE version)**

DEST[63:0] ← SRC1[127:64]
DEST[127:64] ← SRC2[127:64]
DEST[VLMAX-1:128] (Unmodified)

**VUNPCKHPD (VEX.128 encoded version)**

DEST[63:0] ← SRC1[127:64]
DEST[127:64] ← SRC2[127:64]
DEST[VLMAX-1:128] ← 0

**VUNPCKHPD (VEX.256 encoded version)**

DEST[63:0] ← SRC1[127:64]
DEST[127:64] ← SRC2[127:64]
DEST[255:192] ← SRC2[255:192]

Intel C/C++ Compiler Intrinsic Equivalent
UNPCKHPD: __m128d _mm_unpackhi_pd(__m128d a, __m128d b)
UNPCKHPD: __m256d _mm256_unpackhi_pd(__m256d a, __m256d b)

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4.
UNPCKHPS—Unpack and Interleave High Packed Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 15 /r UNPCKHPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Unpacks and Interleaves single-precision floating-point values from high quadwords of xmm1 and xmm2/mem into xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 15 /r VUNPCKHPS xmm1,xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Unpacks and Interleaves single-precision floating-point values from high quadwords of xmm2 and xmm3/m128.</td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 15 /r VUNPCKHPS ymm1,ymm2,ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Unpacks and Interleaves single-precision floating-point values from high quadwords of ymm2 and ymm3/m256.</td>
</tr>
</tbody>
</table>

InstructionOperand Encoding

<table>
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<tr>
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<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs an interleaved unpack of the high-order single-precision floating-point values from the source operand (second operand) and the destination operand (first operand). See Figure 4-21. The source operand can be an XMM register or a 128-bit memory location; the destination operand is an XMM register.
UNPCKHPS—Unpack and Interleave High Packed Single-Precision Floating-Point Values

When unpacking from a memory operand, an implementation may fetch only the appropriate 64 bits; however, alignment to 16-byte boundary and normal segment checking will still be enforced.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: T second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

Operation

**UNPCKHPS (128-bit Legacy SSE version)**
- DEST[31:0] ← SRC1[95:64]
- DEST[63:32] ← SRC2[95:64]
- DEST[95:64] ← SRC1[127:96]
- DEST[127:96] ← SRC2[127:96]
- DEST[VLMAX-1:128] (Unmodified)

**VUNPCKHPS (VEX.128 encoded version)**
- DEST[31:0] ← SRC1[95:64]
- DEST[63:32] ← SRC2[95:64]
- DEST[95:64] ← SRC1[127:96]
- DEST[127:96] ← SRC2[127:96]
- DEST[VLMAX-1:128] ← 0
VUNPCKHPS (VEX.256 encoded version)

DEST[31:0] ← SRC1[95:64]
DEST[63:32] ← SRC2[95:64]
DEST[95:64] ← SRC1[127:96]
DEST[127:96] ← SRC2[127:96]
DEST[255:224] ← SRC2[255:224]

Intel C/C++ Compiler Intrinsic Equivalent

UNPCKHPS: __m128 _mm_unpackhi_ps(__m128 a, __m128 b)
UNPCKHPS: __m256 _mm256_unpackhi_ps (__m256 a, __m256 b);

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4.
UNPCKLPD—Unpack and Interleave Low Packed Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 14 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Unpacks and Interleave double-precision floating-point values from low quadwords of xmm1 and xmm2/m128.</td>
</tr>
<tr>
<td>UNPCKLPD xmm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 14 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Unpacks and Interleave double precision floating-point values low high quadwords of xmm2 and xmm3/m128.</td>
</tr>
<tr>
<td>VUNPCKLPD xmm1,xmm2, xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 14 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Unpacks and Interleave double precision floating-point values low high quadwords of ymm2 and ymm3/m256.</td>
</tr>
<tr>
<td>VUNPCKLPD ymm1,ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an interleaved unpack of the low double-precision floating-point values from the source operand (second operand) and the destination operand (first operand). See Figure 4-22. The source operand can be an XMM register or a 128-bit memory location; the destination operand is an XMM register.
When unpacking from a memory operand, an implementation may fetch only the appropriate 64 bits; however, alignment to 16-byte boundary and normal segment checking will still be enforced.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: T second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.

**Operation**

**UNPCKLPD (128-bit Legacy SSE version)**

\[
\text{DEST}[63:0] \leftarrow \text{SRC1}[63:0] \\
\text{DEST}[127:64] \leftarrow \text{SRC2}[63:0] \\
\text{DEST}[VLMAX-1:128] \text{ (Unmodified)}
\]

**VUNPCKLPD (VEX.128 encoded version)**

\[
\text{DEST}[63:0] \leftarrow \text{SRC1}[63:0] \\
\text{DEST}[127:64] \leftarrow \text{SRC2}[63:0] \\
\text{DEST}[VLMAX-1:128] \leftarrow 0
\]

**VUNPCKLPD (VEX.256 encoded version)**

\[
\text{DEST}[63:0] \leftarrow \text{SRC1}[63:0]
\]
DEST[127:64] ← SRC2[63:0]

**Intel C/C++ Compiler Intrinsic Equivalent**

UNPCKHPD:  __m128d _mm_unpacklo_pd(__m128d a, __m128d b)
UNPCKLPD:  __m256d _mm256_unpacklo_pd(__m256d a, __m256d b)

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4.
UNPCKLPS—Unpack and Interleave Low Packed Single-Precision Floating-Point Values

### Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 14 /r UNPCKLPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Unpacks and Interleaves single-precision floating-point values from low quadwords of xmm1 and xmm2/mem into xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 14 /r VUNPCKLPS xmm1,xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Unpacks and Interleaves single-precision floating-point values from low quadwords of xmm2 and xmm3/m128.</td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 14 /r VUNPCKLPS ymm1,ymm2,ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Unpacks and Interleaves single-precision floating-point values from low quadwords of ymm2 and ymm3/m256.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Performs an interleaved unpack of the low-order single-precision floating-point values from the source operand (second operand) and the destination operand (first operand). See Figure 4-23. The source operand can be an XMM register or a 128-bit memory location; the destination operand is an XMM register.
When unpacking from a memory operand, an implementation may fetch only the appropriate 64 bits; however, alignment to 16-byte boundary and normal segment checking will still be enforced.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: T second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (255:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (255:128) of the corresponding YMM register destination are zeroed.

Operation

**UNPCKLPS (128-bit Legacy SSE version)**

DEST[31:0] ← SRC1[31:0]
DEST[63:32] ← SRC2[31:0]
DEST[95:64] ← SRC1[63:32]
DEST[127:96] ← SRC2[63:32]
DEST[VLMAX-1:128] (Unmodified)

**VUNPCKLPS (VEX.128 encoded version)**

DEST[31:0] ← SRC1[31:0]
DEST[63:32] ← SRC2[31:0]
DEST[95:64] ← SRC1[63:32]
DEST[127:96] ← SRC2[63:63]
DEST[VLMAX-1:128] ← 0
UNPCKLPS (VEX.256 encoded version)
DEST[31:0] ← SRC1[31:0]
DEST[63:32] ← SRC2[31:0]
DEST[95:64] ← SRC1[63:32]
DEST[127:96] ← SRC2[63:32]
DEST[159:128] ← SRC1[159:128]
DEST[255:224] ← SRC2[191:160]

Intel C/C++ Compiler Intrinsic Equivalent
UNPCKLPS:  __m128 _mm_unpacklo_ps(__m128 a, __m128 b)
UNPCKLPS:  __m256 _mm256_unpackl0_ps (__m256 a, __m256 b);

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4.
**VBROADCAST—Load with Broadcast**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.128.66.0F38.W0 18 /r</td>
<td>RM</td>
<td>I/V</td>
<td>AVX</td>
<td>Broadcast single-precision floating-point element in mem to four locations in xmm1.</td>
</tr>
<tr>
<td>VBROADCASTSS xmm1, m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F38.W0 18 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Broadcast single-precision floating-point element in mem to eight locations in ymm1.</td>
</tr>
<tr>
<td>VBROADCASTSS ymm1, m32</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F38.W0 19 /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Broadcast double-precision floating-point element in mem to four locations in ymm1.</td>
</tr>
<tr>
<td>VBROADCASTSD ymm1, m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F38.W0 1A /r</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Broadcast 128 bits of floating-point data in mem to low and high 128-bits in ymm1.</td>
</tr>
<tr>
<td>VBROADCASTF128 ymm1, m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (w)</td>
<td>ModRM/r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Load floating point values from the source operand (second operand) and broadcast to all elements of the destination operand (first operand).

The destination operand is a YMM register. The source operand is either a 32-bit, 64-bit, or 128-bit memory location. Register source encodings are reserved and will #UD.

VBROADCASTSD and VBROADCASTF128 are only supported as 256-bit wide versions. VBROADCASTSS is supported in both 128-bit and 256-bit wide versions.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

If VBROADCASTSD or VBROADCASTF128 is encoded with VEX.L= 0, an attempt to execute the instruction encoded with VEX.L= 0 will cause an #UD exception.
Figure 4-24. VBroadcastSS Operation (VEX.256 encoded version)

Figure 4-25. VBroadcastSS Operation (128-bit version)
**Operation**

**VBROADCASTSS (128 bit version)**
\[
\text{temp} \leftarrow \text{SRC}[31:0] \\
\text{DEST}[31:0] \leftarrow \text{temp} \\
\text{DEST}[63:32] \leftarrow \text{temp} \\
\text{DEST}[95:64] \leftarrow \text{temp} \\
\text{DEST}[127:96] \leftarrow \text{temp} \\
\text{DEST}[\text{VLMAX}-1:128] \leftarrow 0
\]

**VBROADCASTSS (VEX.256 encoded version)**
temp ← SRC[31:0]
DEST[31:0] ← temp
DEST[63:32] ← temp
DEST[95:64] ← temp
DEST[127:96] ← temp
DEST[159:128] ← temp
DEST[191:160] ← temp
DEST[223:192] ← temp
DEST[255:224] ← temp

VBROADCASTSD (VEX.256 encoded version)

temp ← SRC[63:0]
DEST[63:0] ← temp
DEST[127:64] ← temp
DEST[191:128] ← temp
DEST[255:192] ← temp

VBROADCASTF128

temp ← SRC[127:0]
DEST[127:0] ← temp
DEST[VLMAX-1:128] ← temp

Intel C/C++ Compiler Intrinsic Equivalent

VBROADCASTSS: __m128 _mm_broadcast_ss(float *a);
VBROADCASTSS: __m256 _mm256_broadcast_ss(float *a);
VBROADCASTSD: __m256d _mm256_broadcast_sd(double *a);
VBROADCASTF128: __m256 _mm256_broadcast_ps(__m128 * a);
VBROADCASTF128: __m256d _mm256_broadcast_pd(__m128d * a);

Flags Affected
None.

Other Exceptions

See Exceptions Type 6; additionally

#UD If VEX.L = 0 for VBROADCASTSD
If VEX.L = 0 for VBROADCASTF128
If VEX.W = 1.
VCVTPH2PS—Convert 16-bit FP Values to Single-Precision FP Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.256.66.0F38.W0 13 /r</td>
<td>RM</td>
<td>V/V</td>
<td>F16C</td>
<td>Convert eight packed half precision (16-bit) floating-point values in xmm2/m128 to packed single-precision floating-point value in ymm1.</td>
</tr>
<tr>
<td>VCVTPH2PS ymm1, xmm2/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F38.W0 13 /r</td>
<td>RM</td>
<td>V/V</td>
<td>F16C</td>
<td>Convert four packed half precision (16-bit) floating-point values in xmm2/m64 to packed single-precision floating-point value in xmm1.</td>
</tr>
<tr>
<td>VCVTPH2PS xmm1, xmm2/m64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

### Description

Converts four/eight packed half precision (16-bits) floating-point values in the low-order 64/128 bits of an XMM/YMM register or 64/128-bit memory location to four/eight packed single-precision floating-point values and writes the converted values into the destination XMM/YMM register.

If case of a denormal operand, the correct normal result is returned. MXCSR.DAZ is ignored and is treated as if it 0. No denormal exception is reported on MXCSR.

128-bit version: The source operand is a XMM register or 64-bit memory location. The destination operand is a YMM register. The upper bits (255:128) of the corresponding destination YMM register are zeroed.

256-bit version: The source operand is a XMM register or 128-bit memory location. The destination operand is a YMM register.

The diagram below illustrates how data is converted from four packed half precision (in 64 bits) to four single precision (in 128 bits) FP values.

Note: VEX.vvvv is reserved (must be 1111b).
**Operation**

\[
\text{vCvt\_h2s(SRC1[15:0])}
\]

\[
\{
\text{RETURN Cvt\_Half\_Precision\_To\_Single\_Precision(SRC1[15:0]);}
\}
\]

**VCVTPH2PS (VEX.256 encoded version)**

- \( \text{DEST}[31:0] \leftarrow \text{vCvt\_h2s(SRC1[15:0])}; \)
- \( \text{DEST}[63:32] \leftarrow \text{vCvt\_h2s(SRC1[31:16])}; \)
- \( \text{DEST}[95:64] \leftarrow \text{vCvt\_h2s(SRC1[47:32])}; \)
- \( \text{DEST}[127:96] \leftarrow \text{vCvt\_h2s(SRC1[63:48])}; \)
- \( \text{DEST}[159:128] \leftarrow \text{vCvt\_h2s(SRC1[79:64])}; \)
- \( \text{DEST}[191:160] \leftarrow \text{vCvt\_h2s(SRC1[95:80])}; \)
- \( \text{DEST}[223:192] \leftarrow \text{vCvt\_h2s(SRC1[111:96])}; \)
- \( \text{DEST}[255:224] \leftarrow \text{vCvt\_h2s(SRC1[127:112])}; \)

**VCVTPH2PS (VEX.128 encoded version)**

- \( \text{DEST}[31:0] \leftarrow \text{vCvt\_h2s(SRC1[15:0])}; \)
- \( \text{DEST}[63:32] \leftarrow \text{vCvt\_h2s(SRC1[31:16])}; \)
- \( \text{DEST}[95:64] \leftarrow \text{vCvt\_h2s(SRC1[47:32])}; \)
- \( \text{DEST}[127:96] \leftarrow \text{vCvt\_h2s(SRC1[63:48])}; \)
- \( \text{DEST}[VLMAX\,-\,1:128] \leftarrow 0 \)

**Flags Affected**

None
Intel C/C++ Compiler Intrinsic Equivalent

__m128_mm_cvtph_ps(__m128i m1);
__m256_mm256_cvtph_ps(__m128i m1)

SIMD Floating-Point Exceptions
Invalid

Other Exceptions
Exceptions Type 11 (do not report #AC); additionally
#UD If VEX.W=1.
VCVTPS2PH—Convert Single-Precision FP value to 16-bit FP value

Opcode/Instruction

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.256.66.0F3A.W0 1D / r ib</td>
<td>MR</td>
<td>V/V</td>
<td>F16C</td>
<td>Convert eight packed single-precision floating-point value in ymm2 to packed half-precision (16-bit) floating-point value in xmm1/mem. Imm8 provides rounding controls.</td>
</tr>
<tr>
<td>VCVTPS2PH xmm1/m128, ymm2, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.128.66.0F3A.W0.1D / r ib</td>
<td>MR</td>
<td>V/V</td>
<td>F16C</td>
<td>Convert four packed single-precision floating-point value in xmm2 to packed half-precision (16-bit) floating-point value in xmm1/mem. Imm8 provides rounding controls.</td>
</tr>
<tr>
<td>VCVTPS2PH xmm1/m64, xmm2, imm8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM:r/m (w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Convert four or eight packed single-precision floating values in first source operand to four or eight packed half-precision (16-bit) floating-point values. The rounding mode is specified using the immediate field (imm8).

Underflow results (i.e. tiny results) are converted to denormals. MXCSR.FTZ is ignored. If a source element is denormal relative to input format with DM masked and at least one of PM or UM unmasked; a SIMD exception will be raised with DE, UE and PE set.

128-bit version: The source operand is a XMM register. The destination operand is a XMM register or 64-bit memory location. If destination operand is a register then the upper bits (255:64) of corresponding YMM register are zeroed.

256-bit version: The source operand is a YMM register. The destination operand is a XMM register or 128-bit memory location. If the destination operand is a register, the upper bits (255:128) of the corresponding YMM register are zeroed.

Note: VEX.vvvv is reserved (must be 1111b).
The diagram below illustrates how data is converted from four packed single precision (in 128 bits) to four half precision (in 64 bits) FP values.

![Figure 4-29. VCVTPS2PH (128-bit Version)](image)

The immediate byte defines several bit fields that controls rounding operation. The effect and encoding of RC field are listed in Table 4-21.

Table 4-21. Immediate Byte Encoding for 16-bit Floating-Point Conversion Instructions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Field Name/value</th>
<th>Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Imm[1:0]</td>
<td>RC=00B</td>
<td>Round to nearest even</td>
<td>If Imm[2] = 0</td>
</tr>
<tr>
<td></td>
<td>RC=01B</td>
<td>Round down</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RC=10B</td>
<td>Round up</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RC=11B</td>
<td>Truncate</td>
<td></td>
</tr>
<tr>
<td>Imm[2]</td>
<td>MS1=0</td>
<td>Use imm[1:0] for rounding</td>
<td>Ignore MXCSR.RC</td>
</tr>
<tr>
<td></td>
<td>MS1=1</td>
<td>Use MXCSR.RC for rounding</td>
<td></td>
</tr>
<tr>
<td>Imm[7:3]</td>
<td>Ignored</td>
<td>Ignored by processor</td>
<td></td>
</tr>
</tbody>
</table>

Operation

```c
vCvt_s2h(SRC1[31:0])
{
    IF Imm[2] = 0
        THEN // using Imm[1:0] for rounding control, see Table 4-21
            RETURN Cvt_Single_Precision_To_Half_Precision_FP_Imm(SRC1[31:0]);
    ELSE // using MXCSR.RC for rounding control
        RETURN Cvt_Single_Precision_To_Half_Precision_FP_Mxcsr(SRC1[31:0]);
    FI;
}
```

VCVTPS2PH—Convert Single-Precision FP value to 16-bit FP value
VCVTPS2PH (VEX.256 encoded version)
DEST[15:0] ← vCvt_s2h(SRC1[31:0]);
DEST[31:16] ← vCvt_s2h(SRC1[63:32]);
DEST[47:32] ← vCvt_s2h(SRC1[95:64]);
DEST[63:48] ← vCvt_s2h(SRC1[127:96]);
DEST[79:64] ← vCvt_s2h(SRC1[159:128]);
DEST[95:80] ← vCvt_s2h(SRC1[191:160]);
DEST[111:96] ← vCvt_s2h(SRC1[223:192]);
DEST[127:112] ← vCvt_s2h(SRC1[255:224]);
DEST[255:128] ← 0

VCVTPS2PH (VEX.128 encoded version)
DEST[15:0] ← vCvt_s2h(SRC1[31:0]);
DEST[31:16] ← vCvt_s2h(SRC1[63:32]);
DEST[47:32] ← vCvt_s2h(SRC1[95:64]);
DEST[63:48] ← vCvt_s2h(SRC1[127:96]);
DEST[VLMAX-1:64] ← 0

Flags Affected
None

Intel C/C++ Compiler Intrinsic Equivalent
__m128i _mm_cvtps_ph ( __m128 m1, const int imm);
__m128i _mm256_cvtps_ph(__m256 m1, const int imm);

SIMD Floating-Point Exceptions
Invalid, Underflow, Overflow, Precision, Denormal (if MXCSR.DAZ=0);

Other Exceptions
Exceptions Type 11 (do not report #AC); additionally
#UD If VEX.W=1.
VERR/VERW—Verify a Segment for Reading or Writing

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /4</td>
<td>VERR r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set ZF=1 if segment specified with r/m16 can be read.</td>
</tr>
<tr>
<td>0F 00 /5</td>
<td>VERW r/m16</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Set ZF=1 if segment specified with r/m16 can be written.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM: r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Verifies whether the code or data segment specified with the source operand is readable (VERR) or writable (VERW) from the current privilege level (CPL). The source operand is a 16-bit register or a memory location that contains the segment selector for the segment to be verified. If the segment is accessible and readable (VERR) or writable (VERW), the ZF flag is set; otherwise, the ZF flag is cleared. Code segments are never verified as writable. This check cannot be performed on system segments.

To set the ZF flag, the following conditions must be met:

- The segment selector is not NULL.
- The selector must denote a descriptor within the bounds of the descriptor table (GDT or LDT).
- The selector must denote the descriptor of a code or data segment (not that of a system segment or gate).
- For the VERR instruction, the segment must be readable.
- For the VERW instruction, the segment must be a writable data segment.
- If the segment is not a conforming code segment, the segment’s DPL must be greater than or equal to (have less or the same privilege as) both the CPL and the segment selector’s RPL.

The validation performed is the same as is performed when a segment selector is loaded into the DS, ES, FS, or GS register, and the indicated access (read or write) is performed. The segment selector’s value cannot result in a protection exception, enabling the software to anticipate possible segment access problems.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode. The operand size is fixed at 16 bits.
INSTRUCTION SET REFERENCE, M-Z

Operation

IF SRC(Offset) > (GDTR(Limit) or (LDTR(Limit))
  THEN ZF ← 0; Fl;

Read segment descriptor;

IF SegmentDescriptor(DescriptorType) = 0 (* System segment *)
  or (SegmentDescriptor(Type) ≠ conforming code segment)
  and (CPL > DPL) or (RPL > DPL)
  THEN
  ZF ← 0;
ELSE
  IF ((Instruction = VERR) and (Segment readable))
    or ((Instruction = VERW) and (Segment writable))
  THEN
    ZF ← 1;
  FI;
FI;

Flags Affected
The ZF flag is set to 1 if the segment is accessible and readable (VERR) or writable (VERW); otherwise, it is set to 0.

Protected Mode Exceptions
The only exceptions generated for these instructions are those related to illegal addressing of the source operand.

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  If the DS, ES, FS, or GS register is used to access memory and it contains a NULL segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#UD The VERR and VERW instructions are not recognized in real-address mode.
  If the LOCK prefix is used.

4-630  Vol. 2B  VERR/VERw—Verify a Segment for Reading or Writing
**Virtual-8086 Mode Exceptions**

#UD The VERR and VERW instructions are not recognized in virtual-8086 mode.
If the LOCK prefix is used.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used.
VEXTRACTF128 — Extract Packed Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEXTRACTF128 xmm1/m128, ymm2, imm8</td>
<td>MR</td>
<td>V/V</td>
<td>AVX</td>
<td>Extract 128 bits of packed floating-point values from ymm2 and store results in xmm1/mem.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRMr/m (w)</td>
<td>ModRMreg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Extracts 128-bits of packed floating-point values from the source operand (second operand) at an 128-bit offset from imm8[0] into the destination operand (first operand). The destination may be either an XMM register or an 128-bit memory location.

VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD.

The high 7 bits of the immediate are ignored.

If VEXTRACTF128 is encoded with VEX.L= 0, an attempt to execute the instruction encoded with VEX.L= 0 will cause an #UD exception.

**Operation**

**VEXTRACTF128 (memory destination form)**

CASE (imm8[0]) OF

0: DEST[127:0] ← SRC1[127:0]
1: DEST[127:0] ← SRC1[255:128]

ESAC.

**VEXTRACTF128 (register destination form)**

CASE (imm8[0]) OF

0: DEST[127:0] ← SRC1[127:0]
1: DEST[127:0] ← SRC1[255:128]

ESAC.

DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

VEXTRACTF128: __m128 __mm256_extractf128_ps (__m256 a, int offset);
VEXTRACTF128: __m128d_mm256_extractf128_pd(__m256d a, int offset);
VEXTRACTF128: __m128i_mm256_extractf128_si256(__m256i a, int offset);

**SIMD Floating-Point Exceptions**
None

**Other Exceptions**
See Exceptions Type 6; additionally
#UD
  If VEX.L = 0
  If VEX.W = 1.
VINSERTF128 — Insert Packed Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.NDS.256.66.0F3A.W0 18 /r ib</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Insert a single precision floating-point value selected by imm8 from xmm2/m32 into xmm1 at the specified destination element specified by imm8 and zero out destination elements in xmm1 as indicated in imm8.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs an insertion of 128-bits of packed floating-point values from the second source operand (third operand) into an the destination operand (first operand) at an 128-bit offset from imm8[0]. The remaining portions of the destination are written by the corresponding fields of the first source operand (second operand). The second source operand can be either an XMM register or a 128-bit memory location. The high 7 bits of the immediate are ignored.

**Operation**

\[
\text{TEMP}[255:0] \leftarrow \text{SRC1}[255:0] \\
\text{CASE (imm8[0]) OF} \\
\quad 0: \text{TEMP}[127:0] \leftarrow \text{SRC2}[127:0] \\
\quad 1: \text{TEMP}[255:128] \leftarrow \text{SRC2}[127:0] \\
\text{ESAC} \\
\text{DEST} \leftarrow \text{TEMP}
\]

**Intel C/C++ Compiler Intrinsic Equivalent**

\[
\text{INSERTF128: } \quad \_\_\_m256\text{-}\_\_\_m256\_insertf128\_ps (\_\_\_m256 a, \_\_\_m128 b, \text{int offset}); \\
\text{INSERTF128: } \quad \_\_\_m256d\text{-}\_\_\_m256\_insertf128\_pd (\_\_\_m256d a, \_\_\_m128d b, \text{int offset}); \\
\text{INSERTF128: } \quad \_\_\_m256i\text{-}\_\_\_m256\_insertf128\_si256 (\_\_\_m256i a, \_\_\_m128i b, \text{int offset});
\]
**SIMD Floating-Point Exceptions**
None

**Other Exceptions**
See Exceptions Type 6; additionally
#UD If VEX.W = 1.
VMASKMOV—Conditional SIMD Packed Loads and Stores

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.NDS.128.66.0F38.W0 2C /r VMASKMOVPS xmm1, xmm2, m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Conditionally load packed single-precision values from m128 using mask in xmm2 and store in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F38.W0 2C /r VMASKMOVPS ymm1, ymm2, m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Conditionally load packed single-precision values from m256 using mask in ymm2 and store in ymm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.W0 2D /r VMASKMOVPD xmm1, xmm2, m128</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Conditionally load packed double-precision values from m128 using mask in xmm2 and store in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F38.W0 2D /r VMASKMOVPD ymm1, ymm2, m256</td>
<td>RVM V/V</td>
<td>AVX</td>
<td>Conditionally load packed double-precision values from m256 using mask in ymm2 and store in ymm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.W0 2E /r VMASKMOVPS m128, xmm1, xmm2</td>
<td>MVR V/V</td>
<td>AVX</td>
<td>Conditionally store packed single-precision values from xmm2 using mask in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F38.W0 2E /r VMASKMOVPS m256, ymm1, ymm2</td>
<td>MVR V/V</td>
<td>AVX</td>
<td>Conditionally store packed single-precision values from ymm2 using mask in ymm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F38.W0 2F /r VMASKMOVPD m128, xmm1, xmm2</td>
<td>MVR V/V</td>
<td>AVX</td>
<td>Conditionally store packed double-precision values from xmm2 using mask in xmm1.</td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F38.W0 2F /r VMASKMOVPD m256, ymm1, ymm2</td>
<td>MVR V/V</td>
<td>AVX</td>
<td>Conditionally store packed double-precision values from ymm2 using mask in ymm1.</td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
<tr>
<td>MVR</td>
<td>ModRM:r/m (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>
Description

Conditionally moves packed data elements from the second source operand into the corresponding data element of the destination operand, depending on the mask bits associated with each data element. The mask bits are specified in the first source operand.

The mask bit for each data element is the most significant bit of that element in the first source operand. If a mask is 1, the corresponding data element is copied from the second source operand to the destination operand. If the mask is 0, the corresponding data element is set to zero in the load form of these instructions, and unmodified in the store form.

The second source operand is a memory address for the load form of these instructions. The destination operand is a memory address for the store form of these instructions. The other operands are both XMM registers (for VEX.128 version) or YMM registers (for VEX.256 version).

Faults occur only due to mask-bit required memory accesses that caused the faults. Faults will not occur due to referencing any memory location if the corresponding mask bit for that memory location is 0. For example, no faults will be detected if the mask bits are all zero.

Unlike previous MASKMOV instructions (MASKMOVQ and MASKMOVDQU), a non-temporal hint is not applied to these instructions.

Instruction behavior on alignment check reporting with mask bits of less than all 1s are the same as with mask bits of all 1s.

VMASKMOV should not be used to access memory mapped I/O and un-cached memory as the access and the ordering of the individual loads or stores it does is implementation specific.

In cases where mask bits indicate data should not be loaded or stored paging A and D bits will be set in an implementation dependent way. However, A and D bits are always set for pages where data is actually loaded/stored.

Note: for load forms, the first source (the mask) is encoded in VEX.vvvv; the second source is encoded in rm_field, and the destination register is encoded in reg_field.

Note: for store forms, the first source (the mask) is encoded in VEX.vvvv; the second source register is encoded in reg_field, and the destination memory location is encoded in rm_field.

Operation

VMASKMOVPS - 128-bit load

\[
\begin{align*}
\text{DEST}[31:0] & \leftarrow \text{IF (SRC1[31]) Load}_32(\text{mem}) \text{ ELSE 0} \\
\text{DEST}[63:32] & \leftarrow \text{IF (SRC1[63]) Load}_32(\text{mem} + 4) \text{ ELSE 0} \\
\text{DEST}[95:64] & \leftarrow \text{IF (SRC1[95]) Load}_32(\text{mem} + 8) \text{ ELSE 0} \\
\text{DEST}[127:97] & \leftarrow \text{IF (SRC1[127]) Load}_32(\text{mem} + 12) \text{ ELSE 0} \\
\text{DEST}[\text{VLMAX}-1:128] & \leftarrow 0 \\
\text{DEST}[31:0] & \leftarrow \text{IF (SRC1[31]) Load}_32(\text{mem}) \text{ ELSE 0}
\end{align*}
\]
VMASKMOV—Conditional SIMD Packed Loads and Stores

**VMASKMOV—Conditional SIMD Packed Loads and Stores**

DEST[63:32] \( \leftarrow \) IF (SRC1[63]) Load_32(mem + 4) ELSE 0
DEST[95:64] \( \leftarrow \) IF (SRC1[95]) Load_32(mem + 8) ELSE 0
DEST[127:96] \( \leftarrow \) IF (SRC1[127]) Load_32(mem + 12) ELSE 0
DEST[159:128] \( \leftarrow \) IF (SRC1[159]) Load_32(mem + 16) ELSE 0
DEST[191:160] \( \leftarrow \) IF (SRC1[191]) Load_32(mem + 20) ELSE 0
DEST[223:192] \( \leftarrow \) IF (SRC1[223]) Load_32(mem + 24) ELSE 0
DEST[255:224] \( \leftarrow \) IF (SRC1[255]) Load_32(mem + 28) ELSE 0

**VMASKMOVPD - 128-bit load**
DEST[63:0] \( \leftarrow \) IF (SRC1[63]) Load_64(mem) ELSE 0
DEST[127:64] \( \leftarrow \) IF (SRC1[127]) Load_64(mem + 16) ELSE 0
DEST[VLMAX-1:128] \( \leftarrow \) 0

**VMASKMOVPD - 256-bit load**
DEST[63:0] \( \leftarrow \) IF (SRC1[63]) Load_64(mem) ELSE 0
DEST[127:64] \( \leftarrow \) IF (SRC1[127]) Load_64(mem + 8) ELSE 0
DEST[195:128] \( \leftarrow \) IF (SRC1[191]) Load_64(mem + 16) ELSE 0
DEST[255:196] \( \leftarrow \) IF (SRC1[255]) Load_64(mem + 24) ELSE 0

**VMASKMOVPS - 128-bit store**
IF (SRC1[31]) DEST[31:0] \( \leftarrow \) SRC2[31:0]
IF (SRC1[63]) DEST[63:32] \( \leftarrow \) SRC2[63:32]
IF (SRC1[95]) DEST[95:64] \( \leftarrow \) SRC2[95:64]
IF (SRC1[127]) DEST[127:96] \( \leftarrow \) SRC2[127:96]

**VMASKMOVPS - 256-bit store**
IF (SRC1[31]) DEST[31:0] \( \leftarrow \) SRC2[31:0]
IF (SRC1[63]) DEST[63:32] \( \leftarrow \) SRC2[63:32]
IF (SRC1[95]) DEST[95:64] \( \leftarrow \) SRC2[95:64]
IF (SRC1[127]) DEST[127:96] \( \leftarrow \) SRC2[127:96]
IF (SRC1[159]) DEST[159:128] \( \leftarrow \) SRC2[159:128]
IF (SRC1[191]) DEST[191:160] \( \leftarrow \) SRC2[191:160]
IF (SRC1[223]) DEST[223:192] \( \leftarrow \) SRC2[223:192]
IF (SRC1[255]) DEST[255:224] \( \leftarrow \) SRC2[255:224]

**VMASKMOVPD - 128-bit store**
IF (SRC1[63]) DEST[63:0] \( \leftarrow \) SRC2[63:0]
IF (SRC1[127]) DEST[127:64] \( \leftarrow \) SRC2[127:64]

**VMASKMOVPD - 256-bit store**
IF (SRC1[63]) DEST[63:0] \( \leftarrow \) SRC2[63:0]
IF (SRC1[127]) DEST[127:64] \( \leftarrow \) SRC2[127:64]
VMASKMOVPS - 256-bit load
IF (SRC1[255]) DEST[255:192] ← SRC2[255:192]

Intel C/C++ Compiler Intrinsic Equivalent
__m256 _mm256_maskload_ps(float const *a, __m256i mask)
void _mm256_maskstore_ps(float *a, __m256i mask, __m256 b)
__m256d _mm256_maskload_pd(double *a, __m256i mask);
void _mm256_maskstore_pd(double *a, __m256i mask, __m256d b);
__m128 _mm128_maskload_ps(float const *a, __m128i mask)
void _mm128_maskstore_ps(float *a, __m128i mask, __m128 b)
__m128d _mm128_maskload_pd(double *a, __m128i mask);
void _mm128_maskstore_pd(double *a, __m128i mask, __m128d b);

SIMD Floating-Point Exceptions
None

Other Exceptions
See Exceptions Type 6 (No AC# reported for any mask bit combinations);
additionally
#UD If VEX.W = 1.
### VPERMILPD — Permute Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.NDS.128.66.0F38.W0 0D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Permute double-precision floating-point values in xmm2 using controls from xmm3/mem and store result in xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F38.W0 0D /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Permute double-precision floating-point values in ymm2 using controls from ymm3/mem and store result in ymm1.</td>
</tr>
<tr>
<td>VEX.128.66.0F3A.W0 05 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Permute double-precision floating-point values in xmm2/mem using controls from imm8.</td>
</tr>
<tr>
<td>VEX.256.66.0F3A.W0 05 /r ib</td>
<td>RMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Permute double-precision floating-point values in ymm2/mem using controls from imm8.</td>
</tr>
</tbody>
</table>

#### InstructionOperand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMr/m (r)</td>
<td>NA</td>
</tr>
<tr>
<td>RMI</td>
<td>ModRMreg (w)</td>
<td>ModRMr/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Description

Permute double-precision floating-point values in the first source operand (second operand) using 8-bit control fields in the low bytes of the second source operand (third operand) and store results in the destination operand (first operand). The first source operand is a YMM register, the second source operand is a YMM register or a 256-bit memory location, and the destination operand is a YMM register.
VPERMILPD — Permute Double-Precision Floating-Point Values

There is one control byte per destination double-precision element. Each control byte is aligned with the low 8 bits of the corresponding double-precision destination element. Each control byte contains a 1-bit select field (see Figure 4-31) that determines which of the source elements are selected. Source elements are restricted to lie in the same source 128-bit region as the destination.

Figure 4-30. VPERMILPD operation

Permute double-precision floating-point values in the first source operand (second operand) using two, 1-bit control fields in the low 2 bits of the 8-bit immediate and store results in the destination operand (first operand). The source operand is a YMM register or 256-bit memory location and the destination operand is a YMM register.

Note: For the VEX.128.66.0F3A 05 instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.

Figure 4-31. VPERMILPD Shuffle Control

(immediate control version)
Note: For the VEX.256.66.0F3A 05 instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.

**Operation**

**VPERMILPD (256-bit immediate version)**
- IF (imm8[0] = 0) THEN DEST[63:0] ← SRC1[63:0]
- IF (imm8[0] = 1) THEN DEST[63:0] ← SRC1[127:64]
- IF (imm8[1] = 0) THEN DEST[127:64] ← SRC1[127:64]

**VPERMILPD (128-bit immediate version)**
- IF (imm8[0] = 0) THEN DEST[63:0] ← SRC1[63:0]
- IF (imm8[0] = 1) THEN DEST[63:0] ← SRC1[127:64]
- IF (imm8[1] = 0) THEN DEST[127:64] ← SRC1[63:0]

**VPERMILPD (256-bit variable version)**
- IF (SRC2[1] = 0) THEN DEST[63:0] ← SRC1[63:0]
- IF (SRC2[1] = 1) THEN DEST[63:0] ← SRC1[127:64]
- IF (SRC2[65] = 0) THEN DEST[127:64] ← SRC1[63:0]
- IF (SRC2[65] = 1) THEN DEST[127:64] ← SRC1[127:64]

**VPERMILPD (128-bit variable version)**
- IF (SRC2[1] = 0) THEN DEST[63:0] ← SRC1[63:0]
- IF (SRC2[1] = 1) THEN DEST[63:0] ← SRC1[127:64]
- IF (SRC2[65] = 0) THEN DEST[127:64] ← SRC1[63:0]
- IF (SRC2[65] = 1) THEN DEST[127:64] ← SRC1[127:64]
- DEST[VLMAX-1:128] ← 0

**Intel C/C++ Compiler Intrinsic Equivalent**

VPERMILPD:  __m128d _mm_permute_pd (__m128d a, int control)
VPERMILPD:  __m256d _mm256_permute_pd (__m256d a, int control)
VPERMILPD: __m128d_mm_permutevar_pd(__m128d a, __m128i control);
VPERMILPD: __m256d_mm256_permutevar_pd(__m256d a, __m256i control);

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 6; additionally
#UD If VEX.W = 1
VPERMILPS — Permute Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.NDS.128.66.0F38.W0 0C /r VPERMILPS xmm1, xmm2, xmm3/m128</td>
<td>RVM V/V AVX</td>
<td>Permute single-precision floating-point values in xmm2 using controls from xmm3/mem and store result in xmm1.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.128.66.0F3A.W0 04 /r ib VPERMILPS xmm1, xmm2/m128, imm8</td>
<td>RMI V/V AVX</td>
<td>Permute single-precision floating-point values in xmm2/mem using controls from imm8 and store result in xmm1.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F38.W0 0C /r VPERMILPS ymm1, ymm2, ymm3/m256</td>
<td>RVM V/V AVX</td>
<td>Permute single-precision floating-point values in ymm2 using controls from ymm3/mem and store result in ymm1.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.256.66.0F3A.W0 04 /r ib VPERMILPS ymm1, ymm2/m256, imm8</td>
<td>RMI V/V AVX</td>
<td>Permute single-precision floating-point values in ymm2/mem using controls from imm8 and store result in ymm1.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
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<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
<tr>
<td>RMI</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
(variable control version)
Permute single-precision floating-point values in the first source operand (second operand) using 8-bit control fields in the low bytes of corresponding elements the shuffle control (third operand) and store results in the destination operand (first operand). The first source operand is a YMM register, the second source operand is a YMM register or a 256-bit memory location, and the destination operand is a YMM register.
VPERMILPS — Permute Single-Precision Floating-Point Values

There is one control byte per destination single-precision element. Each control byte is aligned with the low 8 bits of the corresponding single-precision destination element. Each control byte contains a 2-bit select field (see Figure 4-33) that determines which of the source elements are selected. Source elements are restricted to lie in the same source 128-bit region as the destination.

(Immediate control version)

Permute single-precision floating-point values in the first source operand (second operand) using four 2-bit control fields in the 8-bit immediate and store results in the destination operand (first operand). The source operand is a YMM register or 256-bit memory location and the destination operand is a YMM register. This is similar to a wider version of PSHUF, just operating on single-precision floating-point values.

Note: For the VEX.128.66.0F3A 04 instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.
INSTRUCTION SET REFERENCE, M-Z

Note: For the VEX.256.66.0F3A 04 instruction version, VEX.vvvv is reserved and must be 1111b otherwise instruction will #UD.

Operation

Select4(SRC, control) {
CASE (control[1:0]) OF
  0: TMP ← SRC[31:0];
  1: TMP ← SRC[63:32];
  2: TMP ← SRC[95:64];
  3: TMP ← SRC[127:96];
ESAC;
RETURN TMP
}

VPERMILPS (256-bit immediate version)
DEST[31:0] ← Select4(SRC1[127:0], imm8[1:0]);
DEST[63:32] ← Select4(SRC1[127:0], imm8[3:2]);
DEST[95:64] ← Select4(SRC1[127:0], imm8[5:4]);
DEST[127:96] ← Select4(SRC1[127:0], imm8[7:6]);
DEST[159:128] ← Select4(SRC1[255:128], imm8[1:0]);
DEST[255:224] ← Select4(SRC1[255:128], imm8[7:6]);

VPERMILPS (128-bit immediate version)
DEST[31:0] ← Select4(SRC1[127:0], imm8[1:0]);
DEST[63:32] ← Select4(SRC1[127:0], imm8[3:2]);
DEST[95:64] ← Select4(SRC1[127:0], imm8[5:4]);
DEST[127:96] ← Select4(SRC1[127:0], imm8[7:6]);
DEST[VLMAX-1:128] ← 0

VPERMILPS (256-bit variable version)
DEST[31:0] ← Select4(SRC1[127:0], SRC2[1:0]);
DEST[63:32] ← Select4(SRC1[127:0], SRC2[33:32]);
DEST[95:64] ← Select4(SRC1[127:0], SRC2[65:64]);
DEST[127:96] ← Select4(SRC1[127:0], SRC2[97:96]);
DEST[255:224] ← Select4(SRC1[255:128], SRC2[225:224]);

VPERMILPS (128-bit variable version)
VPERMILPS — Permute Single-Precision Floating-Point Values

DEST[31:0]  \leftarrow \text{Select4}(SRC1[127:0], SRC2[1:0]);
DEST[63:32]  \leftarrow \text{Select4}(SRC1[127:0], SRC2[33:32]);
DEST[95:64]  \leftarrow \text{Select4}(SRC1[127:0], SRC2[65:64]);
DEST[127:96] \leftarrow \text{Select4}(SRC1[127:0], SRC2[97:96]);
DEST[VLMAX-1:128] \leftarrow 0

Intel C/C++ Compiler Intrinsic Equivalent

VPERMILPS: \texttt{__m128 \_mm\_permute\_ps (\_m128 a, int control);} 
VPERMILPS: \texttt{__m256 \_mm256\_permute\_ps (\_m256 a, int control);} 
VPERMILPS: \texttt{__m128 \_mm\_permutevar\_ps (\_m128 a, \_m128i control);} 
VPERMILPS: \texttt{__m256 \_mm256\_permutevar\_ps (\_m256 a, \_m256i control);} 

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 6; additionally
#UD \texttt{If VEX.W = 1.}
VPERMF2128 — Permute Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.NDS.256.66.0F3A.W0 /r ib</td>
<td>RVMI</td>
<td>V/V</td>
<td>AVX</td>
<td>Permute 128-bit floating-point fields in ymm2 and ymm3/mem using controls from imm8 and store result in ymm1.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RVMI</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>imm8</td>
</tr>
</tbody>
</table>

Description

Permute 128 bit floating-point-containing fields from the first source operand (second operand) and second source operand (third operand) using bits in the 8-bit immediate and store results in the destination operand (first operand). The first source operand is a YMM register, the second source operand is a YMM register or a 256-bit memory location, and the destination operand is a YMM register.

Figure 4-34. VPERMF2128 Operation
Imm8[1:0] select the source for the first destination 128-bit field, imm8[5:4] select
the source for the second destination field. If imm8[3] is set, the low 128-bit field is
zeroed. If imm8[7] is set, the high 128-bit field is zeroed.
VEX.L must be 1, otherwise the instruction will #UD.

**Operation**

**VPERM2F128**
CASE IMM8[1:0] of
0: DEST[127:0] ← SRC1[127:0]
1: DEST[127:0] ← SRC1[255:128]
2: DEST[127:0] ← SRC2[127:0]
ESAC

CASE IMM8[5:4] of
0: DEST[255:128] ← SRC1[127:0]
2: DEST[255:128] ← SRC2[127:0]
ESAC

IF (imm8[3])
DEST[127:0] ← 0
FI

IF (imm8[7])
DEST[VLMAX-1:128] ← 0
FI

**Intel C/C++ Compiler Intrinsic Equivalent**

VPERM2F128: __m256 _mm256_permute2f128_ps (__m256 a, __m256 b, int control)
VPERM2F128: __m256d _mm256_permute2f128_pd (__m256d a, __m256d b, int control)
VPERM2F128: __m256i _mm256_permute2f128_si256 (__m256i a, __m256i b, int control)

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 6; additionally
#UD If VEX.L = 0

VPERM2F128 — Permute Floating-Point Values
If VEX.W = 1.
**Instruction Set Reference, M-Z**

**VTESTPD/VTESTPS—Packed Bit Test**

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.128.66.0F38.W0 0E /r VTESTPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Set ZF and CF depending on sign bit AND and ANDN of packed single-precision floating-point sources.</td>
</tr>
<tr>
<td>VEX.256.66.0F38.W0 0E /r VTESTPS ymm1, ymm2/m256</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Set ZF and CF depending on sign bit AND and ANDN of packed single-precision floating-point sources.</td>
</tr>
<tr>
<td>VEX.128.66.0F38.W0 0F /r VTESTPD xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Set ZF and CF depending on sign bit AND and ANDN of packed double-precision floating-point sources.</td>
</tr>
<tr>
<td>VEX.256.66.0F38.W0 0F /r VTESTPD ymm1, ymm2/m256</td>
<td>RM</td>
<td>V/V</td>
<td>AVX</td>
<td>Set ZF and CF depending on sign bit AND and ANDN of packed double-precision floating-point sources.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

VTESTPS performs a bitwise comparison of all the sign bits of the packed single-precision elements in the first source operation and corresponding sign bits in the second source operand. If the AND of the source sign bits with the dest sign bits produces all zeros, the ZF is set else the ZF is clear. If the AND of the source sign bits with the inverted dest sign bits produces all zeros the CF is set else the CF is clear. An attempt to execute VTESTPS with VEX.W=1 will cause #UD.

VTESTPD performs a bitwise comparison of all the sign bits of the double-precision elements in the first source operation and corresponding sign bits in the second source operand. If the AND of the source sign bits with the dest sign bits produces all zeros, the ZF is set else the ZF is clear. If the AND the source sign bits with the inverted dest sign bits produces all zeros the CF is set else the CF is clear. An attempt to execute VTESTPS with VEX.W=1 will cause #UD.

The first source register is specified by the ModR/M reg field.
INSTRUCTION SET REFERENCE, M-Z

128-bit version: The first source register is an XMM register. The second source register can be an XMM register or a 128-bit memory location. The destination register is not modified.

VEX.256 encoded version: The first source register is a YMM register. The second source register can be a YMM register or a 256-bit memory location. The destination register is not modified.

Note: In VEX-encoded versions, VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD.

Operation

VTESTPS (128-bit version)
TEMP[127:0] ← SRC[127:0] AND DEST[127:0]
IF (TEMP[31] = TEMP[63] = TEMP[95] = TEMP[127] = 0)
    THEN ZF ← 1;
    ELSE ZF ← 0;

TEMP[127:0] ← SRC[127:0] AND NOT DEST[127:0]
IF (TEMP[31] = TEMP[63] = TEMP[95] = TEMP[127] = 0)
    THEN CF ← 1;
    ELSE CF ← 0;
DEST (unmodified)
AF ← OF ← PF ← SF ← 0;

VTESTPS (VEX.256 encoded version)
TEMP[255:0] ← SRC[255:0] AND DEST[255:0]
    THEN ZF ← 1;
    ELSE ZF ← 0;

TEMP[255:0] ← SRC[255:0] AND NOT DEST[255:0]
    THEN CF ← 1;
    ELSE CF ← 0;
DEST (unmodified)
AF ← OF ← PF ← SF ← 0;

VTESTPD (128-bit version)
TEMP[127:0] ← SRC[127:0] AND DEST[127:0]
IF (TEMP[63] = TEMP[127] = 0)
    THEN ZF ← 1;
ELSE ZF ← 0;

TEMP[127:0] ← SRC[127:0] AND NOT DEST[127:0]
IF (TEMP[63] = TEMP[127] = 0)
    THEN CF ← 1;
    ELSE CF ← 0;
DEST (unmodified)
AF ← OF ← PF ← SF ← 0;

VTESTPD (VEX.256 encoded version)
TEMP[255:0] ← SRC[255:0] AND DEST[255:0]
    THEN ZF ← 1;
    ELSE ZF ← 0;

TEMP[255:0] ← SRC[255:0] AND NOT DEST[255:0]
    THEN CF ← 1;
    ELSE CF ← 0;
DEST (unmodified)
AF ← OF ← PF ← SF ← 0;

Intel C/C++ Compiler Intrinsic Equivalent

VTESTPS

int __mm256_testz_ps (__m256 s1, __m256 s2);
int __mm256_testc_ps (__m256 s1, __m256 s2);
int __mm256_testnzc_ps (__m256 s1, __m128 s2);
int __mm_testz_ps (__m128 s1, __m128 s2);
int __mm_testc_ps (__m128 s1, __m128 s2);
int __mm_testnzc_ps (__m128 s1, __m128 s2);

VTESTPD

int __mm256_testz_pd (__m256d s1, __m256d s2);
int __mm256_testc_pd (__m256d s1, __m256d s2);
int __mm256_testnzc_pd (__m256d s1, __m256d s2);
**INSTRUCTION SET REFERENCE, M-Z**

```c
int _mm_testz_pd(__m128d s1, __m128d s2);
int _mm_testc_pd(__m128d s1, __m128d s2);
int _mm_testnzc_pd(__m128d s1, __m128d s2);
```

**Flags Affected**
The OF, AF, PF, SF flags are cleared and the ZF, CF flags are set according to the operation.

**SIMD Floating-Point Exceptions**
None.

**Other Exceptions**
See Exceptions Type 4; additionally

#UD If VEX.vvvv != 1111B.

If VEX.W = 1 for VTESTPS or VTESTPD.
VZEROALL—Zero All YMM Registers

<table>
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<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.256.0F.WIG 77</td>
<td>NP</td>
<td>V/V</td>
<td>AVX</td>
<td>Zero all YMM registers.</td>
</tr>
<tr>
<td>VZEROALL</td>
<td>NA</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

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<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
The instruction zeros contents of all XMM or YMM registers.

Note: VEX.vvvv is reserved and must be 1111b, otherwise instructions will #UD. In Compatibility and legacy 32-bit mode only the lower 8 registers are modified.

Operation

VZEROALL (VEX.256 encoded version)

IF (64-bit mode)

\[
\begin{align*}
YMM0[VMAX-1:0] & \leftarrow 0 \\
YMM1[VMAX-1:0] & \leftarrow 0 \\
YMM2[VMAX-1:0] & \leftarrow 0 \\
YMM3[VMAX-1:0] & \leftarrow 0 \\
YMM4[VMAX-1:0] & \leftarrow 0 \\
YMM5[VMAX-1:0] & \leftarrow 0 \\
YMM6[VMAX-1:0] & \leftarrow 0 \\
YMM7[VMAX-1:0] & \leftarrow 0 \\
YMM8[VMAX-1:0] & \leftarrow 0 \\
YMM9[VMAX-1:0] & \leftarrow 0 \\
YMM10[VMAX-1:0] & \leftarrow 0 \\
YMM11[VMAX-1:0] & \leftarrow 0 \\
YMM12[VMAX-1:0] & \leftarrow 0 \\
YMM13[VMAX-1:0] & \leftarrow 0 \\
YMM14[VMAX-1:0] & \leftarrow 0 \\
YMM15[VMAX-1:0] & \leftarrow 0
\end{align*}
\]

ELSE

\[
\begin{align*}
YMM0[VMAX-1:0] & \leftarrow 0 \\
YMM1[VMAX-1:0] & \leftarrow 0 \\
YMM2[VMAX-1:0] & \leftarrow 0
\end{align*}
\]
INSTRUCTION SET REFERENCE, M-Z

\[
\begin{align*}
YMM3[\text{VLMAX}-1:0] & \leftarrow 0 \\
YMM4[\text{VLMAX}-1:0] & \leftarrow 0 \\
YMM5[\text{VLMAX}-1:0] & \leftarrow 0 \\
YMM6[\text{VLMAX}-1:0] & \leftarrow 0 \\
YMM7[\text{VLMAX}-1:0] & \leftarrow 0 \\
YMM8-15: & \text{Unmodified}
\end{align*}
\]

FI

Intel C/C++ Compiler Intrinsic Equivalent

VZEROALL: \_mm256\_zeroall()

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 8.
VZEROUPPER—Zero Upper Bits of YMM Registers

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VEX.128.0F.WIG 77 VZEROUPPER</td>
<td>NP</td>
<td>V/V</td>
<td>AVX</td>
<td>Zero upper 128 bits of all YMM registers.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description
The instruction zeros the bits in position 128 and higher of all YMM registers. The lower 128-bits of the registers (the corresponding XMM registers) are unmodified.
This instruction is recommended when transitioning between AVX and legacy SSE code - it will eliminate performance penalties caused by false dependencies.
Note: VEX.vvvv is reserved and must be 1111b otherwise instructions will #UD. In Compatibility and legacy 32-bit mode only the lower 8 registers are modified.

Operation

VZEROUPPER
IF (64-bit mode)
  YMM0[VLMAX-1:128] ← 0
  YMM1[VLMAX-1:128] ← 0
  YMM2[VLMAX-1:128] ← 0
  YMM3[VLMAX-1:128] ← 0
  YMM4[VLMAX-1:128] ← 0
  YMM5[VLMAX-1:128] ← 0
  YMM6[VLMAX-1:128] ← 0
  YMM7[VLMAX-1:128] ← 0
  YMM8[VLMAX-1:128] ← 0
  YMM9[VLMAX-1:128] ← 0
  YMM10[VLMAX-1:128] ← 0
  YMM11[VLMAX-1:128] ← 0
  YMM12[VLMAX-1:128] ← 0
  YMM13[VLMAX-1:128] ← 0
  YMM14[VLMAX-1:128] ← 0
  YMM15[VLMAX-1:128] ← 0
ELSE
INSTRUCTION SET REFERENCE, M-Z

YMM0[VLMAX-1:128] ← 0
YMM1[VLMAX-1:128] ← 0
YMM2[VLMAX-1:128] ← 0
YMM3[VLMAX-1:128] ← 0
YMM4[VLMAX-1:128] ← 0
YMM5[VLMAX-1:128] ← 0
YMM6[VLMAX-1:128] ← 0
YMM7[VLMAX-1:128] ← 0
YMM8-15: unmodified

FI

Intel C/C++ Compiler Intrinsic Equivalent

VZEROUPPER: _mm256_zeroupper()

SIMD Floating-Point Exceptions

None.

Other Exceptions

See Exceptions Type 8.
**WAIT/FWAIT—Wait**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B</td>
<td>WAIT</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Check pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>9B</td>
<td>FWAIT</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Check pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Causes the processor to check for and handle pending, unmasked, floating-point exceptions before proceeding. (FWAIT is an alternate mnemonic for WAIT.)

This instruction is useful for synchronizing exceptions in critical sections of code. Coding a WAIT instruction after a floating-point instruction ensures that any unmasked floating-point exceptions the instruction may raise are handled before the processor can modify the instruction’s results. See the section titled “Floating-Point Exception Synchronization” in Chapter 8 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1*, for more information on using the WAIT/FWAIT instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**Operation**

`CheckForPendingUnmaskedFloatingPointExceptions;`

**FPU Flags Affected**

The C0, C1, C2, and C3 flags are undefined.

**Floating-Point Exceptions**

None.

**Protected Mode Exceptions**

- **#NM** If CR0.MP[bit 1] = 1 and CR0.TS[bit 3] = 1.
- **#UD** If the LOCK prefix is used.
INSTRUCTION SET REFERENCE, M-Z

**Real-Address Mode Exceptions**
Same exceptions as in protected mode.

**Virtual-8086 Mode Exceptions**
Same exceptions as in protected mode.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
Same exceptions as in protected mode.
**WBINVD—Write Back and Invalidate Cache**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 09</td>
<td>WBINVD</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Write back and flush internal caches; initiate writing-back and flushing of external caches.</td>
</tr>
</tbody>
</table>

### Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Writes back all modified cache lines in the processor’s internal cache to main memory and invalidates (flushes) the internal caches. The instruction then issues a special-function bus cycle that directs external caches to also write back modified data and another bus cycle to indicate that the external caches should be invalidated.

After executing this instruction, the processor does not wait for the external caches to complete their write-back and flushing operations before proceeding with instruction execution. It is the responsibility of hardware to respond to the cache write-back and flush signals. The amount of time or cycles for WBINVD to complete will vary due to size and other factors of different cache hierarchies. As a consequence, the use of the WBINVD instruction can have an impact on logical processor interrupt/event response time.

The WBINVD instruction is a privileged instruction. When the processor is running in protected mode, the CPL of a program or procedure must be 0 to execute this instruction. This instruction is also a serializing instruction (see “Serializing Instructions” in Chapter 10 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*).

In situations where cache coherency with main memory is not a concern, software can use the INVD instruction.

This instruction’s operation is the same in non-64-bit modes and 64-bit mode.

**IA-32 Architecture Compatibility**

The WBINVD instruction is implementation dependent, and its function may be implemented differently on future Intel 64 and IA-32 processors. The instruction is not supported on IA-32 processors earlier than the Intel486 processor.

**Operation**

WriteBack(InternalCaches);
Flush(InternalCaches);
SignalWriteBack(ExternalCaches);
SignalFlush(ExternalCaches);
Continue; (* Continue execution *)

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If the current privilege level is not 0.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) WBINVD cannot be executed at the virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
WRFSBASE/WRGSBASE—Write FS/GS Segment Base

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32-bit Mode</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F AE /2 WRFSBASE r32</td>
<td>M</td>
<td>V/I</td>
<td>FSGSBASE</td>
<td>Load the FS base address with the 32-bit value in the source register.</td>
</tr>
<tr>
<td>REX.W + F3 0F AE /2 WRFSBASE r64</td>
<td>M</td>
<td>V/I</td>
<td>FSGSBASE</td>
<td>Load the FS base address with the 64-bit value in the source register.</td>
</tr>
<tr>
<td>F3 0F AE /3 WRGSBASE r32</td>
<td>M</td>
<td>V/I</td>
<td>FSGSBASE</td>
<td>Load the GS base address with the 32-bit value in the source register.</td>
</tr>
<tr>
<td>REX.W + F3 0F AE /3 WRGSBASE r64</td>
<td>M</td>
<td>V/I</td>
<td>FSGSBASE</td>
<td>Load the GS base address with the 64-bit value in the source register.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Loads the FS or GS segment base address with the general-purpose register indicated by the modR/M:r/m field.

The source operand may be either a 32-bit or a 64-bit general-purpose register. The REX.W prefix indicates the operand size is 64 bits. If no REX.W prefix is used, the operand size is 32 bits; the upper 32 bits of the source register are ignored and upper 32 bits of the base address (for FS or GS) are cleared.

This instruction is supported only in 64-bit mode.

Operation

FS/GS segment base address ← SRC;

Flags Affected

None

C/C++ Compiler Intrinsic Equivalent

WRFSBASE: void _writefsbase_u32( unsigned int );
WRFSBASE: \_writefsbase\_u64( unsigned \_int64 );
WRGSBASE: void \_writegsbase\_u32( unsigned int );
WRGSBASE: \_writegsbase\_u64( unsigned \_int64 );

**Protected Mode Exceptions**

#UD The WRFSBASE and WRGSBASE instructions are not recognized in protected mode.

**Real-Address Mode Exceptions**

#UD The WRFSBASE and WRGSBASE instructions are not recognized in real-address mode.

**Virtual-8086 Mode Exceptions**

#UD The WRFSBASE and WRGSBASE instructions are not recognized in virtual-8086 mode.

**Compatibility Mode Exceptions**

#UD The WRFSBASE and WRGSBASE instructions are not recognized in compatibility mode.

**64-Bit Mode Exceptions**

#UD If the LOCK prefix is used.
If CR4.FSGSBASE[bit 16] = 0.
If CPUID.07H.0H:EBX.FSGSBASE[bit 0] = 0
#GP(0) If the source register contains a non-canonical address.
WRMSR—Write to Model Specific Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/ Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 30</td>
<td>WRMSR</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Write the value in EDX:EAX to MSR specified by ECX.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Writes the contents of registers EDX:EAX into the 64-bit model specific register (MSR) specified in the ECX register. (On processors that support the Intel 64 architecture, the high-order 32 bits of RCX are ignored.) The contents of the EDX register are copied to high-order 32 bits of the selected MSR and the contents of the EAX register are copied to low-order 32 bits of the MSR. (On processors that support the Intel 64 architecture, the high-order 32 bits of each of RAX and RDX are ignored.) Undefined or reserved bits in an MSR should be set to values previously read.

This instruction must be executed at privilege level 0 or in real-address mode; otherwise, a general protection exception #GP(0) is generated. Specifying a reserved or unimplemented MSR address in ECX will also cause a general protection exception. The processor will also generate a general protection exception if software attempts to write to bits in a reserved MSR.

When the WRMSR instruction is used to write to an MTRR, the TLBs are invalidated. This includes global entries (see “Translation Lookaside Buffers (TLBs)” in Chapter 3 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A).

MSRs control functions for testability, execution tracing, performance-monitoring and machine check errors. Chapter 34, “Model-Specific Registers (MSRs)”, in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C, lists all MSRs that can be read with this instruction and their addresses. Note that each processor family has its own set of MSRs.

The WRMSR instruction is a serializing instruction (see "Serializing Instructions" in Chapter 8 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A). Note that WRMSR to the IA32_TSC_DEADLINE MSR (MSR index 6E0H) and the X2APIC MSRs (MSR indices 802H to 83FH) are not serializing.

The CPUID instruction should be used to determine whether MSRs are supported (CPUID.01H:EDX[5] = 1) before using this instruction.
IA-32 Architecture Compatibility

The MSRs and the ability to read them with the WRMSR instruction were introduced into the IA-32 architecture with the Pentium processor. Execution of this instruction by an IA-32 processor earlier than the Pentium processor results in an invalid opcode exception #UD.

Operation

MSR[ECX] ← EDX:EAX;

Flags Affected

None.

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0.
If the value in ECX specifies a reserved or unimplemented MSR address.
If the value in EDX:EAX sets bits that are reserved in the MSR specified by ECX.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions

#GP If the value in ECX specifies a reserved or unimplemented MSR address.
If the value in EDX:EAX sets bits that are reserved in the MSR specified by ECX.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions

#GP(0) The WRMSR instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions

Same exceptions as in protected mode.

64-Bit Mode Exceptions

Same exceptions as in protected mode.
**XADD—Exchange and Add**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF C0 /r</td>
<td>XADD r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange r8 and r/m8; load sum into r/m8.</td>
</tr>
<tr>
<td>REX + OF C0 /r</td>
<td>XADD r/m8*, r8*</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Exchange r8 and r/m8; load sum into r/m8.</td>
</tr>
<tr>
<td>OF C1 /r</td>
<td>XADD r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange r16 and r/m16; load sum into r/m16.</td>
</tr>
<tr>
<td>OF C1 /r</td>
<td>XADD r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange r32 and r/m32; load sum into r/m32.</td>
</tr>
<tr>
<td>REX,W + OF C1 /r</td>
<td>XADD r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Exchange r64 and r/m64; load sum into r/m64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
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<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR</td>
<td>ModRM:r/m (r, w)</td>
<td>ModRMreg (w)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Exchanges the first operand (destination operand) with the second operand (source operand), then loads the sum of the two values into the destination operand. The destination operand can be a register or a memory location; the source operand is a register.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

**IA-32 Architecture Compatibility**

IA-32 processors earlier than the Intel486 processor do not recognize this instruction. If this instruction is used, you should provide an equivalent code sequence that runs on earlier processors.
Operation

TEMP ← SRC + DEST;
SRC ← DEST;
DEST ← TEMP;

Flags Affected
The CF, PF, AF, SF, ZF, and OF flags are set according to the result of the addition, which is stored in the destination operand.

Protected Mode Exceptions

#GP(0) If the destination is located in a non-writable segment.
      If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
      If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
XADD—Exchange and Add

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Compatibility Mode Exceptions**
Same exceptions as in protected mode.

**64-Bit Mode Exceptions**
- #SS(0) If a memory address referencing the SS segment is in a non-canonical form.
- #GP(0) If the memory address is in a non-canonical form.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
- #UD If the LOCK prefix is used but the destination is not a memory operand.
### XCHG—Exchange Register/Memory with Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>90+rw</td>
<td>XCHG AX, r16</td>
<td>O</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange r16 with AX.</td>
</tr>
<tr>
<td>90+rw</td>
<td>XCHG r16, AX</td>
<td>O</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange AX with r16.</td>
</tr>
<tr>
<td>90+rd</td>
<td>XCHG EAX, r32</td>
<td>O</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange r32 with EAX.</td>
</tr>
<tr>
<td>REX.w + 90+rd</td>
<td>XCHG RAX, r64</td>
<td>O</td>
<td>Valid</td>
<td>N.E.</td>
<td>Exchange r64 with RAX.</td>
</tr>
<tr>
<td>90+rd</td>
<td>XCHG r32, EAX</td>
<td>O</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange EAX with r32.</td>
</tr>
<tr>
<td>REX.w + 90+rd</td>
<td>XCHG R64, RAX</td>
<td>O</td>
<td>Valid</td>
<td>N.E.</td>
<td>Exchange RAX with r64.</td>
</tr>
<tr>
<td>86 /r</td>
<td>XCHG r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange r8 (byte register) with byte from r/m8.</td>
</tr>
<tr>
<td>REX + 86 /r</td>
<td>XCHG r/m8*, r8*</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Exchange r8 (byte register) with byte from r/m8.</td>
</tr>
<tr>
<td>86 /r</td>
<td>XCHG r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange byte from r/m8 with r8 (byte register).</td>
</tr>
<tr>
<td>REX + 86 /r</td>
<td>XCHG r8*, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Exchange byte from r/m8 with r8 (byte register).</td>
</tr>
<tr>
<td>87 /r</td>
<td>XCHG r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange r16 with word from r/m16.</td>
</tr>
<tr>
<td>87 /r</td>
<td>XCHG r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange word from r/m16 with r16.</td>
</tr>
<tr>
<td>87 /r</td>
<td>XCHG r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange r32 with doubleword from r/m32.</td>
</tr>
<tr>
<td>REX.w + 87 /r</td>
<td>XCHG r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>Exchange r64 with quadword from r/m64.</td>
</tr>
<tr>
<td>87 /r</td>
<td>XCHG r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>Exchange doubleword from r/m32 with r32.</td>
</tr>
<tr>
<td>REX.w + 87 /r</td>
<td>XCHG R64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>Exchange quadword from r/m64 with r64.</td>
</tr>
</tbody>
</table>

**NOTES:**

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
**XCHG—Exchange Register/Memory with Register**

**Description**

Exchanges the contents of the destination (first) and source (second) operands. The operands can be two general-purpose registers or a register and a memory location. If a memory operand is referenced, the processor’s locking protocol is automatically implemented for the duration of the exchange operation, regardless of the presence or absence of the LOCK prefix or of the value of the IOPL. (See the LOCK prefix description in this chapter for more information on the locking protocol.)

This instruction is useful for implementing semaphores or similar data structures for process synchronization. (See “Bus Locking” in Chapter 8 of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*, for more information on bus locking.)

The XCHG instruction can also be used instead of the BSWAP instruction for 16-bit operands.

In 64-bit mode, the instruction’s default operation size is 32 bits. Using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

\[
\text{TEMP} \leftarrow \text{DEST}; \\
\text{DEST} \leftarrow \text{SRC}; \\
\text{SRC} \leftarrow \text{TEMP};
\]

**Flags Affected**

None.

**Protected Mode Exceptions**

#GP(0) If either operand is in a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a NULL segment selector.

---

**Instruction Operand Encoding**

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<tr>
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<th>Operand 2</th>
<th>Operand 3</th>
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</tr>
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<tbody>
<tr>
<td>0</td>
<td>AX/EAX/RAX (r, w)</td>
<td>opcode + rd (r, w)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>0</td>
<td>opcode + rd (r, w)</td>
<td>AX/EAX/RAX (r, w)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (r, w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RM</td>
<td>ModRM:reg (w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

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INSTRUCTION SET REFERENCE, M-Z

#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used but the destination is not a memory operand.

Real-Address Mode Exceptions
#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
#UD  If the LOCK prefix is used but the destination is not a memory operand.

Virtual-8086 Mode Exceptions
#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
#UD  If the LOCK prefix is used but the destination is not a memory operand.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0)  If a memory address referencing the SS segment is in a non-canonical form.
#GP(0)  If the memory address is in a non-canonical form.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD  If the LOCK prefix is used but the destination is not a memory operand.
XGETBV—Get Value of Extended Control Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 D0</td>
<td>XGETBV</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Reads an XCR specified by ECX into EDX:EAX.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Reads the contents of the extended control register (XCR) specified in the ECX register into registers EDX:EAX. (On processors that support the Intel 64 architecture, the high-order 32 bits of RCX are ignored.) The EDX register is loaded with the high-order 32 bits of the XCR and the EAX register is loaded with the low-order 32 bits. (On processors that support the Intel 64 architecture, the high-order 32 bits of each of RAX and RDX are cleared.) If fewer than 64 bits are implemented in the XCR being read, the values returned to EDX:EAX in unimplemented bit locations are undefined.

Specifying a reserved or unimplemented XCR in ECX causes a general protection exception.

Currently, only XCR0 (the XFEATURE_ENABLED_MASK register) is supported. Thus, all other values of ECX are reserved and will cause a #GP(0).

Operation

EDX:EAX ← XCR[ECX];

Flags Affected

None.

Protected Mode Exceptions

<table>
<thead>
<tr>
<th>Exception Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP(0)</td>
<td>If an invalid XCR is specified in ECX.</td>
</tr>
<tr>
<td>#UD</td>
<td>If CPUID.01H:ECX.XSAVE[bit 26] = 0.</td>
</tr>
<tr>
<td></td>
<td>If CR4.OSXSAVE[bit 18] = 0.</td>
</tr>
<tr>
<td></td>
<td>If the LOCK prefix is used.</td>
</tr>
<tr>
<td></td>
<td>If 66H, F3H or F2H prefix is used.</td>
</tr>
</tbody>
</table>
Real-Address Mode Exceptions
#GP   If an invalid XCR is specified in ECX.
#UD   If CPUID.01H:ECX.XSAVE[bit 26] = 0.
      If CR4.OSXSAVE[bit 18] = 0.
      If the LOCK prefix is used.
      If 66H, F3H or F2H prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
**XLAT/XLATB—Table Look-up Translation**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td>XLAT m8</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Set AL to memory byte DS:([E]BX + unsigned AL).</td>
</tr>
<tr>
<td>D7</td>
<td>XLATB</td>
<td>NP</td>
<td>Valid</td>
<td>Valid</td>
<td>Set AL to memory byte DS:([E]BX + unsigned AL).</td>
</tr>
<tr>
<td>REX.W + D7</td>
<td>XLATB</td>
<td>NP</td>
<td>Valid</td>
<td>N.E.</td>
<td>Set AL to memory byte [RBX + unsigned AL].</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Locates a byte entry in a table in memory, using the contents of the AL register as a table index, then copies the contents of the table entry back into the AL register. The index in the AL register is treated as an unsigned integer. The XLAT and XLATB instructions get the base address of the table in memory from either the DS:EBX or the DS:BX registers (depending on the address-size attribute of the instruction, 32 or 16, respectively). (The DS segment may be overridden with a segment override prefix.)

At the assembly-code level, two forms of this instruction are allowed: the “explicit-operand” form and the “no-operand” form. The explicit-operand form (specified with the XLAT mnemonic) allows the base address of the table to be specified explicitly with a symbol. This explicit-operands form is provided to allow documentation; however, note that the documentation provided by this form can be misleading. That is, the symbol does not have to specify the correct base address. The base address is always specified by the DS:(E)BX registers, which must be loaded correctly before the XLAT instruction is executed.

The no-operators form (XLATB) provides a “short form” of the XLAT instructions. Here also the processor assumes that the DS:(E)BX registers contain the base address of the table.

In 64-bit mode, operation is similar to that in legacy or compatibility mode. AL is used to specify the table index (the operand size is fixed at 8 bits). RBX, however, is used to specify the table’s base address. See the summary chart at the beginning of this section for encoding data and limits.

**Operation**

IF AddressSize = 16
THEN
    AL ← (DS:BX + ZeroExtend(AL));
ELSE IF (AddressSize = 32)
    AL ← (DS:EBX + ZeroExtend(AL)); FI;
ELSE (AddressSize = 64)
    AL ← (RBX + ZeroExtend(AL));
FI;

Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a NULL segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If the LOCK prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.

Compatibility Mode Exceptions
Same exceptions as in protected mode.
64-Bit Mode Exceptions

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
#GP(0) If the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs.
#UD If the LOCK prefix is used.
## XOR—Logical Exclusive OR

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>34 ib</td>
<td>XOR AL, imm8</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>AL XOR imm8.</td>
</tr>
<tr>
<td>35 iw</td>
<td>XOR AX, imm16</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>AX XOR imm16.</td>
</tr>
<tr>
<td>35 id</td>
<td>XOR EAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>Valid</td>
<td>EAX XOR imm32.</td>
</tr>
<tr>
<td>REX.w + 35 id</td>
<td>XOR RAX, imm32</td>
<td>I</td>
<td>Valid</td>
<td>N.E.</td>
<td>RAX XOR imm32 (sign-extended).</td>
</tr>
<tr>
<td>80 /6 ib</td>
<td>XOR r/m8, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m8 XOR imm8.</td>
</tr>
<tr>
<td>REX + 80 /6 ib</td>
<td>XOR r/m8*, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m8 XOR imm8.</td>
</tr>
<tr>
<td>81 /6 iw</td>
<td>XOR r/m16, imm16</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 XOR imm16.</td>
</tr>
<tr>
<td>81 /6 id</td>
<td>XOR r/m32, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 XOR imm32.</td>
</tr>
<tr>
<td>REX.w + 81 /6 id</td>
<td>XOR r/m64, imm32</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 XOR imm32 (sign-extended).</td>
</tr>
<tr>
<td>83 /6 ib</td>
<td>XOR r/m16, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 XOR imm8 (sign-extended).</td>
</tr>
<tr>
<td>83 /6 ib</td>
<td>XOR r/m32, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 XOR imm8 (sign-extended).</td>
</tr>
<tr>
<td>REX.w + 83 /6 ib</td>
<td>XOR r/m64, imm8</td>
<td>MI</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 XOR imm8 (sign-extended).</td>
</tr>
<tr>
<td>30 /r</td>
<td>XOR r/m8, r8</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m8 XOR r8.</td>
</tr>
<tr>
<td>REX + 30 /r</td>
<td>XOR r/m8*, r8*</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m8 XOR r8.</td>
</tr>
<tr>
<td>31 /r</td>
<td>XOR r/m16, r16</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m16 XOR r16.</td>
</tr>
<tr>
<td>31 /r</td>
<td>XOR r/m32, r32</td>
<td>MR</td>
<td>Valid</td>
<td>Valid</td>
<td>r/m32 XOR r32.</td>
</tr>
<tr>
<td>REX.w + 31 /r</td>
<td>XOR r/m64, r64</td>
<td>MR</td>
<td>Valid</td>
<td>N.E.</td>
<td>r/m64 XOR r64.</td>
</tr>
<tr>
<td>32 /r</td>
<td>XOR r8, r/m8</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>r8 XOR r/m8.</td>
</tr>
<tr>
<td>REX + 32 /r</td>
<td>XOR r8*, r/m8*</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>r8 XOR r/m8.</td>
</tr>
<tr>
<td>33 /r</td>
<td>XOR r16, r/m16</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>r16 XOR r/m16.</td>
</tr>
<tr>
<td>33 /r</td>
<td>XOR r32, r/m32</td>
<td>RM</td>
<td>Valid</td>
<td>Valid</td>
<td>r32 XOR r/m32.</td>
</tr>
<tr>
<td>REX.w + 33 /r</td>
<td>XOR r64, r/m64</td>
<td>RM</td>
<td>Valid</td>
<td>N.E.</td>
<td>r64 XOR r/m64.</td>
</tr>
</tbody>
</table>

### NOTES:

* In 64-bit mode, r/m8 can not be encoded to access the following byte registers if a REX prefix is used: AH, BH, CH, DH.
XOR—Logical Exclusive OR

Description
Performs a bitwise exclusive OR (XOR) operation on the destination (first) and source (second) operands and stores the result in the destination operand location. The source operand can be an immediate, a register, or a memory location; the destination operand can be a register or a memory location. (However, two memory operands cannot be used in one instruction.) Each bit of the result is 1 if the corresponding bits of the operands are different; each bit is 0 if the corresponding bits are the same.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically.

In 64-bit mode, using a REX prefix in the form of REX.R permits access to additional registers (R8-R15). Using a REX prefix in the form of REX.W promotes operation to 64 bits. See the summary chart at the beginning of this section for encoding data and limits.

Operation
DEST ← DEST XOR SRC;

Flags Affected
The OF and CF flags are cleared; the SF, ZF, and PF flags are set according to the result. The state of the AF flag is undefined.

Protected Mode Exceptions
#GP(0) If the destination operand points to a non-writable segment. If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If the DS, ES, FS, or GS register contains a NULL segment selector.
#PF(fault-code) If a page fault occurs.

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>AL/AX/EAX/RAX</td>
<td>imm8/16/32</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MI</td>
<td>ModRM:r/m (r, w)</td>
<td>imm8/16/32</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>MR</td>
<td>ModRM:r/m (r, w)</td>
<td>ModRM:reg (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Real-Address Mode Exceptions**

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Virtual-8086 Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

#UD If the LOCK prefix is used but the destination is not a memory operand.

**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#GP(0) If the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

#UD If the LOCK prefix is used but the destination is not a memory operand.
XORPD—Bitwise Logical XOR for Double-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 57 /r</td>
<td>RM</td>
<td>V/V</td>
<td>SSE2</td>
<td>Bitwise exclusive-OR of xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>VXORPD xmm1,xmm2,m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.128.66.0F.WIG 57 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical XOR of packed double-precision floating-point values in xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VXORPD xmm1,xmm2,xmm3/m128</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VEX.NDS.256.66.0F.WIG 57 /r</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical XOR of packed double-precision floating-point values in ymm2 and ymm3/mem.</td>
</tr>
<tr>
<td>VXORPD ymm1, ymm2, ymm3/m256</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRMreg (r, w)</td>
<td>ModRMrm/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRMreg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRMrm/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical exclusive-OR of the two packed double-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the result in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VLMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VLMAX-1:128) of the corresponding YMM register destination are zeroed.
VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.

**Operation**

**XORPD (128-bit Legacy SSE version)**

- DEST[63:0] ← DEST[63:0] BITWISE XOR SRC[63:0]
- DEST[VLMAX-1:128] (Unmodified)

**VXORPD (VEX.128 encoded version)**

- DEST[63:0] ← SRC1[63:0] BITWISE XOR SRC2[63:0]
- DEST[127:64] ← SRC1[127:64] BITWISE XOR SRC2[127:64]
- DEST[VLMAX-1:128] ← 0

**VXORPD (VEX.256 encoded version)**

- DEST[63:0] ← SRC1[63:0] BITWISE XOR SRC2[63:0]
- DEST[127:64] ← SRC1[127:64] BITWISE XOR SRC2[127:64]

**Intel C/C++ Compiler Intrinsic Equivalent**

- XORPD: `__m128d _mm_xor_pd(__m128d a, __m128d b)`
- VXORPD: `__m256d _mm256_xor_pd (__m256d a, __m256d b)`

**SIMD Floating-Point Exceptions**

None.

**Other Exceptions**

See Exceptions Type 4.
XORPS—Bitwise Logical XOR for Single-Precision Floating-Point Values

<table>
<thead>
<tr>
<th>Opcode/Instruction</th>
<th>Op/En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 57 /r XORPS xmm1, xmm2/m128</td>
<td>RM</td>
<td>V/V</td>
<td>SSE</td>
<td>Bitwise exclusive-OR of xmm2/m128 and xmm1.</td>
</tr>
<tr>
<td>VEX.NDS.128.0F.WIG 57 /r VXORPS xmm1,xmm2, xmm3/m128</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical XOR of packed single-precision floating-point values in xmm2 and xmm3/mem.</td>
</tr>
<tr>
<td>VEX.NDS.256.0F.WIG 57 /r VXORPS ymm1, ymm2, ymm3/m256</td>
<td>RVM</td>
<td>V/V</td>
<td>AVX</td>
<td>Return the bitwise logical XOR of packed single-precision floating-point values in ymm2 and ymm3/mem.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM</td>
<td>ModRM:reg (r, w)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>RVM</td>
<td>ModRM:reg (w)</td>
<td>VEX.vvvv (r)</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

Performs a bitwise logical exclusive-OR of the four packed single-precision floating-point values from the source operand (second operand) and the destination operand (first operand), and stores the result in the destination operand. The source operand can be an XMM register or a 128-bit memory location. The destination operand is an XMM register.

In 64-bit mode, using a REX prefix in the form of REX.R permits this instruction to access additional registers (XMM8-XMM15).

128-bit Legacy SSE version: The second source can be an XMM register or an 128-bit memory location. The destination is not distinct from the first source XMM register and the upper bits (VMAX-1:128) of the corresponding YMM register destination are unmodified.

VEX.128 encoded version: the first source operand is an XMM register or 128-bit memory location. The destination operand is an XMM register. The upper bits (VMAX-1:128) of the corresponding YMM register destination are zeroed.

VEX.256 encoded version: The first source operand is a YMM register. The second source operand can be a YMM register or a 256-bit memory location. The destination operand is a YMM register.
INSTRUCTION SET REFERENCE, M-Z

Operation

**XORPS (128-bit Legacy SSE version)**
DEST[31:0] ← SRC1[31:0] BITWISE XOR SRC2[31:0]
DEST[95:64] ← SRC1[95:64] BITWISE XOR SRC2[95:64]
DEST[VLMAX-1:128] (Unmodified)

**VXORPS (VEX.128 encoded version)**
DEST[31:0] ← SRC1[31:0] BITWISE XOR SRC2[31:0]
DEST[95:64] ← SRC1[95:64] BITWISE XOR SRC2[95:64]
DEST[VLMAX-1:128] ← 0

**VXORPS (VEX.256 encoded version)**
DEST[31:0] ← SRC1[31:0] BITWISE XOR SRC2[31:0]
DEST[95:64] ← SRC1[95:64] BITWISE XOR SRC2[95:64]

Intel C/C++ Compiler Intrinsic Equivalent
XORPS: __m128 _mm_xor_ps(__m128 a, __m128 b)
VXORPS: __m256 _mm256_xor_ps (__m256 a, __m256 b);

SIMD Floating-Point Exceptions
None.

Other Exceptions
See Exceptions Type 4.
**XRSTOR—Restore Processor Extended States**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Compat/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /5</td>
<td>XRSTOR mem</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Restore processor extended states from memory. The states are specified by EDX:EAX</td>
</tr>
<tr>
<td>REX.W+ 0F AE /5</td>
<td>XRSTOR64 mem</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Restore processor extended states from memory. The states are specified by EDX:EAX</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m (r)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a full or partial restore of the enabled processor states using the state information stored in the memory address specified by the source operand. The implicit EDX:EAX register pair specifies a 64-bit restore mask.

The format of the XSAVE/XRSTOR area is shown in Table 4-22. The memory layout of the XSAVE/XRSTOR area may have holes between save areas written by the processor as a result of the processor not supporting certain processor extended states or system software not supporting certain processor extended states. There is no relationship between the order of XCR0 bits and the order of the state layout. States corresponding to higher and lower XCR0 bits may be intermingled in the layout.
XRSTOR operates on each subset of the processor state or a processor extended state in one of three ways (depending on the corresponding bit in XCR0 (XFEATURE_ENABLED_MASK register), the restore mask EDX:EAX, and the save mask XSAVE.HEADER.XSTATE_BV in memory):

- Updates the processor state component using the state information stored in the respective save area (see Table 4-22) of the source operand, if the corresponding bit in XCR0, EDX:EAX, and XSAVE.HEADER.XSTATE_BV are all 1.
- Writes certain registers in the processor state component using processor-supplied values (see Table 4-24) without using state information stored in respective save area of the memory region, if the corresponding bit in XCR0 and EDX:EAX are both 1, but the corresponding bit in XSAVE.HEADER.XSTATE_BV is 0.
- The processor state component is unchanged, if the corresponding bit in XCR0 or EDX:EAX is 0.

The format of the header section (XSAVE.HEADER) of the XSAVE/XRSTOR area is shown in Table 4-23.
XRSTOR—Restore Processor Extended States

Table 4-23. XSAVE.HEADER Layout

<table>
<thead>
<tr>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
<th>Byte Offset from Header</th>
<th>Byte Offset from XSAVE/XRSTOR Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rsvd (Must be 0)</td>
<td>XSTATE_BV</td>
<td>0</td>
<td>512</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>Rsvd (Must be 0)</td>
<td>16</td>
<td>528</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>Reserved</td>
<td>32</td>
<td>544</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>Reserved</td>
<td>48</td>
<td>560</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

If a processor state component is not enabled in XCR0 but the corresponding save mask bit in XSAVE.HEADER.XSTATE_BV is 1, an attempt to execute XRSTOR will cause a #GP(0) exception. Software may specify all 1’s in the implicit restore mask EDX:EAX, so that all the enabled processors states in XCR0 are restored from state information stored in memory or from processor supplied values. When using all 1’s as the restore mask, software is required to determine the total size of the XSAVE/XRSTOR save area (specified as source operand) to fit all enabled processor states by using the value enumerated in CPUID.(EAX=0D, ECX=0):EBX. While it’s legal to set any bit in the EDX:EAX mask to 1, it is strongly recommended to set only the bits that are required to save/restore specific states.

An attempt to restore processor states with writing 1s to reserved bits in certain registers (see Table 4-25) will cause a #GP(0) exception.

Because bit 63 of XCR0 is reserved for future bit vector expansion, it will not be used for any future processor state feature, and XRSTOR will ignore bit 63 of EDX:EAX (EDX[31]).

Table 4-24. Processor Supplied Init Values XRSTOR May Use

<table>
<thead>
<tr>
<th>Processor State Component</th>
<th>Processor Supplied Register Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>x87 FPU State</td>
<td>FCW ← 037FH; FTW ← 0FFFFH; FSW ← 0H; FPU CS ← 0H; FPU DS ← 0H; FPU IP ← 0H; FPU DP ← 0; ST0-ST7 ← 0;</td>
</tr>
<tr>
<td>SSE State†</td>
<td>If 64-bit Mode: XMM0-XMM15 ← 0H; Else XMM0-XMM7 ← 0H</td>
</tr>
</tbody>
</table>

NOTES:
1. MXCSR state is not updated by processor supplied values. MXCSR state can only be updated by XRSTOR from state information stored in XSAVE/XRSTOR area.
A source operand not aligned to 64-byte boundary (for 64-bit and 32-bit modes) will result in a general-protection (#GP) exception. In 64-bit mode, the upper 32 bits of RDX and RAX are ignored.

**Operation**

/* The alignment of the x87 and SSE fields in the XSAVE area is the same as in FXSAVE area*/

\[
\begin{align*}
RS\_TMP\_MASK[62:0] & \leftarrow (EDX[30:0] \ll 32) \text{ OR } EAX[31:0]; \\
ST\_TMP\_MASK[62:0] & \leftarrow SRCMEM.HEADER.XSTATE\_BV[62:0]; \\
\text{IF } \left( (\left( XCR0[62:0] \text{ XOR } 7\text{FFFFFFF}_8\text{FFFFFFFH} \right) \text{ AND } ST\_TMP\_MASK[62:0] ) \right) & \text{ THEN} \\
& \text{ #GP(0)} \\
\text{ELSE } & \text{ FOR } i = 0, 62 \text{ STEP 1} \\
& \text{ IF } (\text{ RS\_TMP\_MASK}[i] \text{ and } XCR0[i] ) \\
& \text{ THEN} \\
& \text{ IF } (\text{ ST\_TMP\_MASK}[i] ) \\
& \text{ CASE } ( i ) \text{ OF} \\
& 0: \text{ Processor state}[x87\ FPU] \leftarrow SRCMEM.\text{FPUSSESave\_Area}[FPU]; \\
& 1: \text{ Processor state}[SSE] \leftarrow SRCMEM.\text{FPUSSESave\_Area}[SSE]; \\
& \text{ // MXCSR is loaded as part of the SSE state} \\
& \text{DEFAULT: // } i \text{ corresponds to a valid sub-leaf index of CPUID leaf ODH} \\
& \text{ Processor state}[i] \leftarrow SRCMEM.\text{Ext\_Save\_Area}[ i ]; \\
& \text{ESAC;} \\
\text{ELSE } & \\
& \text{ Processor extended state}[i] \leftarrow \text{ Processor supplied values; (see Table 4-24)} \\
& \text{CASE } ( i ) \text{ OF} \\
& 1: \text{ MXCSR } \leftarrow SRCMEM.\text{FPUSSESave\_Area}[SSE]; \\
& \text{ESAC; } \\
& \text{FI;} \\
& \text{FI;} \\
& \text{NEXT;} \\
& \text{FI;}
\end{align*}
\]

**Table 4-25. Reserved Bit Checking and XRSTOR**

<table>
<thead>
<tr>
<th>Processor State Component</th>
<th>Reserved Bit Checking</th>
</tr>
</thead>
<tbody>
<tr>
<td>X87 FPU State</td>
<td>None</td>
</tr>
<tr>
<td>SSE State</td>
<td>Reserved bits of MXCSR</td>
</tr>
</tbody>
</table>

A source operand not aligned to 64-byte boundary (for 64-bit and 32-bit modes) will result in a general-protection (#GP) exception. In 64-bit mode, the upper 32 bits of RDX and RAX are ignored.
Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If a memory operand is not aligned on a 64-byte boundary, regardless of segment.
If a bit in XCR0 is 0 and the corresponding bit in HEADER.XSTATE_BV field of the source operand is 1.
If bytes 23:8 of HEADER is not zero.
If attempting to write any reserved bits of the MXCSR register with 1.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#NM If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.XSAVE[bit 26] = 0.
If CR4.OSXSAVE[bit 18] = 0.
If the LOCK prefix is used.
If 66H, F3H or F2H prefix is used.
#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 64-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
If a bit in XCR0 is 0 and the corresponding bit in HEADER.XSTATE_BV field of the source operand is 1.
INSTRUCTION SET REFERENCE, M-Z

If bytes 23:8 of HEADER is not zero.
If attempting to write any reserved bits of the MXCSR register with 1.

#NM If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.XSAVE[bit 26] = 0.
If CR4.OSXSAVE[bit 18] = 0.
If the LOCK prefix is used.
If 66H, F3H or F2H prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in Protected Mode

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions

#GP(0) If the memory address is in a non-canonical form.
If a memory operand is not aligned on a 64-byte boundary, regardless of segment.
If a bit in XCR0 is 0 and the corresponding bit in XSAVE.HEADER.XSTATE_BV is 1.
If bytes 23:8 of HEADER is not zero.
If attempting to write any reserved bits of the MXCSR register with 1.

#SS(0) If a memory address referencing the SS segment is in a non-canonical form.

#PF(fault-code) If a page fault occurs.

#NM If CR0.TS[bit 3] = 1.

#UD If CPUID.01H:ECX.XSAVE[bit 26] = 0.
If CR4.OSXSAVE[bit 18] = 0.
If the LOCK prefix is used.
If 66H, F3H or F2H prefix is used.

#AC If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment
check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).
**XSAVE—Save Processor Extended States**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Op/En</th>
<th>64-Bit Mode</th>
<th>Comp/Leg Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OF AE /4</td>
<td>XSAVE mem</td>
<td>M</td>
<td>Valid</td>
<td>Valid</td>
<td>Save processor extended states to memory. The states are specified by EDX:EAX</td>
</tr>
<tr>
<td>REX.W+ OF AE /4</td>
<td>XSAVE64 mem</td>
<td>M</td>
<td>Valid</td>
<td>N.E.</td>
<td>Save processor extended states to memory. The states are specified by EDX:EAX</td>
</tr>
</tbody>
</table>

**Instruction Operand Encoding**

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

**Description**

Performs a full or partial save of the enabled processor state components to a memory address specified in the destination operand. A full or partial save of the processor states is specified by an implicit mask operand via the register pair, EDX:EAX. The destination operand is a memory location that must be 64-byte aligned.

The implicit 64-bit mask operand in EDX:EAX specifies the subset of enabled processor state components to save into the XSAVE/XRSTOR save area. The XSAVE/XRSTOR save area comprises of individual save area for each processor state components and a header section, see Table 4-22. Each component save area is written if both the corresponding bits in the save mask operand and in XCR0 (the XFEATURE_ENABLED_MASK register) are 1. A processor state component save area is not updated if either one of the corresponding bits in the mask operand or in XCR0 is 0. If the mask operand (EDX:EAX) contains all 1’s, all enabled processor state components in XCR0 are written to the respective component save area.

The bit assignment used for the EDX:EAX register pair matches XCR0 (see chapter 2 of Vol. 3B). For the XSAVE instruction, software can specify "1" in any bit position of EDX:EAX, irrespective of whether the corresponding bit position in XCR0 is valid for the processor. The bit vector in EDX:EAX is "anded" with XCR0 to determine which save area will be written. While it’s legal to set any bit in the EDX:EAX mask to 1, it is strongly recommended to set only the bits that are required to save/restore specific states. When specifying 1 in any bit position of EDX:EAX mask, software is required to determine the total size of the XSAVE/XRSTOR save area (specified as destination operand) to fit all enabled processor states by using the value enumerated in CPUID.(EAX=0D, ECX=0):EBX.
The content layout of the XSAVE/XRSTOR save area is architecturally defined to be extendable and enumerated via the sub-leaves of CPUID.0DH leaf. The extendable framework of the XSAVE/XRSTOR layout is depicted by Table 4-22. The layout of the XSAVE/XRSTOR save area is fixed and may contain non-contiguous individual save areas. The XSAVE/XRSTOR save area is not compacted if some features are not saved or are not supported by the processor and/or by system software.

The layout of the register fields of first 512 bytes of the XSAVE/XRSTOR is the same as the FXSAVE/FXRSTOR area (refer to “FXSAVE—Save x87 FPU, MMX Technology, and SSE State” on page 458). But XSAVE/XRSTOR organizes the 512 byte area as x87 FPU states (including FPU operation states, x87/MMX data registers), MXCSR (including MXCSR_MASK), and XMM registers.

Bytes 464:511 are available for software use. The processor does not write to bytes 464:511 when executing XSAVE.

The processor writes 1 or 0 to each HEADER.XSTATE_BV[i] bit field of an enabled processor state component in a manner that is consistent to XRSTOR’s interaction with HEADER.XSTATE_BV (see the operation section of XRSTOR instruction). If a processor implementation discern that a processor state component is in its initialized state (according to Table 4-24) it may modify the corresponding bit in the HEADER.XSTATE_BV as ‘0’.

A destination operand not aligned to 64-byte boundary (in either 64-bit or 32-bit modes) will result in a general-protection (#GP) exception being generated. In 64-bit mode, the upper 32 bits of RDX and RAX are ignored.

**Operation**

\[
\text{TMP\_MASK}[62:0] \leftarrow ((\text{EDX}[30:0] \ll 32) \text{ OR } \text{EAX}[31:0]) \text{ AND } \text{XCR0}[62:0];
\]

FOR \( i = 0, 62 \) STEP 1

IF ( \( \text{TMP\_MASK}[i] = 1 \) ) THEN

THEN

CASE (\( i \)) of

0: \( \text{DEST.FPUSSESAVE\_Area[x87 FPU]} \leftarrow \text{processor state[x87 FPU]}; \)

1: \( \text{DEST.FPUSSESAVE\_Area[SSE]} \leftarrow \text{processor state[SSE]}; \)

// SSE state include MXCSR

DEFAULT: // \( i \) corresponds to a valid sub-leaf index of CPUID leaf 0DH

\( \text{DEST.Ext\_Save\_Area[i]} \leftarrow \text{processor state[i]}; \)

ENDCASE:

\( \text{DEST.HEADER.XSTATE\_BV}[i] \leftarrow \text{INIT\_FUNCTION}[i]; \)

FI;

NEXT;

**Flags Affected**

None.
INSTRUCTION SET REFERENCE, M-Z

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
       If a memory operand is not aligned on a 64-byte boundary, regardless of segment.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#NM  If CR0.TS[bit 3] = 1.
#UD  If CPUID.01H:ECX.XSAVE[bit 26] = 0.
       If CR4.OSXSAVE[bit 18] = 0.
       If the LOCK prefix is used.
       If 66H, F3H or F2H prefix is used.
#AC  If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).

Real-Address Mode Exceptions

#GP  If a memory operand is not aligned on a 64-byte boundary, regardless of segment.
       If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM  If CR0.TS[bit 3] = 1.
#UD  If CPUID.01H:ECX.XSAVE[bit 26] = 0.
       If CR4.OSXSAVE[bit 18] = 0.
       If the LOCK prefix is used.
       If 66H, F3H or F2H prefix is used.

Virtual-8086 Mode Exceptions

Same exceptions as in protected mode.

XSAVE—Save Processor Extended States
**Compatibility Mode Exceptions**

Same exceptions as in protected mode.

**64-Bit Mode Exceptions**

- **#SS(0)**: If a memory address referencing the SS segment is in a non-canonical form.
- **#GP(0)**: If the memory address is in a non-canonical form.
- If a memory operand is not aligned on a 64-byte boundary, regardless of segment.
- **#PF(fault-code)**: If a page fault occurs.
- **#NM**: If CR0.TS[bit 3] = 1.
- **#UD**: If CPUID.01H:ECX.XSAVE[bit 26] = 0.
  - If CR4.OSXSAVE[bit 18] = 0.
  - If the LOCK prefix is used.
  - If 66H, F3H or F2H prefix is used.
- **#AC**: If this exception is disabled a general protection exception (#GP) is signaled if the memory operand is not aligned on a 16-byte boundary, as described above. If the alignment check exception (#AC) is enabled (and the CPL is 3), signaling of #AC is not guaranteed and may vary with implementation, as follows. In all implementations where #AC is not signaled, a general protection exception is signaled in its place. In addition, the width of the alignment check may also vary with implementation. For instance, for a given implementation, an alignment check exception might be signaled for a 2-byte misalignment, whereas a general protection exception might be signaled for all other misalignments (4-, 8-, or 16-byte misalignments).
XSAVEOPT—Save Processor Extended States Optimized

<table>
<thead>
<tr>
<th>Opcode/ Instruction</th>
<th>Op/ En</th>
<th>64/32 bit Mode Support</th>
<th>CPUID Feature Flag</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AE /6 XSAVEOPT</td>
<td>M</td>
<td>V/V</td>
<td>XSAVEOPT</td>
<td>Save processor extended states specified in EDX:EAX to memory, optimizing the state save operation if possible.</td>
</tr>
<tr>
<td>REX.w + 0F AE /6 XSAVEOPT64</td>
<td>M</td>
<td>V/V</td>
<td>XSAVEOPT</td>
<td>Save processor extended states specified in EDX:EAX to memory, optimizing the state save operation if possible.</td>
</tr>
</tbody>
</table>

Instruction Operand Encoding

<table>
<thead>
<tr>
<th>Op/En</th>
<th>Operand 1</th>
<th>Operand 2</th>
<th>Operand 3</th>
<th>Operand 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>ModRM:r/m(w)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Description

XSAVEOPT performs a full or partial save of the enabled processor state components to a memory address specified in the destination operand. A full or partial save of the processor states is specified by an implicit mask operand via the register pair, EDX:EAX. The destination operand is a memory location that must be 64-byte aligned. The hardware may optimize the manner in which data is saved. The performance of this instruction will be equal or better than using the XSAVE instruction.

The implicit 64-bit mask operand in EDX:EAX specifies the subset of enabled processor state components to save into the XSAVE/XRSTOR save area. The XSAVE/XRSTOR save area comprises of individual save area for each processor state components and a header section, see Table 4-22.

The bit assignment used for the EDX:EAX register pair matches XCR0 (the XFEATURE_ENABLED_MASK register). For the XSAVEOPT instruction, software can specify "1" in any bit position of EDX:EAX, irrespective of whether the corresponding bit position in XCR0 is valid for the processor. The bit vector in EDX:EAX is "anded" with XCR0 to determine which save area will be written. While it’s legal to set any bit in the EDX:EAX mask to 1, it is strongly recommended to set only the bits that are required to save/restore specific states. When specifying 1 in any bit position of EDX:EAX mask, software is required to determine the total size of the XSAVE/XRSTOR save area (specified as destination operand) to fit all enabled processor states by using the value enumerated in CPUID.(EAX=0D, ECX=0):EBX.

The content layout of the XSAVE/XRSTOR save area is architecturally defined to be extendable and enumerated via the sub-leaves of CPUID.0DH leaf. The extendable
framework of the XSAVE/XRSTOR layout is depicted by Table 4-22. The layout of the XSAVE/XRSTOR save area is fixed and may contain non-contiguous individual save areas. The XSAVE/XRSTOR save area is not compacted if some features are not saved or are not supported by the processor and/or by system software.

The layout of the register fields of first 512 bytes of the XSAVE/XRSTOR is the same as the FXSAVE/FXRSTOR area. But XSAVE/XRSTOR organizes the 512 byte area as x87 FPU states (including FPU operation states, x87/MMX data registers), MXCSR (including MXCSR_MASK), and XMM registers.

The processor writes 1 or 0 to each HEADER.XSTATE_BV[i] bit field of an enabled processor state component in a manner that is consistent to XRSTOR's interaction with HEADER.XSTATE_BV.

The state updated to the XSAVE/XRSTOR area may be optimized as follows:

- If the state is in its initialized form, the corresponding XSTATE_BV bit may be set to 0, and the corresponding processor state component that is indicated as initialized will not be saved to memory.

A processor state component save area is not updated if either one of the corresponding bits in the mask operand or in XCR0 is 0. The processor state component that is updated to the save area is computed by bit-wise AND of the mask operand (EDX:EAX) with XCR0.

HEADER.XSTATE_BV is updated to reflect the data that is actually written to the save area. A "1" bit in the header indicates the contents of the save area corresponding to that bit are valid. A "0" bit in the header indicates that the state corresponding to that bit is in its initialized form. The memory image corresponding to a "0" bit may or may not contain the correct (initialized) value since only the header bit (and not the save area contents) is updated when the header bit value is 0. XRSTOR will ensure the correct value is placed in the register state regardless of the value of the save area when the header bit is zero.

**XSAVEOPT Usage Guidelines**

When using the XSAVEOPT facility, software must be aware of the following guidelines:

1. The processor uses a tracking mechanism to determine which state components will be written to memory by the XSAVEOPT instruction. The mechanism includes three sub-conditions that are recorded internally each time XRSTOR is executed and evaluated on the invocation of the next XSAVEOPT. If a change is detected in any one of these sub-conditions, XSAVEOPT will behave exactly as XSAVE. The three sub-conditions are:
   - current CPL of the logical processor
   - indication whether or not the logical processor is in VMX non-root operation
   - linear address of the XSAVE/XRSTOR area
2. Upon allocation of a new XSAVE/XRSTOR area and before an XSAVE or XSAVEOPT instruction is used, the save area header (HEADER:XSTATE) must be initialized to zeroes for proper operation.

3. XSAVEOPT is designed primarily for use in context switch operations. The values stored by the XSAVEOPT instruction depend on the values previously stored in a given XSAVE area.

4. Manual modifications to the XSAVE area between an XRSTOR instruction and the matching XSAVEOPT may result in data corruption.

5. For optimization to be performed properly, the XRSTOR XSAVEOPT pair must use the same segment when referencing the XSAVE area and the base of that segment must be unchanged between the two operations.

6. Software should avoid executing XSAVEOPT into a buffer from which it hadn’t previously executed a XRSTOR. For newly allocated buffers, software can execute XRSTOR with the linear address of the buffer and a restore mask of EDX:EAX = 0. Executing XRSTOR(0:0) doesn’t restore any state, but ensures expected operation of the XSAVEOPT instruction.

7. The XSAVE area can be moved or even paged, but the contents at the linear address of the save area at an XSAVEOPT must be the same as that when the previous XRSTOR was performed.

A destination operand not aligned to 64-byte boundary (in either 64-bit or 32-bit modes) will result in a general-protection (#GP) exception being generated. In 64-bit mode, the upper 32 bits of RDX and RAX are ignored.

**Operation**

```plaintext
TMP_MASK[62:0] = (EDX[30:0] << 32) OR EAX[31:0] AND XCR0[62:0];
FOR i = 0, 62 STEP 1
    IF (TMP_MASK[i] = 1)
        THEN
            If not HW_CAN_OPTIMIZE_SAVE
                THEN
                    CASE ( i ) of
                        0: DEST.FPUSSESAVE_Area[x87 FPU]   processor state[x87 FPU];
                            // SSE state include MXCSR
                        1: DEST.FPUSSESAVE_Area[SSE]    processor state[SSE];
                        2: DEST.EXT_SAVE_Area2[YMM]   processor state[YMM];
                        DEFAULT: // i corresponds to a valid sub-leaf index of CPUID leaf 0DH
                            DEST.Ext_Save_Area[ i ]   processor state[i] ;
                    ESAC;
                FI;
            DEST.HEADER.XSTATE_BV[i] = INIT_FUNCTION[i];
        FI;
    NEXT;
```
Flags Affected
None.

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If a memory operand is not aligned on a 64-byte boundary, regardless of segment.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#NM If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.XSAVE[bit 26] = 0.
If CPUID.(EAX=0DH, ECX=01H):EAX.XSAVEOPT[bit 0] = 0.
If CR4.OSXSAVE[bit 18] = 0.
If the LOCK prefix is used.
If 66H, F3H or F2H prefix is used.

Real-Address Mode Exceptions
#GP If a memory operand is not aligned on a 64-byte boundary, regardless of segment.
If any part of the operand lies outside the effective address space from 0 to FFFFH.
#NM If CR0.TS[bit 3] = 1.
#UD If CPUID.01H:ECX.XSAVE[bit 26] = 0.
If CPUID.(EAX=0DH, ECX=01H):EAX.XSAVEOPT[bit 0] = 0.
If CR4.OSXSAVE[bit 18] = 0.
If the LOCK prefix is used.
If 66H, F3H or F2H prefix is used.

Virtual-8086 Mode Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
#SS(0) If a memory address referencing the SS segment is in a non-canonical form.
INSTRUCTION SET REFERENCE, M-Z

#GP(0) If the memory address is in a non-canonical form.
If a memory operand is not aligned on a 64-byte boundary, regardless of segment.

#PF(fault-code) If a page fault occurs.

#NM If CR0.TS[bit 3] = 1.

#UD If CPUID.01H:ECX.XSAVE[bit 26] = 0.
If CPUID.(EAX=0DH, ECX=01H):EAX.XSAVEOPT[bit 0] = 0.
If CR4.OSXSAVE[bit 18] = 0.
If the LOCK prefix is used.
If 66H, F3H or F2H prefix is used.
**XSETBV—Set Extended Control Register**

**Description**

Writes the contents of registers EDX:EAX into the 64-bit extended control register (XCR) specified in the ECX register. (On processors that support the Intel 64 architecture, the high-order 32 bits of RCX are ignored.) The contents of the EDX register are copied to high-order 32 bits of the selected XCR and the contents of the EAX register are copied to low-order 32 bits of the XCR. (On processors that support the Intel 64 architecture, the high-order 32 bits of each of RAX and RDX are ignored.) Undefined or reserved bits in an XCR should be set to values previously read.

This instruction must be executed at privilege level 0 or in real-address mode; otherwise, a general protection exception #GP(0) is generated. Specifying a reserved or unimplemented XCR in ECX will also cause a general protection exception. The processor will also generate a general protection exception if software attempts to write to reserved bits in an XCR.

Currently, only XCR0 (the XFEATURE_ENABLED_MASK register) is supported. Thus, all other values of ECX are reserved and will cause a #GP(0). Note that bit 0 of XCR0 (corresponding to x87 state) must be set to 1; the instruction will cause a #GP(0) if an attempt is made to clear this bit. Additionally, bit 1 of XCR0 (corresponding to AVX state) and bit 2 of XCR0 (corresponding to SSE state) must be set to 1 when using AVX registers; the instruction will cause a #GP(0) if an attempt is made to set XCR0[2:1] = 10.

**Operation**

XCR(ECX) ← EDX:EAX;

**Flags Affected**

None.

**Protected Mode Exceptions**

#GP(0) If the current privilege level is not 0.
If an invalid XCR is specified in ECX.
INSTRUCTION SET REFERENCE, M-Z

If the value in EDX:EAX sets bits that are reserved in the XCR specified by ECX.
If an attempt is made to clear bit 0 of XCR0.
If an attempt is made to set XCR0[2:1] = 10.

#UD
If CPUID.01H:ECX.XSAVE[bit 26] = 0.
If CR4.OSXSAVE[bit 18] = 0.
If the LOCK prefix is used.
If 66H, F3H or F2H prefix is used.

Real-Address Mode Exceptions
#GP
If an invalid XCR is specified in ECX.
If the value in EDX:EAX sets bits that are reserved in the XCR specified by ECX.
If an attempt is made to clear bit 0 of XCR0.
If an attempt is made to set XCR0[2:1] = 10.

#UD
If CPUID.01H:ECX.XSAVE[bit 26] = 0.
If CR4.OSXSAVE[bit 18] = 0.
If the LOCK prefix is used.
If 66H, F3H or F2H prefix is used.

Virtual-8086 Mode Exceptions
#GP(0) The XSETBV instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
CHAPTER 5
SAFER MODE EXTENSIONS REFERENCE

5.1 OVERVIEW

This chapter describes the Safer Mode Extensions (SMX) for the Intel 64 and IA-32 architectures. Safer Mode Extensions (SMX) provide a programming interface for system software to establish a measured environment within the platform to support trust decisions by end users. The measured environment includes:

- Measured launch of a system executive, referred to as a Measured Launched Environment (MLE)\(^1\). The system executive may be based on a Virtual Machine Monitor (VMM), a measured VMM is referred to as MVMM\(^2\).
- Mechanisms to ensure the above measurement is protected and stored in a secure location in the platform.
- Protection mechanisms that allow the VMM to control attempts to modify the VMM.

The measurement and protection mechanisms used by a measured environment are supported by the capabilities of an Intel® Trusted Execution Technology (Intel® TXT) platform:

- The SMX are the processor’s programming interface in an Intel TXT platform;
- The chipset in an Intel TXT platform provides enforcement of the protection mechanisms;
- Trusted Platform Module (TPM) 1.2 in the platform provides platform configuration registers (PCRs) to store software measurement values.

5.2 SMX FUNCTIONALITY

SMX functionality is provided in an Intel 64 processor through the GETSEC instruction via leaf functions. The GETSEC instruction supports multiple leaf functions. Leaf functions are selected by the value in EAX at the time GETSEC is executed. Each GETSEC leaf function is documented separately in the reference pages with a unique mnemonic (even though these mnemonics share the same opcode, 0F 37).

---

5.2.1 Detecting and Enabling SMX

Software can detect support for SMX operation using the CPUID instruction. If software executes CPUID with 1 in EAX, a value of 1 in bit 6 of ECX indicates support for SMX operation (GETSEC is available), see CPUID instruction for the layout of feature flags of reported by CPUID.01H:ECX.

System software enables SMX operation by setting CR4.SMXE[Bit 14] = 1 before attempting to execute GETSEC. Otherwise, execution of GETSEC results in the processor signaling an invalid opcode exception (#UD).

If the CPUID SMX feature flag is clear (CPUID.01H.ECX[Bit 6] = 0), attempting to set CR4.SMXE[Bit 14] results in a general protection exception.

The IA32_FEATURE_CONTROL MSR (at address 03AH) provides feature control bits that configure operation of VMX and SMX. These bits are documented in Table 5-1.

### Table 5-1. Layout of IA32_FEATURE_CONTROL

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Lock bit (0 = unlocked, 1 = locked). When set to ‘1’ further writes to this MSR are blocked.</td>
</tr>
<tr>
<td>1</td>
<td>Enable VMX in SMX operation</td>
</tr>
<tr>
<td>2</td>
<td>Enable VMX outside SMX operation</td>
</tr>
<tr>
<td>7:3</td>
<td>Reserved</td>
</tr>
<tr>
<td>14:8</td>
<td>SENTER Local Function Enables: When set, each bit in the field represents an enable control for a corresponding SENTER function.</td>
</tr>
<tr>
<td>15</td>
<td>SENTER Global Enable: Must be set to ‘1’ to enable operation of GETSEC[SENTER]</td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

- Bit 0 is a lock bit. If the lock bit is clear, an attempt to execute VMXON will cause a general-protection exception. Attempting to execute GETSEC[SENTER] when the lock bit is clear will also cause a general-protection exception. If the lock bit is set, WRMSR to the IA32_FEATURE_CONTROL MSR will cause a general-protection exception. Once the lock bit is set, the MSR cannot be modified until a power-on reset. System BIOS can use this bit to provide a setup option for BIOS to disable support for VMX, SMX or both VMX and SMX.
- Bit 1 enables VMX in SMX operation (between executing the SENTER and SEXIT leaves of GETSEC). If this bit is clear, an attempt to execute VMXON in SMX will cause a general-protection exception if executed in SMX operation. Attempts to set this bit on logical processors that do not support both VMX operation (Chapter 5, “Safer Mode Extensions Reference”) and SMX operation cause general-protection exceptions.
• Bit 2 enables VMX outside SMX operation. If this bit is clear, an attempt to execute VMXON will cause a general-protection exception if executed outside SMX operation. Attempts to set this bit on logical processors that do not support VMX operation cause general-protection exceptions.

• Bits 8 through 14 specify enabled functionality of the SENTER leaf function. Each bit in the field represents an enable control for a corresponding SENTER function. Only enabled SENTER leaf functionality can be used when executing SENTER.

• Bits 15 specify global enable of all SENTER functionalities.

5.2.2 SMX Instruction Summary

System software must first query for available GETSEC leaf functions by executing GETSEC[CAPABILITIES]. The CAPABILITIES leaf function returns a bit map of available GETSEC leaves. An attempt to execute an unsupported leaf index results in an undefined opcode (#UD) exception.

5.2.2.1 GETSEC[CAPABILITIES]

The SMX functionality provides an architectural interface for newer processor generations to extend SMX capabilities. Specifically, the GETSEC instruction provides a capability leaf function for system software to discover the available GETSEC leaf functions that are supported in a processor. Table 5-2 lists the currently available GETSEC leaf functions.

<table>
<thead>
<tr>
<th>Index (EAX)</th>
<th>Leaf function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>CAPABILITIES</td>
<td>Returns the available leaf functions of the GETSEC instruction</td>
</tr>
<tr>
<td>1</td>
<td>Undefined</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>ENTERACCS</td>
<td>Enter</td>
</tr>
<tr>
<td>3</td>
<td>EXITAC</td>
<td>Exit</td>
</tr>
<tr>
<td>4</td>
<td>SENTER</td>
<td>Launch an MLE</td>
</tr>
<tr>
<td>5</td>
<td>EXIT</td>
<td>Exit the MLE</td>
</tr>
<tr>
<td>6</td>
<td>PARAMETERS</td>
<td>Return SMX related parameter information</td>
</tr>
<tr>
<td>7</td>
<td>SMCTRL</td>
<td>SMX mode control</td>
</tr>
<tr>
<td>8</td>
<td>WAKEUP</td>
<td>Wake up sleeping processors in safer mode</td>
</tr>
<tr>
<td>9 - (4G-1)</td>
<td>Undefined</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
5.2.2.2  GETSEC[ENTERACCS]

The GETSEC[ENTERACCS] leaf enables authenticated code execution mode. The ENTERACCS leaf function performs an authenticated code module load using the chipset public key as the signature verification. ENTERACCS requires the existence of an Intel® Trusted Execution Technology capable chipset since it unlocks the chipset private configuration register space after successful authentication of the loaded module. The physical base address and size of the authenticated code module are specified as input register values in EBX and ECX, respectively.

While in the authenticated code execution mode, certain processor state properties change. For this reason, the time in which the processor operates in authenticated code execution mode should be limited to minimize impact on external system events.

Upon entry into , the previous paging context is disabled (since the authenticated code module image is specified with physical addresses and can no longer rely upon external memory-based page-table structures).

Prior to executing the GETSEC[ENTERACCS] leaf, system software must ensure the logical processor issuing GETSEC[ENTERACCS] is the boot-strap processor (BSP), as indicated by IA32_APIC_BASE.BSP = 1. System software must ensure other logical processors are in a suitable idle state and not marked as BSP.

The GETSEC[ENTERACCS] leaf may be used by different agents to load different authenticated code modules to perform functions related to different aspects of a measured environment, for example system software and Intel® TXT enabled BIOS may use more than one authenticated code modules.

5.2.2.3  GETSEC[EXITAC]

GETSEC[EXITAC] takes the processor out of . When this instruction leaf is executed, the contents of the authenticated code execution area are scrubbed and control is transferred to the non-authenticated context defined by a near pointer passed with the GETSEC[EXITAC] instruction.

The authenticated code execution area is no longer accessible after completion of GETSEC[EXITAC]. RBX (or EBX) holds the address of the near absolute indirect target to be taken.

5.2.2.4  GETSEC[SENTER]

The GETSEC[SENTER] leaf function is used by the initiating logical processor (ILP) to launch an MLE. GETSEC[SENTER] can be considered a superset of the ENTERACCS leaf, because it enters as part of the measured environment launch.

Measured environment startup consists of the following steps:

- the ILP rendezvous the responding logical processors (RLPs) in the platform into a controlled state (At the completion of this handshake, all the RLPs except for
the ILP initiating the measured environment launch are placed in a newly defined SENTER sleep state).

- Load and authenticate the authenticated code module required by the measured environment, and enter authenticated code execution mode.
- Verify and lock certain system configuration parameters.
- Measure the dynamic root of trust and store into the PCRs in TPM.
- Transfer control to the MLE with interrupts disabled.

Prior to executing the GETSEC[SENTER] leaf, system software must ensure the platform’s TPM is ready for access and the ILP is the boot-strap processor (BSP), as indicated by IA32_APIC_BASE.BSP. System software must ensure other logical processors (RLPs) are in a suitable idle state and not marked as BSP.

System software launching a measurement environment is responsible for providing a proper authentic code module address when executing GETSEC[SENTER]. The AC module responsible for the launch of a measured environment and loaded by GETSEC[SENTER] is referred to as SINIT. See Intel® Trusted Execution Technology Measured Launched Environment Programming Guide for additional information on system software requirements prior to executing GETSEC[SENTER].

5.2.2.5 GETSEC[SEXIT]

System software exits the measured environment by executing the instruction GETSEC[SEXIT] on the ILP. This instruction rendezvous the responding logical processors in the platform for exiting from the measured environment. External events (if left masked) are unmasked and Intel® TXT-capable chipset’s private configuration space is re-locked.

5.2.2.6 GETSEC[PARAMETERS]

The GETSEC[PARAMETERS] leaf function is used to report attributes, options and limitations of SMX operation. Software uses this leaf to identify operating limits or additional options.

The information reported by GETSEC[PARAMETERS] may require executing the leaf multiple times using EBX as an index. If the GETSEC[PARAMETERS] instruction leaf or if a specific parameter field is not available, then SMX operation should be interpreted to use the default limits of respective GETSEC leaves or parameter fields defined in the GETSEC[PARAMETERS] leaf.

5.2.2.7 GETSEC[SMCTRL]

The GETSEC[SMCTRL] leaf function is used for providing additional control over specific conditions associated with the SMX architecture. An input register is supported for selecting the control operation to be performed. See the specific leaf description for details on the type of control provided.
5.2.2.8 GETSEC[WAKEUP]
Responding logical processors (RLPs) are placed in the SENTER sleep state after the initiating logical processor executes GETSEC[SENTER]. The ILP can wake up RLPs to join the measured environment by using GETSEC[WAKEUP]. When the RLPs in SENTER sleep state wake up, these logical processors begin execution at the entry point defined in a data structure held in system memory (pointed to by an chipset register LT.MLE.JOIN) in TXT configuration space.

5.2.3 Measured Environment and SMX
This section gives a simplified view of a representative life cycle of a measured environment that is launched by a system executive using SMX leaf functions. Intel® Trusted Execution Technology Measured Launched Environment Programming Guide provides more detailed examples of using SMX and chipset resources (including chipset registers, Trusted Platform Module) to launch an MVMM.

The life cycle starts with the system executive (an OS, an OS loader, and so forth) loading the MLE and SINIT AC module into available system memory. The system executive must validate and parpare the platform for the measured launch. When the platform is properly configured, the system executive executes GETSEC[SENTER] on the initiating logical processor (ILP) to rendezvous the responding logical processors into an SENTER sleep state, the ILP then enters into using the SINIT AC module. In a multi-threaded or multi-processing environment, the system executive must ensure that other logical processors are already in an idle loop, or asleep (such as after executing HLT) before executing GETSEC[SENTER].

After the GETSEC[SENTER] rendezvous handshake is performed between all logical processors in the platform, the ILP loads the chipset authenticated code module (SINIT) and performs an authentication check. If the check passes, the processor hashes the SINIT AC module and stores the result into TPM PCR 17. It then switches execution context to the SINIT AC module. The SINIT AC module will perform a number of platform operations, including: verifying the system configuration, protecting the system memory used by the MLE from I/O devices capable of DMA, producing a hash of the MLE, storing the hash value in TPM PCR 18, and various other operations. When SINIT completes execution, it executes the GETSEC[EXITAC] instruction and transfers control the MLE at the designated entry point.

Upon receiving control from the SINIT AC module, the MLE must establish its protection and isolation controls before enabling DMA and interrupts and transferring control to other software modules. It must also wakeup the RLPs from their SENTER sleep state using the GETSEC[WAKEUP] instruction and bring them into its protection and isolation environment.

While executing in a measured environment, the MVMM can access the Trusted Platform Module (TPM) in locality 2. The MVMM has complete access to all TPM commands and may use the TPM to report current measurement values or use the measurement values to protect information such that only when the platform config-
uration registers (PCRs) contain the same value is the information released from the TPM. This protection mechanism is known as sealing.

A measured environment shutdown is ultimately completed by executing GETSEC[SEXIT]. Prior to this step system software is responsible for scrubbing sensitive information left in the processor caches, system memory.

### 5.3 GETSEC LEAF FUNCTIONS

This section provides detailed descriptions of each leaf function of the GETSEC instruction. GETSEC is available only if CPUID.01H:ECX[Bit 6] = 1. This indicates the availability of SMX and the GETSEC instruction. Before GETSEC can be executed, SMX must be enabled by setting CR4.SMXE[Bit 14] = 1.

A GETSEC leaf can only be used if it is shown to be available as reported by the GETSEC[CAPABILITIES] function. Attempts to access a GETSEC leaf index not supported by the processor, or if CR4.SMXE is 0, results in the signaling of an undefined opcode exception.

All GETSEC leaf functions are available in protected mode, including the compatibility sub-mode of IA-32e mode and the 64-bit sub-mode of IA-32e mode. Unless otherwise noted, the behavior of all GETSEC functions and interactions related to the measured environment are independent of IA-32e mode. This also applies to the interpretation of register widths passed as input parameters to GETSEC functions and to register results returned as output parameters.

The GETSEC functions ENTERACCS, SENTER, SEXIT, and WAKEUP require a Intel® TXT capable-chipset to be present in the platform. The GETSEC[CAPABILITIES] returned bit vector in position 0 indicates an Intel® TXT-capable chipset has been sampled present by the processor.

The processor's operating mode also affects the execution of the following GETSEC leaf functions: SMCTRL, ENTERACCS, EXITAC, SENTER, SEXIT, and WAKEUP. These functions are only allowed in protected mode at CPL = 0. They are not allowed while in SMM in order to prevent potential intra-mode conflicts. Further execution qualifications exist to prevent potential architectural conflicts (for example: nesting of the measured environment or authenticated code execution mode). See the definitions of the GETSEC leaf functions for specific requirements.

---

1. This chapter uses the 64-bit notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because processors that support SMX also support Intel 64 Architecture. The MVMM can be launched in IA-32e mode or outside IA-32e mode. The 64-bit notation of processor registers also refer to its 32-bit forms if SMX is used in 32-bit environment. In some places, notation such as EAX is used to refer specifically to lower 32 bits of the indicated register.

2. Sampled present means that the processor sent a message to the chipset and the chipset responded that it (a) knows about the message and (b) is capable of executing SENTER. This means that the chipset CAN support Intel® TXT, and is configured and WILLING to support it.
For the purpose of performance monitor counting, the execution of GETSEC functions is counted as a single instruction with respect to retired instructions. The response by a responding logical processor (RLP) to messages associated with GETSEC[SENTER] or GTSEC[SEXIT] is transparent to the retired instruction count on the ILP.
GETSEC[CAPABILITIES] - Report the SMX Capabilities

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 37</td>
<td>GETSEC[CAPABILITIES]</td>
<td>Report the SMX capabilities. The capabilities index is input in EBX with the result returned in EAX.</td>
</tr>
</tbody>
</table>

**Description**

The GETSEC[CAPABILITIES] function returns a bit vector of supported GETSEC leaf functions. The CAPABILITIES leaf of GETSEC is selected with EAX set to 0 at entry. EBX is used as the selector for returning the bit vector field in EAX. GETSEC[CAPABILITIES] may be executed at all privilege levels, but the CR4.SMXE bit must be set or an undefined opcode exception (#UD) is returned.

With EBX = 0 upon execution of GETSEC[CAPABILITIES], EAX returns the a bit vector representing status on the presence of a Intel® TXT-capable chipset and the first 30 available GETSEC leaf functions. The format of the returned bit vector is provided in Table 5-3.

If bit 0 is set to 1, then an Intel® TXT-capable chipset has been sampled present by the processor. If bits in the range of 1-30 are set, then the corresponding GETSEC leaf function is available. If the bit value at a given bit index is 0, then the GETSEC leaf function corresponding to that index is unsupported and attempted execution results in a #UD.

Bit 31 of EAX indicates if further leaf indexes are supported. If the Extended Leafs bit 31 is set, then additional leaf functions are accessed by repeating GETSEC[CAPABILITIES] with EBX incremented by one. When the most significant bit of EAX is not set, then additional GETSEC leaf functions are not supported; indexing EBX to a higher value results in EAX returning zero.

**Table 5-3. Getsec Capability Result Encoding (EBX = 0)**

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chipset Present</td>
<td>0</td>
<td>Intel® TXT-capable chipset is present</td>
</tr>
<tr>
<td>Undefined</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>ENTERACCS</td>
<td>2</td>
<td>GETSEC[ENTERACCS] is available</td>
</tr>
<tr>
<td>EXITAC</td>
<td>3</td>
<td>GETSEC[EXITAC] is available</td>
</tr>
<tr>
<td>SENTER</td>
<td>4</td>
<td>GETSEC[SENTER] is available</td>
</tr>
<tr>
<td>SEXIT</td>
<td>5</td>
<td>GETSEC[SEXIT] is available</td>
</tr>
</tbody>
</table>
Table 5-3. Getsec Capability Result Encoding (EBX = 0) (Contd.)

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PARAMETERS</td>
<td>6</td>
<td>GETSEC[PARAMETERS] is available</td>
</tr>
<tr>
<td>SMCTRL</td>
<td>7</td>
<td>GETSEC[SMCTRL] is available</td>
</tr>
<tr>
<td>WAKEUP</td>
<td>8</td>
<td>GETSEC[WAKEUP] is available</td>
</tr>
<tr>
<td>Undefined</td>
<td>30:9</td>
<td>Reserved</td>
</tr>
<tr>
<td>Extended Leafs</td>
<td>31</td>
<td>Reserved for extended information reporting of GETSEC capabilities</td>
</tr>
</tbody>
</table>

Operation

IF (CR4.SMXE=0)
    THEN #UD;
ELSIF (in VMX non-root operation)
    THEN VM Exit (reason="GETSEC instruction");
IF (EBX=0) THEN
    BitVector← 0;
    IF (TXT chipset present)
        BitVector[Chipset present]← 1;
    IF (ENTERACCS Available)
        THEN BitVector[ENTERACCS]← 1;
    IF (EXITAC Available)
        THEN BitVector[EXITAC]← 1;
    IF (SENTER Available)
        THEN BitVector[SENTER]← 1;
    IF (SEXIT Available)
        THEN BitVector[SEXIT]← 1;
    IF (PARAMETERS Available)
        THEN BitVector[PARAMETERS]← 1;
    IF (SMCTRL Available)
        THEN BitVector[SMCTRL]← 1;
    IF (WAKEUP Available)
        THEN BitVector[WAKEUP]← 1;
    EAX← BitVector;
ELSE
    EAX← 0;
END;

Flags Affected

None
Use of Prefixes

LOCK Causes #UD
REP* Cause #UD (includes REPNE/REPNZ and REP/REPE/REPZ)
Operand size Causes #UD
Segment overrides Ignored
Address size Ignored
REX Ignored

Protected Mode Exceptions

#UD IF CR4.SMXE = 0.

Real-Address Mode Exceptions

#UD IF CR4.SMXE = 0.

Virtual-8086 Mode Exceptions

#UD IF CR4.SMXE = 0.

Compatibility Mode Exceptions

#UD IF CR4.SMXE = 0.

64-Bit Mode Exceptions

#UD IF CR4.SMXE = 0.

VM-exit Condition

Reason (GETSEC) IF in VMX non-root operation.
Description

The GETSEC[ENTERACCS] function loads, authenticates and executes an authenticated code module using an Intel® TXT platform chipset's public key. The ENTERACCS leaf of GETSEC is selected with EAX set to 2 at entry.

There are certain restrictions enforced by the processor for the execution of the GETSEC[ENTERACCS] instruction:

- Execution is not allowed unless the processor is in protected mode or IA-32e mode with CPL = 0 and EFLAGS.VM = 0.
- Processor cache must be available and not disabled, that is, CR0.CD and CR0.NW bits must be 0.
- For processor packages containing more than one logical processor, CR0.CD is checked to ensure consistency between enabled logical processors.
- For enforcing consistency of operation with numeric exception reporting using Interrupt 16, CR0.NE must be set.
- An Intel TXT-capable chipset must be present as communicated to the processor by sampling of the power-on configuration capability field after reset.
- The processor can not already be in authenticated code execution mode as launched by a previous GETSEC[ENTERACCS] or GETSEC[SENTER] instruction without a subsequent exiting using GETSEC[EXITAC].
- To avoid potential operability conflicts between modes, the processor is not allowed to execute this instruction if it currently is in SMM or VMX operation.
- To insure consistent handling of SIPI messages, the processor executing the GETSEC[ENTERACCS] instruction must also be designated the BSP (boot-strap processor) as defined by A32_APIC_BASE.BSP (Bit 8).

Failure to conform to the above conditions results in the processor signaling a general protection exception.

Prior to execution of the ENTERACCS leaf, other logical processors, i.e. RLPs, in the platform must be:

- idle in a wait-for-SIPI state (as initiated by an INIT assertion or through reset for non-BSP designated processors), or
- in the SENTER sleep state as initiated by a GETSEC[SENTER] from the initiating logical processor (ILP).

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 37</td>
<td>GETSEC[ENTERACCS]</td>
<td>Enter authenticated code execution mode. EBX holds the authenticated code module physical base address. ECX holds the authenticated code module size (bytes).</td>
</tr>
</tbody>
</table>
If other logical processor(s) in the same package are not idle in one of these states, execution of ENTERACCS signals a general protection exception. The same requirement and action applies if the other logical processor(s) of the same package do not have CR0.CD = 0.

A successful execution of ENTERACCS results in the ILP entering an authenticated code execution mode. Prior to reaching this point, the processor performs several checks. These include:

- Establish and check the location and size of the specified authenticated code module to be executed by the processor.
- Inhibit the ILP’s response to the external events: INIT, A20M, NMI and SMI.
- Broadcast a message to enable protection of memory and I/O from other processor agents.
- Load the designated code module into an authenticated code execution area.
- Isolate the contents of the authenticated code execution area from further state modification by external agents.
- Authenticate the authenticated code module.
- Initialize the initiating logical processor state based on information contained in the authenticated code module header.
- Unlock the Intel® TXT-capable chipset private configuration space and TPM locality 3 space.
- Begin execution in the authenticated code module at the defined entry point.

The GETSEC[ENTERACCS] function requires two additional input parameters in the general purpose registers EBX and ECX. EBX holds the authenticated code (AC) module physical base address (the AC module must reside below 4 GBytes in physical address space) and ECX holds the AC module size (in bytes). The physical base address and size are used to retrieve the code module from system memory and load it into the internal authenticated code execution area. The base physical address is checked to verify it is on a modulo-4096 byte boundary. The size is verified to be a multiple of 64, that it does not exceed the internal authenticated code execution area capacity (as reported by GETSEC[CAPABILITIES]), and that the top address of the AC module does not exceed 32 bits. An error condition results in an abort of the authenticated code execution launch and the signaling of a general protection exception.

As an integrity check for proper processor hardware operation, execution of GETSEC[ENTERACCS] will also check the contents of all the machine check status registers (as reported by the MSRs IA32_MCI_STATUS) for any valid uncorrectable error condition. In addition, the global machine check status register IA32_MCG_STATUS MCIP bit must be cleared and the IERR processor package pin (or its equivalent) must not be asserted, indicating that no machine check exception processing is currently in progress. These checks are performed prior to initiating the load of the authenticated code module. Any outstanding valid uncorrectable machine check error condition present in these status registers at this point will result in the processor signaling a general protection violation.
The ILP masks the response to the assertion of the external signals INIT#, A20M, NMI#, and SMI#. This masking remains active until optionally unmasked by GETSEC[EXITAC] (this defined unmasking behavior assumes GETSEC[ENTERACCS] was not executed by a prior GETSEC[SENTER]). The purpose of this masking control is to prevent exposure to existing external event handlers that may not be under the control of the authenticated code module.

The ILP sets an internal flag to indicate it has entered authenticated code execution mode. The state of the A20M pin is likewise masked and forced internally to a de-asserted state so that any external assertion is not recognized during authenticated code execution mode.

To prevent other (logical) processors from interfering with the ILP operating in authenticated code execution mode, memory (excluding implicit write-back transactions) access and I/O originating from other processor agents are blocked. This protection starts when the ILP enters into authenticated code execution mode. Only memory and I/O transactions initiated from the ILP are allowed to proceed. Exiting authenticated code execution mode is done by executing GETSEC[EXITAC]. The protection of memory and I/O activities remains in effect until the ILP executes GETSEC[EXITAC].

Prior to launching the authenticated execution module using GETSEC[ENTERACCS] or GETSEC[SENTER], the processor’s MTRRs (Memory Type Range Registers) must first be initialized to map out the authenticated RAM addresses as WB (writeback). Failure to do so may affect the ability for the processor to maintain isolation of the loaded authenticated code module. If the processor detected this requirement is not met, it will signal an Intel® TXT reset condition with an error code during the loading of the authenticated code module.

While physical addresses within the load module must be mapped as WB, the memory type for locations outside of the module boundaries must be mapped to one of the supported memory types as returned by GETSEC[PARAMETERS] (or UC as default).

To conform to the minimum granularity of MTRR MSRs for specifying the memory type, authenticated code RAM (ACRAM) is allocated to the processor in 4096 byte granular blocks. If an AC module size as specified in ECX is not a multiple of 4096 then the processor will allocate up to the next 4096 byte boundary for mapping as ACRAM with indeterminate data. This pad area will not be visible to the authenticated code module as external memory nor can it depend on the value of the data used to fill the pad area.

At the successful completion of GETSEC[ENTERACCS], the architectural state of the processor is partially initialized from contents held in the header of the authenticated code module. The processor GDTR, CS, and DS selectors are initialized from fields within the authenticated code module. Since the authenticated code module must be relocatable, all address references must be relative to the authenticated code module base address in EBX. The processor GDTR base value is initialized to the AC module header field GDTBasePtr + module base address held in EBX and the GDTR limit is set to the value in the GDTLimit field. The CS selector is initialized to the AC module header SegSel field, while the DS selector is initialized to CS + 8. The segment
descriptor fields are implicitly initialized to BASE=0, LIMIT=FFFFFFFFh, G=1, D=1, P=1, S=1, read/write access for DS, and execute/read access for CS. The processor begins the authenticated code module execution with the EIP set to the AC module header EntryPoint field + module base address (EBX). The AC module based fields used for initializing the processor state are checked for consistency and any failure results in a shutdown condition.

A summary of the register state initialization after successful completion of GETSEC[ENTERACCS] is given for the processor in Table 5-4. The paging is disabled upon entry into authenticated code execution mode. The authenticated code module is loaded and initially executed using physical addresses. It is up to the system software after execution of GETSEC[ENTERACCS] to establish a new (or restore its previous) paging environment with an appropriate mapping to meet new protection requirements. EBP is initialized to the authenticated code module base physical address for initial execution in the authenticated environment. As a result, the authenticated code can reference EBP for relative address based references, given that the authenticated code module must be position independent.

Table 5-4. Register State Initialization after GETSEC[ENTERACCS]

<table>
<thead>
<tr>
<th>Register State</th>
<th>Initialization Status</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>CR0</td>
<td>PG←0, AM←0, WP←0: Others unchanged</td>
<td>Paging, Alignment Check, Write-protection are disabled</td>
</tr>
<tr>
<td>CR4</td>
<td>MCE←0: Others unchanged</td>
<td>Machine Check Exceptions Disabled</td>
</tr>
<tr>
<td>EFLAGS</td>
<td>000000002H</td>
<td>IA-32e mode disabled</td>
</tr>
<tr>
<td>IA32_EFER</td>
<td>0H</td>
<td></td>
</tr>
<tr>
<td>EIP</td>
<td>AC.base + EntryPoint</td>
<td>AC.base is in EBX as input to GETSEC[ENTERACCS]</td>
</tr>
<tr>
<td>ECX</td>
<td>Pre-ENTERACCS state: [31:16]=GDTR.limit; [15:0]=CS.sel</td>
<td>Carry forward processor state across GETSEC[ENTERACCS]</td>
</tr>
<tr>
<td>[E</td>
<td>R]DX</td>
<td>Pre-ENTERACCS state: GDTR base</td>
</tr>
<tr>
<td>EBP</td>
<td>AC.base</td>
<td></td>
</tr>
<tr>
<td>CS</td>
<td>Sel=[SegSel], base=0, limit=FFFFFFFFh, G=1, D=1, AR=9BH</td>
<td></td>
</tr>
<tr>
<td>DS</td>
<td>Sel=[SegSel] +8, base=0, limit=FFFFFFFFh, G=1, D=1, AR=93H</td>
<td></td>
</tr>
</tbody>
</table>
The segmentation related processor state that has not been initialized by GETSEC[ENTERACCS] requires appropriate initialization before use. Since a new GDT context has been established, the previous state of the segment selector values held in ES, SS, FS, GS, TR, and LDTR might not be valid.

The MSR IA32_EFER is also unconditionally cleared as part of the processor state initialized by ENTERACCS. Since paging is disabled upon entering authenticated code execution mode, a new paging environment will have to be reestablished in order to establish IA-32e mode while operating in authenticated code execution mode.

Debug exception and trap related signaling is also disabled as part of GETSEC[ENTERACCS]. This is achieved by resetting DR7, TF in EFLAGS, and the MSR IA32_DEBUGCTL. These debug functions are free to be re-enabled once supporting exception handler(s), descriptor tables, and debug registers have been properly initialized following entry into authenticated code execution mode. Also, any pending single-step trap condition will have been cleared upon entry into this mode.

The IA32_MISC_ENABLE MSR is initialized upon entry into authenticated execution mode. Certain bits of this MSR are preserved because preserving these bits may be important to maintain previously established platform settings (See the footnote for Table 5-5.). The remaining bits are cleared for the purpose of establishing a more consistent environment for the execution of authenticated code modules. One of the impacts of initializing this MSR is any previous condition established by the MONITOR instruction will be cleared.

To support the possible return to the processor architectural state prior to execution of GETSEC[ENTERACCS], certain critical processor state is captured and stored in the general-purpose registers at instruction completion. [E|R]BX holds effective address ([E|R]IP) of the instruction that would execute next after GETSEC[ENTERACCS], ECX[15:0] holds the CS selector value, ECX[31:16] holds the GDTR limit field, and [E|R]DX holds the GDTR base field. The subsequent authenticated code can preserve the contents of these registers so that this state can be manually restored if needed, prior to exiting authenticated code execution mode with GETSEC(EXITAC). For the processor state after exiting authenticated code execution mode, see the description of GETSEC[SEXIT].
The IDTR will also require reloading with a new IDT context after entering authenticated code execution mode, before any exceptions or the external interrupts INTR and NMI can be handled. Since external interrupts are re-enabled at the completion of authenticated code execution mode (as terminated with EXITAC), it is recommended that a new IDT context be established before this point. Until such a new IDT context is established, the programmer must take care in not executing an INT n instruction or any other operation that would result in an exception or trap signaling.

Prior to completion of the GETSEC[ENTERACCS] instruction and after successful authentication of the AC module, the private configuration space of the Intel TXT chipset is unlocked. The authenticated code module alone can gain access to this normally restricted chipset state for the purpose of securing the platform.

---

### Table 5-5. IA32_MISC_ENABLE MSR Initialization\(^1\) by ENTERACCS and SENTER

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast strings enable</td>
<td>0</td>
<td>Clear to 0</td>
</tr>
<tr>
<td>FOPCODE compatibility mode enable</td>
<td>2</td>
<td>Clear to 0</td>
</tr>
<tr>
<td>Thermal monitor enable</td>
<td>3</td>
<td>Set to 1 if other thermal monitor capability is not enabled.(^2)</td>
</tr>
<tr>
<td>Split-lock disable</td>
<td>4</td>
<td>Clear to 0</td>
</tr>
<tr>
<td>Bus lock on cache line splits disable</td>
<td>8</td>
<td>Clear to 0</td>
</tr>
<tr>
<td>Hardware prefetch disable</td>
<td>9</td>
<td>Clear to 0</td>
</tr>
<tr>
<td>GV1/2 legacy enable</td>
<td>15</td>
<td>Clear to 0</td>
</tr>
<tr>
<td>MONITOR/MWAIT s/m enable</td>
<td>18</td>
<td>Clear to 0</td>
</tr>
<tr>
<td>Adjacent sector prefetch disable</td>
<td>19</td>
<td>Clear to 0</td>
</tr>
</tbody>
</table>

**NOTES:**

1. The number of IA32_MISC_ENABLE fields that are initialized may vary due to processor implementations.
2. ENTERACCS (and SENTER) initialize the state of processor thermal throttling such that at least a minimum level is enabled. If thermal throttling is already enabled when executing one of the GETSEC leaves, then no change in the thermal throttling control settings will occur. If thermal throttling is disabled, then it will be enabled via setting of the thermal throttle control bit 3 as a result of executing these GETSEC leaves.
SAFER MODE EXTENSIONS REFERENCE

Once the authenticated code module is launched at the completion of GETSEC[ENTERACCS], it is free to enable interrupts by setting EFLAGS.IF and enable NMI by execution of IRET. This presumes that it has re-established interrupt handling support through initialization of the IDT, GDT, and corresponding interrupt handling code.

Operation in a Uni-Processor Platform

(* The state of the internal flag ACMODEFLAG persists across instruction boundary *)

IF (CR4.SMXE=0)
   THEN #UD;
ELSIF (in VMX non-root operation)
   THEN VM Exit (reason="GETSEC instruction");
ELSIF (GETSEC leaf unsupported)
   THEN #UD;
ELSIF (in VMX operation) or
   (CR0.PE=0) or (CR0.CD=1) or (CR0.NW=1) or (CR0.NE=0) or
   (CPL>0) or (EFLAGS.VM=1) or
   (IA32_APIC_BASE.BSP=0) or
   (TXT chipset not present) or
   (ACMODEFLAG=1) or (IN_SMM=1))
   THEN #GP(0);
IF (GETSEC[PARAMETERS].Parameter_Type = 5, MCA_Handling (bit 6) = 0)
   FOR I = 0 to IA32_MCG_CAP.COUNT-1 DO
   IF (IA32_MC[I].STATUS = uncorrectable error)
      THEN #GP(0);
   OD;
IF (IA32_MCG_STATUS.MCIP=1) or (IERR pin is asserted)
   THEN #GP(0);
ACBASE← EBX;
ACSIZE← ECX;
IF (((ACBASE MOD 4096) != 0) or ((ACSIZE MOD 64 )!= 0 ) or (ACSIZE < minimum module size) OR
(ACSIZE > authenticated RAM capacity)) or ((ACBASE+ACSIZE) > (2^32 -1)))
   THEN #GP(0);
IF (secondary thread(s) CR0.CD = 1) or ((secondary thread(s) NOT(wait-for-SIPI)) and
   (secondary thread(s) not in SENTER sleep state)
   THEN #GP(0);
Mask SMI, INIT, A20M, and NMI external pin events;
IA32_MISC_ENABLE← (IA32_MISC_ENABLE & MASK_CONST*)
(* The hexadecimal value of MASK_CONST may vary due to processor implementations *)
A20M← 0;
IA32_DEBUGCTL← 0;
Invalidate processor TLB(s);
Drain Outgoing Transactions;
ACMODEFLAG ← 1;
SignalTXTMessage(ProcessorHold);
Load the internal ACRAM based on the AC module size;
(* Ensure that all ACRAM loads hit Write Back memory space *)
IF (ACRAM memory type != WB)
    THEN TXT-SHUTDOWN(#BadACMMType);
IF (AC module header version is not supported) OR (ACRAM[ModuleType] <> 2)
    THEN TXT-SHUTDOWN(#UnsupportedACM);
    (* Authenticate the AC Module and shutdown with an error if it fails *)
KEY ← GETKEY(ACRAM, ACBASE);
KEYHASH ← HASH(KEY);
CSKEYHASH ← READ(TXT.PUBLIC.KEY);
IF (KEYHASH <> CSKEYHASH)
    THEN TXT-SHUTDOWN(#AuthenticateFail);
SIGNATURE ← DECRIPT(ACRAM, ACBASE, KEY);
    (* The value of SIGNATURE_LEN_CONST is implementation-specific *)
FOR I=0 to SIGNATURE_LEN_CONST - 1 DO
    ACRAM[SCRATCH.I] ← SIGNATURE[I];
COMPUTEDSIGNATURE ← HASH(ACRAM, ACBASE, ACSIZE);
FOR I=0 to SIGNATURE_LEN_CONST - 1 DO
    ACRAM[SCRATCH.SIGNATURE_LEN_CONST+I] ← COMPUTEDSIGNATURE[I];
IF (SIGNATURE <> COMPUTEDSIGNATURE)
    THEN TXT-SHUTDOWN(#AuthenticateFail);
ACMCONTROL ← ACRAM[CodeControl];
IF ((ACMCONTROL.0 = 0) and (ACMCONTROL.1 = 1) and (snoop hit to modified line detected on ACRAM load))
    THEN TXT-SHUTDOWN(#UnexpectedHITM);
IF (ACMCONTROL reserved bits are set)
    THEN TXT-SHUTDOWN(#BadACMFormat);
IF ((ACRAM[GDTBasePtr] < (ACRAM[HeaderLen] * 4 + Scratch_size)) OR
     ((ACRAM[GDTBasePtr] + ACRAM[GDTLimit]) >= ACSIZE))
    THEN TXT-SHUTDOWN(#BadACMFormat);
IF ((ACMCONTROL.0 = 1) and (ACMCONTROL.1 = 1) and (snoop hit to modified line detected on ACRAM load))
    THEN ACEntryPoint ← ACRBASE+ACRAM[ErrorEntryPoint];
ELSE
    ACEntryPoint ← ACRBASE+ACRAM[EntryPoint];
IF ((ACEntryPoint >= ACSIZE) OR (ACEntryPoint < (ACRAM[HeaderLen] * 4 + Scratch_size)))
    THEN TXT-SHUTDOWN(#BadACMFormat);
IF (ACRAM[GDTLimit] & FFFF0000h)
    THEN TXT-SHUTDOWN(#BadACMFormat);
IF ((ACRAM[SegSel] > (ACRAM[GDTLimit] - 15)) OR (ACRAM[SegSel] < 8))
    THEN TXT-SHUTDOWN(#BadACMFormat);
IF ((ACRAM[SegSel].TI=1) OR (ACRAM[SegSel].RPL!=0))
SAFER MODE EXTENSIONS REFERENCE

THEN TXT-SHUTDOWN(#BadACMFormat);
CR0.[PG.AM.WP]← 0;
CR4.MCE← 0;
EFLAGS← 00000002h;
IA32_EFER← 0h;
[E|R]BX← [E|R]IP of the instruction after GETSEC[ENTERACCS];
ECX← Pre-GETSEC[ENTERACCS] GDT.limit:CS.sel;
[E|R]DX← Pre-GETSEC[ENTERACCS] GDT.base;
EBP← ACBASE;
GDTR.BASE← ACBASE+ACRAM[GDTBasePtr];
GDTR.LIMIT← ACRAM[GDTLimit];
CS.SEL← ACRAM[SegSel];
CS.BASE← 0;
CS.LIMIT← FFFFDh;
CS.G← 1;
CS.D← 1;
CS.AR← 9Bh;
DS.SEL← ACRAM[SegSel]+8;
DS.BASE← 0;
DS.LIMIT← FFFFFFFh;
DS.G← 1;
DS.D← 1;
DS.AR← 93h;
DR7← 00000400h;
IA32_DEBUGCTL← 0;
SignalTXTMsg(OpenPrivate);
SignalTXTMsg(OpenLocality3);
EIP← ACEntryPoint;
END;

Flags Affected
All flags are cleared.

Use of Prefixes

LOCK Causes #UD
REP* Cause #UD (includes REPNE/REPNZ and REP/REPE/REPZ)
Operand size Causes #UD
Segment overrides Ignored
Address size Ignored
REX Ignored
Protected Mode Exceptions

#UD  If CR4.SMXE = 0.
     If GETSEC[ENTERACCS] is not reported as supported by
     GETSEC[CAPABILITIES].

#GP(0)  If CR0.CD = 1 or CR0.NW = 1 or CR0.NE = 0 or CR0.PE = 0 or
        CPL > 0 or EFLAGS.VM = 1.
     If a Intel® TXT-capable chipset is not present.
     If in VMX root operation.
     If the initiating processor is not designated as the bootstrap
     processor via the MSR bit IA32_APIC_BASE.BSP.
     If the processor is already in authenticated code execution
     mode.
     If the processor is in SMM.
     If a valid uncorrectable machine check error is logged in
     IA32_MC[I]_STATUS.
     If the authenticated code base is not on a 4096 byte boundary.
     If the authenticated code size > processor internal authenti-
     cated code area capacity.
     If the authenticated code size is not modulo 64.
     If other enabled logical processor(s) of the same package
     CR0.CD = 1.
     If other enabled logical processor(s) of the same package are
     not in the wait-for-SIPI or SENTER sleep state.

Real-Address Mode Exceptions

#UD  If CR4.SMXE = 0.
     If GETSEC[ENTERACCS] is not reported as supported by
     GETSEC[CAPABILITIES].

#GP(0)  GETSEC[ENTERACCS] is not recognized in real-address mode.

Virtual-8086 Mode Exceptions

#UD  If CR4.SMXE = 0.
     If GETSEC[ENTERACCS] is not reported as supported by
     GETSEC[CAPABILITIES].

#GP(0)  GETSEC[ENTERACCS] is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions

All protected mode exceptions apply.

#GP  IF AC code module does not reside in physical address below
     2^32 -1.
SAFER MODE EXTENSIONS REFERENCE

64-Bit Mode Exceptions
All protected mode exceptions apply.
#GP IF AC code module does not reside in physical address below
2^32 -1.

VM-exit Condition
Reason (GETSEC) IF in VMX non-root operation.
GETSEC[EXITAC]—Exit Authenticated Code Execution Mode

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 37</td>
<td>GETSEC[EXITAC]</td>
<td>Exit authenticated code execution mode. RBX holds the Near Absolute Indirect jump target and EDX hold the exit parameter flags</td>
</tr>
</tbody>
</table>

**Description**

The GETSEC[EXITAC] leaf function exits the ILP out of authenticated code execution mode established by GETSEC[ENTERACCS] or GETSEC[SENTER]. The EXITAC leaf of GETSEC is selected with EAX set to 3 at entry. EBX (or RBX, if in 64-bit mode) holds the near jump target offset for where the processor execution resumes upon exiting authenticated code execution mode. EDX contains additional parameter control information. Currently only an input value of 0 in EDX is supported. All other EDX settings are considered reserved and result in a general protection violation.

GETSEC[EXITAC] can only be executed if the processor is in protected mode with CPL = 0 and EFLAGS.VM = 0. The processor must also be in authenticated code execution mode. To avoid potential operability conflicts between modes, the processor is not allowed to execute this instruction if it is in SMM or in VMX operation. A violation of these conditions results in a general protection violation.

Upon completion of the GETSEC[EXITAC] operation, the processor unmask responses to external event signals INIT#, NMI#, and SMI#. This unmasking is performed conditionally, based on whether the authenticated code execution mode was entered via execution of GETSEC[SENTER] or GETSEC[ENTERACCS]. If the processor is in authenticated code execution mode due to the execution of GETSEC[SENTER], then these external event signals will remain masked. In this case, A20M is kept disabled in the measured environment until the measured environment executes GETSEC[SEXIT]. INIT# is unconditionally unmasked by EXITAC. Note that any events that are pending, but have been blocked while in authenticated code execution mode, will be recognized at the completion of the GETSEC[EXITAC] instruction if the pin event is unmasked.

The intent of providing the ability to optionally leave the pin events SMI#, and NMI# masked is to support the completion of a measured environment bring-up that makes use of VMX. In this envisioned security usage scenario, these events will remain masked until an appropriate virtual machine has been established in order to field servicing of these events in a safer manner. Details on when and how events are masked and unmasked in VMX operation are described in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C*. It should be cautioned that if no VMX environment is to be activated following GETSEC[EXITAC], that these events will remain masked until the measured environment is exited with GETSEC[SEXIT]. If this is not desired then the GETSEC function SMCTRL(0) can be used for unmasking SMI# in this context. NMI# can be correspondingly unmasked by execution of IRET.
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A successful exit of the authenticated code execution mode requires the ILP to perform additional steps as outlined below:

- Invalidate the contents of the internal authenticated code execution area.
- Invalidate processor TLBs.
- Clear the internal processor AC Mode indicator flag.
- Re-lock the TPM locality 3 space.
- Unlock the Intel® TXT-capable chipset memory and I/O protections to allow memory and I/O activity by other processor agents.
- Perform a near absolute indirect jump to the designated instruction location.

The content of the authenticated code execution area is invalidated by hardware in order to protect it from further use or visibility. This internal processor storage area can no longer be used or relied upon after GETSEC[EXITAC]. Data structures need to be re-established outside of the authenticated code execution area if they are to be referenced after EXITAC. Since addressed memory content formerly mapped to the authenticated code execution area may no longer be coherent with external system memory after EXITAC, processor TLBs in support of linear to physical address translation are also invalidated.

Upon completion of GETSEC[EXITAC] a near absolute indirect transfer is performed with EIP loaded with the contents of EBX (based on the current operating mode size). In 64-bit mode, all 64 bits of RBX are loaded into RIP if REX.W precedes GETSEC[EXITAC]. Otherwise RBX is treated as 32 bits even while in 64-bit mode. Conventional CS limit checking is performed as part of this control transfer. Any exception conditions generated as part of this control transfer will be directed to the existing IDT; thus it is recommended that an IDTR should also be established prior to execution of the EXITAC function if there is a need for fault handling. In addition, any segmentation related (and paging) data structures to be used after EXITAC should be re-established or validated by the authenticated code prior to EXITAC.

In addition, any segmentation related (and paging) data structures to be used after EXITAC need to be re-established and mapped outside of the authenticated RAM designated area by the authenticated code prior to EXITAC. Any data structure held within the authenticated RAM allocated area will no longer be accessible after completion by EXITAC.

**Operation**

(* The state of the internal flag ACMODEFLAG and SENTERFLAG persist across instruction boundary *)

IF (CR4.SMXE=0)
  THEN #UD;
ELSIF ( in VMX non-root operation)
  THEN VM Exit (reason="GETSEC instruction");
ELSIF (GETSEC leaf unsupported)
  THEN #UD;
ELSIF ((in VMX operation) or ( in 64-bit mode) and ( RBX is non-canonical))
  THEN #UD;
(CR0.PE=0) or (CPL>0) or (EFLAGS.VM=1) or
(ACMODEFLAG=0) or (IN_SMM=1)) or (EDX != 0))
THEN #GP(0);
IF (OperandSize = 32)
THEN tempEIP← EBX;
ELSIF (OperandSize = 64)
THEN tempEIP← RBX;
ELSE
   tempEIP← EBX AND 0000FFFFH;
IF (tempEIP > code segment limit)
THEN #GP(0);
Invalidate ACRAM contents;
Invalidate processor TLB(s);
Drain outgoing messages;
SignalTXTMsg(CloseLocality3);
SignalTXTMsg(LockSMRAM);
SignalTXTMsg(ProcessorRelease);
Unmask INIT;
IF (SENTERFLAG=0)
   THEN Unmask SMI, INIT, NMI, and A20M pin event;
ELSEIF (IA32_SMM_MONITOR_CTL[0] = 0)
   THEN Unmask SMI pin event;
ACMODEFLAG← 0;
EIP← tempEIP;
END;

Flags Affected
None.

Use of Prefixes
LOCK  Causes #UD
REP*  Cause #UD (includes REPNE/REPNZ and REP/REPE/REPSZ)
Operand size  Causes #UD
Segment overrides  Ignored
Address size  Ignored
REX.W  Sets 64-bit mode Operand size attribute

Protected Mode Exceptions
#UD  If CR4.SMXE = 0.
     If GETSEC(EXITAC] is not reported as supported by
     GETSEC[CAPABILITIES].
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#GP(0) If CR0.PE = 0 or CPL>0 or EFLAGS.VM =1.
If in VMX root operation.
If the processor is not currently in authenticated code execution mode.
If the processor is in SMM.
If any reserved bit position is set in the EDX parameter register.

Real-Address Mode Exceptions
#UD If CR4.SMXE = 0.
If GETSEC[EXITAC] is not reported as supported by
GETSEC[CAPABILITIES].
#GP(0) GETSEC[EXITAC] is not recognized in real-address mode.

Virtual-8086 Mode Exceptions
#UD If CR4.SMXE = 0.
If GETSEC[EXITAC] is not reported as supported by
GETSEC[CAPABILITIES].
#GP(0) GETSEC[EXITAC] is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
All protected mode exceptions apply.

64-Bit Mode Exceptions
All protected mode exceptions apply.
#GP(0) If the target address in RBX is not in a canonical form.

VM-Exit Condition
Reason (GETSEC) IF in VMX non-root operation.
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GETSEC[SENTER]—Enter a Measured Environment

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 37</td>
<td>GETSEC[SENTER]</td>
<td>Launch a measured environment</td>
</tr>
<tr>
<td>(EAX=4)</td>
<td></td>
<td>EBX holds the SINIT authenticated code module physical base address.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ECX holds the SINIT authenticated code module size (bytes).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EDX controls the level of functionality supported by the measured environment launch.</td>
</tr>
</tbody>
</table>

Description

The GETSEC[SENTER] instruction initiates the launch of a measured environment and places the initiating logical processor (ILP) into the authenticated code execution mode. The SENTER leaf of GETSEC is selected with EAX set to 4 at execution. The physical base address of the AC module to be loaded and authenticated is specified in EBX. The size of the module in bytes is specified in ECX. EDX controls the level of functionality supported by the measured environment launch. To enable the full functionality of the protected environment launch, EDX must be initialized to zero.

The authenticated code base address and size parameters (in bytes) are passed to the GETSEC[SENTER] instruction using EBX and ECX respectively. The ILP evaluates the contents of these registers according to the rules for the AC module address in GETSEC[ENTERACCS]. AC module execution follows the same rules, as set by GETSEC[ENTERACCS].

The launching software must ensure that the TPM.ACCESS_0.activeLocality bit is clear before executing the GETSEC[SENTER] instruction.

There are restrictions enforced by the processor for execution of the GETSEC[SENTER] instruction:

- Execution is not allowed unless the processor is in protected mode or IA-32e mode with CPL = 0 and EFLAGS.VM = 0.
- Processor cache must be available and not disabled using the CR0.CD and NW bits.
- For enforcing consistency of operation with numeric exception reporting using Interrupt 16, CR0.NE must be set.
- An Intel TXT-capable chipset must be present as communicated to the processor by sampling of the power-on configuration capability field after reset.
- The processor can not be in authenticated code execution mode or already in a measured environment (as launched by a previous GETSEC[ENTERACCS] or GETSEC[SENTER] instruction).
- To avoid potential operability conflicts between modes, the processor is not allowed to execute this instruction if it currently is in SMM or VMX operation.
To insure consistent handling of SIPI messages, the processor executing the GETSEC[SENTER] instruction must also be designated the BSP (boot-strap processor) as defined by A32_APIC_BASE.BSP (Bit 8).

EDX must be initialized to a setting supportable by the processor. Unless enumeration by the GETSEC[PARAMETERS] leaf reports otherwise, only a value of zero is supported.

Failure to abide by the above conditions results in the processor signaling a general protection violation.

This instruction leaf starts the launch of a measured environment by initiating a rendezvous sequence for all logical processors in the platform. The rendezvous sequence involves the initiating logical processor sending a message (by executing GETSEC[SENTER]) and other responding logical processors (RLPs) acknowledging the message, thus synchronizing the RLP(s) with the ILP.

In response to a message signaling the completion of rendezvous, RLPs clear the bootstrap processor indicator flag (IA32_APIC_BASE.BSP) and enter an SENTER sleep state. In this sleep state, RLPs enter an idle processor condition while waiting to be activated after a measured environment has been established by the system executive. RLPs in the SENTER sleep state can only be activated by the GETSEC leaf function WAKEUP in a measured environment.

A successful launch of the measured environment results in the initiating logical processor entering the authenticated code execution mode. Prior to reaching this point, the ILP performs the following steps internally:

- Inhibit processor response to the external events: INIT, A20M, NMI, and SMI.
- Establish and check the location and size of the authenticated code module to be executed by the ILP.
- Check for the existence of an Intel® TXT-capable chipset.
- Verify the current power management configuration is acceptable.
- Broadcast a message to enable protection of memory and I/O from activities from other processor agents.
- Load the designated AC module into authenticated code execution area.
- Isolate the content of authenticated code execution area from further state modification by external agents.
- Authenticate the AC module.
- Updated the Trusted Platform Module (TPM) with the authenticated code module's hash.
- Initialize processor state based on the authenticated code module header information.
- Unlock the Intel® TXT-capable chipset private configuration register space and TPM locality 3 space.
- Begin execution in the authenticated code module at the defined entry point.
As an integrity check for proper processor hardware operation, execution of GETSEC[SENTER] will also check the contents of all the machine check status registers (as reported by the MSRs IA32_MCI_STATUS) for any valid uncorrectable error condition. In addition, the global machine check status register IA32_MCG_STATUS MCIP bit must be cleared and the IERR processor package pin (or its equivalent) must be not asserted, indicating that no machine check exception processing is currently in-progress. These checks are performed twice: once by the ILP prior to the broadcast of the rendezvous message to RLPs, and later in response to RLPs acknowledging the rendezvous message. Any outstanding valid uncorrectable machine check error condition present in the machine check status registers at the first check point will result in the ILP signaling a general protection violation. If an outstanding valid uncorrectable machine check error condition is present at the second check point, then this will result in the corresponding logical processor signaling the more severe TXT-shutdown condition with an error code of 12.

Before loading and authentication of the target code module is performed, the processor also checks that the current voltage and bus ratio encodings correspond to known good values supportable by the processor. The MSR IA32_PERF_STATUS values are compared against either the processor supported maximum operating target setting, system reset setting, or the thermal monitor operating target. If the current settings do not meet any of these criteria then the SENTER function will attempt to change the voltage and bus ratio select controls in a processor-specific manner. This adjustment may be to the thermal monitor, minimum (if different), or maximum operating target depending on the processor.

This implies that some thermal operating target parameters configured by BIOS may be overridden by SENTER. The measured environment software may need to take responsibility for restoring such settings that are deemed to be safe, but not necessarily recognized by SENTER. If an adjustment is not possible when an out of range setting is discovered, then the processor will abort the measured launch. This may be the case for chipset controlled settings of these values or if the controllability is not enabled on the processor. In this case it is the responsibility of the external software to program the chipset voltage ID and/or bus ratio select settings to known good values recognized by the processor, prior to executing SENTER.

**NOTE**

For a mobile processor, an adjustment can be made according to the thermal monitor operating target. For a quad-core processor the SENTER adjustment mechanism may result in a more conservative but non-uniform voltage setting, depending on the pre-SENTER settings per core.

The ILP and RLPs mask the response to the assertion of the external signals INIT#, A20M, NMI#, and SMI#. The purpose of this masking control is to prevent exposure to existing external event handlers until a protected handler has been put in place to directly handle these events. Masked external pin events may be unmasked conditionally or unconditionally via the GETSEC(EXITAC), GETSEC(SEXIT), GETSEC(SMCTRL) or for specific VMX related operations such as a VM entry or the
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VMXOFF instruction (see respective GETSEC leaves and Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C for more details). The state of the A20M pin is masked and forced internally to a de-asserted state so that external assertion is not recognized. A20M masking as set by GETSEC[SENTER] is undone only after taking down the measured environment with the GETSEC[SEXIT] instruction or processor reset. INTR is masked by simply clearing the EFLAGS.IF bit. It is the responsibility of system software to control the processor response to INTR through appropriate management of EFLAGS.

To prevent other (logical) processors from interfering with the ILP operating in authenticated code execution mode, memory (excluding implicit write-back transactions) and I/O activities originating from other processor agents are blocked. This protection starts when the ILP enters into authenticated code execution mode. Only memory and I/O transactions initiated from the ILP are allowed to proceed. Exiting authenticated code execution mode is done by executing GETSEC[EXITAC]. The protection of memory and I/O activities remains in effect until the ILP executes GETSEC[EXITAC].

Once the authenticated code module has been loaded into the authenticated code execution area, it is protected against further modification from external bus snoops. There is also a requirement that the memory type for the authenticated code module address range be WB (via initialization of the MTRRs prior to execution of this instruction). If this condition is not satisfied, it is a violation of security and the processor will force a TXT system reset (after writing an error code to the chipset LT.ERROR-CODE register). This action is referred to as a Intel® TXT reset condition. It is performed when it is considered unreliable to signal an error through the conventional exception reporting mechanism.

To conform to the minimum granularity of MTRR MSRs for specifying the memory type, authenticated code RAM (ACRAM) is allocated to the processor in 4096 byte granular blocks. If an AC module size as specified in ECX is not a multiple of 4096 then the processor will allocate up to the next 4096 byte boundary for mapping as ACRAM with indeterminate data. This pad area will not be visible to the authenticated code module as external memory nor can it depend on the value of the data used to fill the pad area.

Once successful authentication has been completed by the ILP, the computed hash is stored in the TPM at PCR17 after this register is implicitly reset. PCR17 is a dedicated register for holding the computed hash of the authenticated code module loaded and subsequently executed by the GETSEC[SENTER]. As part of this process, the dynamic PCRs 18-22 are reset so they can be utilized by subsequently software for registration of code and data modules. After successful execution of SENTER, PCR17 contains the measurement of AC code and the SENTER launching parameters.

After authentication is completed successfully, the private configuration space of the Intel® TXT-capable chipset is unlocked so that the authenticated code module and measured environment software can gain access to this normally restricted chipset state. The Intel® TXT-capable chipset private configuration space can be locked later by software writing to the chipset LT.CMD.CLOSE-PRIVATE register or unconditionally using the GETSEC[SEXIT] instruction.
The SENTER leaf function also initializes some processor architecture state for the ILP from contents held in the header of the authenticated code module. Since the authenticated code module is relocatable, all address references are relative to the base address passed in via EBX. The ILP GDTR base value is initialized to EBX + [GDTBasePtr] and GDTR limit set to [GDTLimit]. The CS selector is initialized to the value held in the AC module header field SegSel, while the DS, SS, and ES selectors are initialized to CS+8. The segment descriptor fields are initialized implicitly with BASE=0, LIMIT=FFFFFh, G=1, D=1, P=1, S=1, read/write/accessed for DS, SS, and ES, while execute/read/accessed for CS. Execution in the authenticated code module for the ILP begins with the EIP set to EBX + [EntryPoint]. AC module defined fields used for initializing processor state are consistency checked with a failure resulting in an TXT-shutdown condition.

Table 5-6 provides a summary of processor state initialization for the ILP and RLP(s) after successful completion of GETSEC[SENTER]. For both ILP and RLP(s), paging is disabled upon entry to the measured environment. It is up to the ILP to establish a trusted paging environment, with appropriate mappings, to meet protection requirements established during the launch of the measured environment. RLP state initialization is not completed until a subsequent wake-up has been signaled by execution of the GETSEC[WAKEUP] function by the ILP.

Table 5-6. Register State Initialization after GETSEC[SENTER] and GETSEC[WAKEUP]

<table>
<thead>
<tr>
<th>Register State</th>
<th>ILP after GETSEC[SENTER]</th>
<th>RLP after GETSEC[WAKEUP]</th>
</tr>
</thead>
<tbody>
<tr>
<td>CR0</td>
<td>PG←0, AM←0, WP←0; Others unchanged</td>
<td>PG←0, CD←0, NW←0, AM←0, WP←0; PE←1, NE←1</td>
</tr>
<tr>
<td>CR4</td>
<td>00004000H</td>
<td>00004000H</td>
</tr>
<tr>
<td>EFLAGS</td>
<td>00000002H</td>
<td>00000002H</td>
</tr>
<tr>
<td>IA32_EFER</td>
<td>0H</td>
<td>0</td>
</tr>
<tr>
<td>EIP</td>
<td>[EntryPoint from MLE header]</td>
<td>[LT.MLE.JOIN + 12]</td>
</tr>
<tr>
<td>EBX</td>
<td>Unchanged [SINIT.BASE]</td>
<td>Unchanged</td>
</tr>
<tr>
<td>EDX</td>
<td>SENTER control flags</td>
<td>Unchanged</td>
</tr>
<tr>
<td>EBP</td>
<td>SINIT.BASE</td>
<td>Unchanged</td>
</tr>
<tr>
<td>CS</td>
<td>Sel=[SINIT SegSel], base=0, limit=FFFFH, G=1, D=1, AR=9BH</td>
<td>Sel = [LT.MLE.Join + 8], base = 0, limit = FFFFFH, G = 1, D = 1, AR = 9BH</td>
</tr>
<tr>
<td>DS, ES, SS</td>
<td>Sel=[SINIT SegSel] +8, base=0, limit=FFFFH, G=1, D=1, AR=93H</td>
<td>Sel = [LT.MLE.Join + 8] +8, base = 0, limit = FFFFFH, G = 1, D = 1, AR = 93H</td>
</tr>
</tbody>
</table>
Segmentation related processor state that has not been initialized by GETSEC[SENTER] requires appropriate initialization before use. Since a new GDT context has been established, the previous state of the segment selector values held in FS, GS, TR, and LDTR may no longer be valid. The IDTR will also require reloading with a new IDT context after launching the measured environment before exceptions or the external interrupts INTR and NMI can be handled. In the meantime, the programmer must take care in not executing an INT n instruction or any other condition that would result in an exception or trap signaling.

Debug exception and trap related signaling is also disabled as part of execution of GETSEC[SENTER]. This is achieved by clearing DR7, TF in EFLAGS, and the MSR IA32_DEBUGCTL as defined in Table 5-6. These can be re-enabled once supporting exception handler(s), descriptor tables, and debug registers have been properly re-initialized following SENTER. Also, any pending single-step trap condition will be cleared at the completion of SENTER for both the ILP and RLP(s).

Performance related counters and counter control registers are cleared as part of execution of SENTER on both the ILP and RLP. This implies any active performance counters at the time of SENTER execution will be disabled. To reactive the processor performance counters, this state must be re-initialized and re-enabled.

Since MCE along with all other state bits (with the exception of SMXE) are cleared in CR4 upon execution of SENTER processing, any enabled machine check error condition that occurs will result in the processor performing the TXT-shutdown action. This also applies to an RLP while in the SENTER sleep state. For each logical processor

### Table 5-6. Register State Initialization after GETSEC[SENTER] and GETSEC[WAKEUP]

<table>
<thead>
<tr>
<th>Register</th>
<th>Base Initialization</th>
<th>Limit Initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDTR</td>
<td>SINIT.base (EBX) +  [SINIT.GDTBasePtr], Limit=[SINIT.GDTLimit]</td>
<td>[LT.MLE.JOIN + 4], Limit = [LT.MLE.JOIN]</td>
</tr>
<tr>
<td>DR7</td>
<td>00000400H</td>
<td>00000400H</td>
</tr>
<tr>
<td>IA32_DEBUGCTL</td>
<td>0H</td>
<td>0H</td>
</tr>
<tr>
<td>Performance counters and counter control registers</td>
<td>See Table 5-5</td>
<td>See Table 5-5</td>
</tr>
<tr>
<td>IA32_MISC_ENABLE</td>
<td>Bit 2←0</td>
<td>Bit 2←0</td>
</tr>
<tr>
<td>IA32_SMM_MONITOR_CTL</td>
<td>Bit 2←0</td>
<td>Bit 2←0</td>
</tr>
</tbody>
</table>

### NOTES:


See Table 5-5
CR4.MCE must be reestablished with a valid machine check exception handler to otherwise avoid an TXT-shutdown under such conditions.

The MSR IA32_EFER is also unconditionally cleared as part of the processor state initialized by SENTER for both the ILP and RLP. Since paging is disabled upon entering authenticated code execution mode, a new paging environment will have to be re-established if it is desired to enable IA-32e mode while operating in authenticated code execution mode.

The miscellaneous feature control MSR, IA32_MISC_ENABLE, is initialized as part of the measured environment launch. Certain bits of this MSR are preserved because preserving these bits may be important to maintain previously established platform settings. See the footnote for Table 5-5 The remaining bits are cleared for the purpose of establishing a more consistent environment for the execution of authenticated code modules. Among the impact of initializing this MSR, any previous condition established by the MONITOR instruction will be cleared.

**Effect of MSR IA32_FEATURE_CONTROL MSR**

Bits 15:8 of the IA32_FEATURE_CONTROL MSR affect the execution of GETSEC(SENDER). These bits consist of two fields:

- Bit 15: a global enable control for execution of SENTER.
- Bits 14:8: a parameter control field providing the ability to qualify SENTER execution based on the level of functionality specified with corresponding EDX parameter bits 6:0.

The layout of these fields in the IA32_FEATURE_CONTROL MSR is shown in Table 5-1.

Prior to the execution of GETSEC(SENDER), the lock bit of IA32_FEATURE_CONTROL MSR must be bit set to affirm the settings to be used. Once the lock bit is set, only a power-up reset condition will clear this MSR. The IA32_FEATURE_CONTROL MSR must be configured in accordance to the intended usage at platform initialization. Note that this MSR is only available on SMX or VMX enabled processors. Otherwise, IA32_FEATURE_CONTROL is treated as reserved.

The *Intel® Trusted Execution Technology Measured Launched Environment Programming Guide* provides additional details and requirements for programming measured environment software to launch in an Intel TXT platform.

**Operation in a Uni-Processor Platform**

(* The state of the internal flag ACMODEFLAG and SENTERFLAG persist across instruction boundary *)

GETSEC(SENDER) (ILP only):

IF (CR4.SMXE=0)
    THEN #UD;
ELSE IF (in VMX non-root operation)
    THEN VM Exit (reason="GETSEC instruction");
ELSE IF (GETSEC leaf unsupported)
    THEN #UD;

GETSEC(SENDER)—Enter a Measured Environment
ELSE IF ((in VMX root operation) or (CR0.PE=0) or (CR0.CD=1) or (CR0.NW=1) or (CR0.NE=0) or (CPL>0) or (EFLAGS.VM=1) or (IA32_APIC_BASE.BSP=0) or (TXT chipset not present) or (SENTERFLAG=1) or (IN_SMM=1) or (TPM interface is not present) or (EDX != (SENTER_EDX_support_mask & EDX)) or (IA32_CR_FEATURE_CONTROL[0]=0) or (IA32_CR_FEATURE_CONTROL[15]=0) or ((IA32_CR_FEATURE_CONTROL[14:8] & EDX[6:0]) != EDX[6:0])) THEN #GP(0);

IF (GETSEC[PARAMETERS].Parameter_Type = 5, MCA_Handling (bit 6) = 0) FOR I = 0 to IA32_MCG_CAP.COUNT-1 DO
  IF IA32_MC[I]_STATUS = uncorrectable error THEN #GP(0);
FD;
OD;
FD;
IF (IA32_MCG_STATUS.MCIP=1) or (IERR pin is asserted) THEN #GP(0);
ACBASE← EBX;
ACSIZE← ECX;
IF (((ACBASE MOD 4096) != 0) or ((ACSIZE MOD 64) != 0 ) or (ACSIZE < minimum module size) or (ACSIZE > AC RAM capacity) or ((ACBASE+ACSIZE) > (2^32 -1))) THEN #GP(0);
Mask SMI, INIT, A20M, and NMI external pin events;
SignalTXTMsg(SENTER);
DO WHILE (no SignalSENTER message);

TXT_SENTER__MSG_EVENT (ILP & RLP):
Mask and clear SignalSENTER event;
Unmask SignalSEXIT event;
IF (in VMX operation)
  THEN TXT-SHUTDOWN(#IllegalEvent);
FOR I = 0 to IA32_MCG_CAP.COUNT-1 DO
  IF IA32_MC[I]_STATUS = uncorrectable error
    THEN TXT-SHUTDOWN(#UnrecovMCError);
FD;
OD;
IF (IA32_MCG_STATUS.MCIP=1) or (IERR pin is asserted)
  THEN TXT-SHUTDOWN(#UnrecovMCError);
IF (Voltage or bus ratio status are NOT at a known good state)
  THEN IF (Voltage select and bus ratio are internally adjustable)
THEN
  Make product-specific adjustment on operating parameters;
ELSE
  TXT-SHUTDOWN(#IllegalVIDBRatio);
FI;

IA32_MISC_ENABLE ← (IA32_MISC_ENABLE & MASK_CONST*)
(* The hexadecimal value of MASK_CONST may vary due to processor implementations *)
A20M ← 0;
IA32_DEBUGCTL ← 0;
Invalidate processor TLB(s);
Drain outgoing transactions;
Clear performance monitor counters and control;
SENDERFLAG ← 1;
SignalTXTMsg(SENTERAck);
IF (logical processor is not ILP)
   THEN GOTO RLP_SENTER_ROUTINE;
(* ILP waits for all logical processors to ACK *)
DO
  DONE ← TXT.READ(LT_STS);
  WHILE (not DONE);
  SignalTXTMsg(SENTERContinue);
  SignalTXTMsg(ProcessorHold);
  FOR I=ACBASE to ACBASE+ACSIZE-1 DO
    ACRAM[I-ACBASE].ADDR ← I;
    ACRAM[I-ACBASE].DATA ← LOAD(I);
  OD;
  IF (ACRAM memory type != WB)
     THEN TXT-SHUTDOWN(#BadACMMType);
  IF (AC module header version is not supported) OR (ACRAM[ModuleType] <> 2)
     THEN TXT-SHUTDOWN(#UnsupportedACM);
  KEY ← GETKEY(ACRAM, ACBASE);
  KEYHASH ← HASH(KEY);
  CSKEYHASH ← LT.READ(LT_Public.KEY);
  IF (KEYHASH <> CSKEYHASH)
     THEN TXT-SHUTDOWN(#AuthenticateFail);
  SIGNATURE ← DECRYPT(ACRAM, ACBASE, KEY);
  (* The value of SIGNATURE_LEN_CONST is implementation-specific *)
  FOR I=0 to SIGNATURE_LEN_CONST - 1 DO
    ACRAM[SCRATCH.I] ← SIGNATURE[I];
    COMPUTEDSIGNATURE ← HASH(ACRAM, ACBASE, ACSIZE);
  FOR I=0 to SIGNATURE_LEN_CONST - 1 DO
    ACRAM[SCRATCH.SIGNATURE_LEN_CONST+I] ← COMPUTEDSIGNATURE[I];
IF (SIGNATURE != COMPUTEDSIGNATURE)
    THEN TXT-SHUTDOWN(#AuthenticateFail);
ACMCONTROL ← ACRAM[CodeControl];
IF ((ACMCONTROL.0 = 0) and (ACMCONTROL.1 = 1) and (snoop hit to modified line detected on
ACRAM load))
    THEN TXT-SHUTDOWN(#UnexpectedHITM);
IF (ACMCONTROL reserved bits are set)
    THEN TXT-SHUTDOWN(#BadACMFormat);
IF ((ACRAM[GDTBasePtr] < (ACRAM[HeaderLen] * 4 + Scratch_size)) OR
    ((ACRAM[GDTBasePtr] + ACRAM[GDTLimit]) >= ACSIZE))
    THEN TXT-SHUTDOWN(#BadACMFormat);
IF ((ACMCONTROL.0 = 1) and (ACMCONTROL.1 = 1) and (snoop hit to modified
    line detected on ACRAM load))
    THEN ACEntryPoint ← ACBASE+ACRAM[ErrorEntryPoint];
ELSE
    ACEntryPoint ← ACBASE+ACRAM[EntryPoint];
IF ((ACEntryPoint >= ACSIZE) or (ACEntryPoint < (ACRAM[HeaderLen] * 4 + Scratch_size)))
    THEN TXT-SHUTDOWN(#BadACMFormat);
IF ((ACRAM[SegSel] > (ACRAM[GDTLimit] - 15)) or (ACRAM[SegSel] < 8))
    THEN TXT-SHUTDOWN(#BadACMFormat);
ACRAM[SCRATCH.SIGNATURE_LEN_CONST] ← EDX;
WRITE(TPM.HASH.START) ← 0;
FOR I=0 to SIGNATURE_LEN_CONST + 3 DO
    WRITE(TPM.HASH.DATA) ← ACRAM[SCRATCH.I];
WRITE(TPM.HASH.END) ← 0;
ACMODEFLAG ← 1;
CR0.[PG.AM.WP] ← 0;
CR4 ← 00004000h;
EFLAGS ← 00000002h;
IA32_EFER ← 0;
EBP ← ACBASE;
GDTR.BASE ← ACBASE+ACRAM[GDTBasePtr];
GDTR.LIMIT ← ACRAM[GDTLimit];
CS.SEL ← ACRAM[SegSel];
CS.BASE ← 0;
CS.LIMIT ← $FFFF$;
CS.G ← 1;
CS.D ← 1;
CS.AR ← 9Bh;
DS.SEL ← ACRAM[SegSel]+8;
DS.BASE ← 0;
DS.LIMIT ← $FFFF$;
DS.G ← 1;
DS.D ← 1;
DS.AR ← 93h;
SS ← DS;
ES ← DS;
DR7 ← 00000400h;
IA32_DEBUGCTL ← 0;
SignalTXTMsg(UnlockSMRAM);
SignalTXTMsg(OpenPrivate);
SignalTXTMsg(OpenLocality3);
EIP ← AEntryPoint;
END;

**RLP_SENTER_ROUTINE:** (RLP only)

Mask SMI, INIT, A20M, and NMI external pin events
Unmask SignalWAKEUP event;
Wait for SignalSENTERContinue message;
IA32_APIC_BASE.BSP ← 0;
GOTO SENTER sleep state;
END;

**Flags Affected**

All flags are cleared.

**Use of Prefixes**

<table>
<thead>
<tr>
<th>Prefix</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOCK</td>
<td>Causes #UD</td>
</tr>
<tr>
<td>REP</td>
<td>Cause #UD (includes REPNE/REPNZ and REP/REPE/REPE)</td>
</tr>
<tr>
<td></td>
<td>Causes #UD</td>
</tr>
<tr>
<td></td>
<td>Ignored</td>
</tr>
<tr>
<td></td>
<td>Ignored</td>
</tr>
<tr>
<td></td>
<td>Ignored</td>
</tr>
</tbody>
</table>

**Protected Mode Exceptions**

- **#UD**
  - If CR4.SMXE = 0.
  - If GETSEC[SENTER] is not reported as supported by GETSEC[CAPABILITIES].

- **#GP(0)**
  - If CR0.CD = 1 or CR0.NW = 1 or CR0.NE = 0 or CR0.PE = 0 or CPL > 0 or EFLAGS.VM = 1.
  - If in VMX root operation.
  - If the initiating processor is not designated as the bootstrap processor via the MSR bit IA32_APIC_BASE.BSP.
SAFER MODE EXTENSIONS REFERENCE

If an Intel® TXT-capable chipset is not present.
If an Intel® TXT-capable chipset interface to TPM is not detected as present.
If a protected partition is already active or the processor is already in authenticated code mode.
If the processor is in SMM.
If a valid uncorrectable machine check error is logged in IA32_MC[1]_STATUS.
If the authenticated code base is not on a 4096 byte boundary.
If the authenticated code size > processor's authenticated code execution area storage capacity.
If the authenticated code size is not modulo 64.

Real-Address Mode Exceptions
#UD If CR4.SMXE = 0.
    If GETSEC[SENTER] is not reported as supported by GETSEC[CAPABILITIES].
#GP(0) GETSEC[SENTER] is not recognized in real-address mode.

Virtual-8086 Mode Exceptions
#UD If CR4.SMXE = 0.
    If GETSEC[SENTER] is not reported as supported by GETSEC[CAPABILITIES].
#GP(0) GETSEC[SENTER] is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
All protected mode exceptions apply.
#GP IF AC code module does not reside in physical address below $2^{32} -1$.

64-Bit Mode Exceptions
All protected mode exceptions apply.
#GP IF AC code module does not reside in physical address below $2^{32} -1$.

VM-Exit Condition
Reason (GETSEC) IF in VMX non-root operation.
GETSEC[SEXIT]—Exit Measured Environment

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 37</td>
<td>GETSEC[SEXIT]</td>
<td>Exit measured environment</td>
</tr>
<tr>
<td>(EAX=5)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Description

The GETSEC[SEXIT] instruction initiates an exit of a measured environment established by GETSEC[SENTER]. The SEXIT leaf of GETSEC is selected with EAX set to 5 at execution. This instruction leaf sends a message to all logical processors in the platform to signal the measured environment exit.

There are restrictions enforced by the processor for the execution of the GETSEC[SEXIT] instruction:

- Execution is not allowed unless the processor is in protected mode (CR0.PE = 1) with CPL = 0 and EFLAGS.VM = 0.
- The processor must be in a measured environment as launched by a previous GETSEC[SENTER] instruction, but not still in authenticated code execution mode.
- To avoid potential inter-operability conflicts between modes, the processor is not allowed to execute this instruction if it currently is in SMM or in VMX operation.
- To insure consistent handling of SIPI messages, the processor executing the GETSEC[SEXIT] instruction must also be designated the BSP (bootstrap processor) as defined by the register bit IA32_APIC_BASE.BSP (bit 8).

Failure to abide by the above conditions results in the processor signaling a general protection violation.

This instruction initiates a sequence to rendezvous the RLPs with the ILP. It then clears the internal processor flag indicating the processor is operating in a measured environment.

In response to a message signaling the completion of rendezvous, all RLPs restart execution with the instruction that was to be executed at the time GETSEC[SEXIT] was recognized. This applies to all processor conditions, with the following exceptions:

- If an RLP executed HLT and was in this halt state at the time of the message initiated by GETSEC[SEXIT], then execution resumes in the halt state.
- If an RLP was executing MWAIT, then a message initiated by GETSEC[SEXIT] causes an exit of the MWAIT state, falling through to the next instruction.
- If an RLP was executing an intermediate iteration of a string instruction, then the processor resumes execution of the string instruction at the point which the message initiated by GETSEC[SEXIT] was recognized.
- If an RLP is still in the SENTER sleep state (never awakened with GETSEC[WAKEUP]), it will be sent to the wait-for-SIPI state after first clearing...
the bootstrap processor indicator flag (IA32_APIC_BASE.BSP) and any pending
SIPI state. In this case, such RLPs are initialized to an architectural state
consistent with having taken a soft reset using the INIT# pin.

Prior to completion of the GETSEC[SEXIT] operation, both the ILP and any active
RLPs unmask the response of the external event signals INIT#, A20M, NMI#, and
SMI#. This unmasking is performed unconditionally to recognize pin events which
are masked after a GETSEC[SENTER]. The state of A20M is unmasked, as the A20M
pin is not recognized while the measured environment is active.

On a successful exit of the measured environment, the ILP re-locks the Intel® TXT-
capable chipset private configuration space. GETSEC[SEXIT] does not affect the
content of any PCR.

At completion of GETSEC[SEXIT] by the ILP, execution proceeds to the next instruc-
tion. Since EFLAGS and the debug register state are not modified by this instruction,
a pending trap condition is free to be signaled if previously enabled.

**Operation in a Uni-Processor Platform**

(* The state of the internal flag ACMODEFLAG and SENTERFLAG persist across instruction
boundary *)

**GETSEC[SEXIT] (ILP only):**

IF (CR4.SMXE=0)
  THEN #UD;
ELSE IF (in VMX non-root operation)
  THEN VM Exit (reason="GETSEC instruction");
ELSE IF (GETSEC leaf unsupported)
  THEN #UD;
ELSE IF (in VMX root operation) or
  (CPL>0) or (EFLAGS.VM=1) or
  (IA32_APIC_BASE.BSP=0) or
  (TXT chipset not present) or
  (SENTERFLAG=0) or (ACMODEFLAG=1) or (IN_SMM=1)
  THEN #GP(0);
SignalTXTMsg(SEXIT);
DO
  WHILE (no SignalSEXIT message);

**TXT_SEXIT_MSG_EVENT (ILP & RLP):**

Mask and clear SignalSEXIT event;
Clear MONITOR FSM;
Unmask SignalSENTER event;
IF (in VMX operation)
  THEN TXT-SHUTDOWN(#IllegalEvent);
SignalTXTMsg(SEXITAck);
IF (logical processor is not ILP)
THEN GOTO RLP_SEXIT_ROUTINE;
(* ILP waits for all logical processors to ACK *)
DO
  DONE ← READ(LT.STS);
  WHILE (NOT DONE);
  SignalTXTMsg(SEXITContinue);
  SignalTXTMsg(ClosePrivate);
  SENTERFLAG ← 0;
Unmask SMI, INIT, A20M, and NMI external pin events;
END;

RLP_SEXIT_ROUTINE (RLPs only):
Wait for SignalSEXITContinue message;
Unmask SMI, INIT, A20M, and NMI external pin events;
IF (prior execution state = HLT)
  THEN reenter HLT state;
IF (prior execution state = SENTER sleep)
  THEN
    IA32_APIC_BASE.BSP ← 0;
    Clear pending SIPI state;
    Call INIT_PROCESSOR_STATE;
    Unmask SIPI event;
    GOTO WAIT-FOR-SIPI;
FI;
END;

Flags Affected
ILP: None.
RLPs: all flags are modified for an RLP, returning to wait-for-SIPI state, none otherwise

Use of Prefixes
LOCK Causes #UD
REP* Cause #UD (includes REPNE/REPNZ and REP/REPE/REPZ)
Operand size Causes #UD
Segment overrides Ignored
Address size Ignored
REX Ignored

Protected Mode Exceptions
#UD If CR4.SMXE = 0.
SAFER MODE EXTENSIONS REFERENCE

If GETSEC[SEXIT] is not reported as supported by GETSEC[CAPABILITIES].

#GP(0) If CR0.PE = 0 or CPL > 0 or EFLAGS.VM = 1.
If in VMX root operation.
If the initiating processor is not designated as the via the MSR bit IA32_APIC_BASE.BSP.
If an Intel® TXT-capable chipset is not present.
If a protected partition is not already active or the processor is already in authenticated code mode.
If the processor is in SMM.

Real-Address Mode Exceptions

#UD If CR4.SMXE = 0.
If GETSEC[SEXIT] is not reported as supported by GETSEC[CAPABILITIES].

#GP(0) GETSEC[SEXIT] is not recognized in real-address mode.

Virtual-8086 Mode Exceptions

#UD If CR4.SMXE = 0.
If GETSEC[SEXIT] is not reported as supported by GETSEC[CAPABILITIES].

#GP(0) GETSEC[SEXIT] is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
All protected mode exceptions apply.

64-Bit Mode Exceptions
All protected mode exceptions apply.

VM-Exit Condition
Reason (GETSEC) IF in VMX non-root operation.
GETSEC[PARAMETERS]—Report the SMX Parameters

Table 5-7 defines the parameter types supported in current and future implementations.

<table>
<thead>
<tr>
<th>Parameter Type EAX[4:0]</th>
<th>Parameter Description</th>
<th>EAX[31:5]</th>
<th>EBX[31:0]</th>
<th>ECX[31:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>NULL</td>
<td>Reserved (0 returned)</td>
<td>Reserved (unmodified)</td>
<td>Reserved (unmodified)</td>
</tr>
<tr>
<td>1</td>
<td>Supported AC module versions</td>
<td>Reserved (0 returned)</td>
<td>version comparison mask</td>
<td>version numbers supported</td>
</tr>
<tr>
<td>2</td>
<td>Max size of authenticated code execution area</td>
<td>Multiply by 32 for size in bytes</td>
<td>Reserved (unmodified)</td>
<td>Reserved (unmodified)</td>
</tr>
<tr>
<td>3</td>
<td>External memory types supported during AC mode</td>
<td>Memory type bit mask</td>
<td>Reserved (unmodified)</td>
<td>Reserved (unmodified)</td>
</tr>
</tbody>
</table>
Table 5-7. SMX Reporting Parameters Format (Contd.)

<table>
<thead>
<tr>
<th>Parameter Type EAX[4:0]</th>
<th>Parameter Description</th>
<th>EAX[31:5]</th>
<th>EBX[31:0]</th>
<th>ECX[31:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Selective SENTER functionality control</td>
<td>EAX[14:8] correspond to available SENTER function disable controls</td>
<td>Reserved (unmodified)</td>
<td>Reserved (unmodified)</td>
</tr>
<tr>
<td>5</td>
<td>TXT extensions support</td>
<td>TXT Feature Extensions Flags (see Table 5-8)</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>6-31</td>
<td>Undefined</td>
<td>Reserved (unmodified)</td>
<td>Reserved (unmodified)</td>
<td>Reserved (unmodified)</td>
</tr>
</tbody>
</table>

Table 5-8. TXT Feature Extensions Flags

<table>
<thead>
<tr>
<th>Bit</th>
<th>Definition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Processor based S-CRTM support</td>
<td>Returns 1 if this processor implements a processor-rooted S-CRTM capability and 0 if not (S-CRTM is rooted in BIOS). This flag cannot be used to infer whether the chipset supports TXT or whether the processor support SMX.</td>
</tr>
<tr>
<td>6</td>
<td>Machine Check Handling</td>
<td>Returns 1 if it machine check status registers can be preserved through ENTERACCS and SENTER. If this bit is 1, the caller of ENTERACCS and SENTER is not required to clear machine check error status bits before invoking these GETSEC leaves. If this bit returns 0, the caller of ENTERACCS and SENTER must clear all machine check error status bits before invoking these GETSEC leaves.</td>
</tr>
<tr>
<td>31:7</td>
<td>Reserved</td>
<td>Reserved for future use. Will return 0.</td>
</tr>
</tbody>
</table>

Supported AC module versions (as defined by the AC module HeaderVersion field) can be determined for a particular SMX capable processor by the type 1 parameter. Using EBX to index through the available parameters reported by GETSEC[PARAMETERS] for each unique parameter set returned for type 1, software can determine the complete list of AC module version(s) supported.
For each parameter set, EBX returns the comparison mask and ECX returns the available HeaderVersion field values supported, after AND’ing the target HeaderVersion with the comparison mask. Software can then determine if a particular AC module version is supported by following the pseudo-code search routine given below:

```
parameter_search_index= 0
do {
    EBX= parameter_search_index++
    EAX= 6
    GETSEC
    if (EAX[4:0] = 1) {
        if ((version_query & EBX) = ECX) {
            version_is_supported= 1
            break
        }
    }
} while (EAX[4:0]!= 0)
```

If only AC modules with a HeaderVersion of 0 are supported by the processor, then only one parameter set of type 1 will be returned, as follows: EAX = 00000001H, EBX = FFFFFFFFH and ECX = 00000000H.

The maximum capacity for an authenticated code execution area supported by the processor is reported with the parameter type of 2. The maximum supported size in bytes is determined by multiplying the returned size in EAX[31:5] by 32. Thus, for a maximum supported authenticated RAM size of 32KBytes, EAX returns with 00008002H.

Supportable memory types for memory mapped outside of the authenticated code execution area are reported with the parameter type of 3. While is active, as initiated by the GETSEC functions SENTER and ENTERACCS and terminated by EXITAC, there are restrictions on what memory types are allowed for the rest of system memory. It is the responsibility of the system software to initialize the memory type range register (MTRR) MSRs and/or the page attribute table (PAT) to only map memory types consistent with the reporting of this parameter. The reporting of supportable memory types of external memory is indicated using a bit map returned in EAX[31:8]. These bit positions correspond to the memory type encodings defined for the MTRR MSR and PAT programming. See Table 5-9.

The parameter type of 4 is used for enumerating the availability of selective GETSEC[SENTER] function disable controls. If a 1 is reported in bits 14:8 of the returned parameter EAX, then this indicates a disable control capability exists with SENTER for a particular function. The enumerated field in bits 14:8 corresponds to use of the EDX input parameter bits 6:0 for SENTER. If an enumerated field bit is set to 1, then the corresponding EDX input parameter bit of EDX may be set to 1 to disable that designated function. If the enumerated field bit is 0 or this parameter is not reported, then no disable capability exists with the corresponding EDX input parameter for SENTER, and EDX bit(s) must be cleared to 0 to enable execution of...
SAFER MODE EXTENSIONS REFERENCE

SENTER. If no selective disable capability for SENTER exists as enumerated, then the corresponding bits in the IA32_FEATURE_CONTROL MSR bits 14:8 must also be programmed to 1 if the SENTER global enable bit 15 of the MSR is set. This is required to enable future extensibility of SENTER selective disable capability with respect to potentially separate software initialization of the MSR.

Table 5-9. External Memory Types Using Parameter 3

<table>
<thead>
<tr>
<th>EAX Bit Position</th>
<th>Parameter Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>Uncacheable (UC)</td>
</tr>
<tr>
<td>9</td>
<td>Write Combining (WC)</td>
</tr>
<tr>
<td>11:10</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>Write-through (WT)</td>
</tr>
<tr>
<td>13</td>
<td>Write-protected (WP)</td>
</tr>
<tr>
<td>14</td>
<td>Write-back (WB)</td>
</tr>
<tr>
<td>31:15</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Table 5-10. Default Parameter Values

<table>
<thead>
<tr>
<th>Parameter Type EAX[4:0]</th>
<th>Default Setting</th>
<th>Parameter Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.0 only</td>
<td>Supported AC module versions</td>
</tr>
<tr>
<td>2</td>
<td>32 KBytes</td>
<td>Authenticated code execution area size</td>
</tr>
<tr>
<td>3</td>
<td>UC only</td>
<td>External memory types supported during AC execution mode</td>
</tr>
<tr>
<td>4</td>
<td>None</td>
<td>Available SENTER selective disable controls</td>
</tr>
</tbody>
</table>

Operation

(* example of a processor supporting only a 0.0 HeaderVersion, 32K ACRAM size, memory types UC and WC *)

IF (CR4.SMXE=0)
    THEN #UD;
ELSE IF (in VMX non-root operation)
THEN VM Exit (reason="GETSEC instruction");
ELSE IF (GETSEC leaf unsupported)
    THEN #UD;
    (* example of a processor supporting a 0.0 HeaderVersion *)
IF (EBX=0) THEN
    EAX← 00000001h;
    EBX← FFFFFFFFh;
    ECX← 00000000h;
ELSE IF (EBX=1)
    (* example of a processor supporting a 32K ACRAM size *)
    THEN EAX← 00008002h;
ELSE IF (EBX= 2)
    (* example of a processor supporting external memory types of UC and WC *)
    THEN EAX← 0000303h;
ELSE IF (EBX= other value(s) less than unsupported index value)
    (* EAX value varies. Consult Table 5-7 and Table 5-8*)
    ELSE (* unsupported index*)
    EAX ← 00000000h;
END;

Flags Affected
None.

Use of Prefixes
LOCK Causes #UD
REP* Cause #UD (includes REPNE/REPNZ and REP/REPE/REPZ)
Operand size Causes #UD
Segment overrides Ignored
Address size Ignored
REX Ignored

Protected Mode Exceptions
#UD If CR4.SMXE = 0.
    If GETSEC[PARAMETERS] is not reported as supported by GETSEC[CAPABILITIES].

Real-Address Mode Exceptions
#UD If CR4.SMXE = 0.
    If GETSEC[PARAMETERS] is not reported as supported by GETSEC[CAPABILITIES].

GETSEC[PARAMETERS]—Report the SMX Parameters
SAFER MODE EXTENSIONS REFERENCE

Virtual-8086 Mode Exceptions

#UD If CR4.SMXE = 0.
If GETSEC[PARAMETERS] is not reported as supported by
GETSEC[CAPABILITIES].

Compatibility Mode Exceptions
All protected mode exceptions apply.

64-Bit Mode Exceptions
All protected mode exceptions apply.

VM-Exit Condition
Reason (GETSEC) IF in VMX non-root operation.
GETSEC[SMCTRL]—SMX Mode Control

Description

The GETSEC[SMCTRL] instruction is available for performing certain SMX specific mode control operations. The operation to be performed is selected through the input register EBX. Currently only an input value in EBX of 0 is supported. All other EBX settings will result in the signaling of a general protection violation.

If EBX is set to 0, then the SMCTRL leaf is used to re-enable SMI events. SMI is masked by the ILP executing the GETSEC[SENTER] instruction (SMI is also masked in the responding logical processors in response to SENTER rendezvous messages.). The determination of when this instruction is allowed and the events that are unmasked is dependent on the processor context (See Table 5-11). For brevity, the usage of SMCTRL where EBX=0 will be referred to as GETSEC[SMCTRL(0)].

As part of support for launching a measured environment, the SMI, NMI and INIT events are masked after GETSEC[SENTER], and remain masked after exiting authenticated execution mode. Unmasking these events should be accompanied by securely enabling these event handlers. These security concerns can be addressed in VMX operation by a MVMM.

The VM monitor can choose two approaches:

• In a dual monitor approach, the executive software will set up an SMM monitor in parallel to the executive VMM (i.e. the MVMM), see Chapter 29, "System Management Mode" of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3C. The SMM monitor is dedicated to handling SMI events without compromising the security of the MVMM. This usage model of handling SMI while a measured environment is active does not require the use of GETSEC[SMCTRL(0)] as event re-enabling after the VMX environment launch is handled implicitly and through separate VMX based controls.

• If a dedicated SMM monitor will not be established and SMIs are to be handled within the measured environment, then GETSEC[SMCTRL(0)] can be used by the executive software to re-enable SMI that has been masked as a result of SENTER.

Table 5-11 defines the processor context in which GETSEC[SMCTRL(0)] can be used and which events will be unmasked. Note that the events that are unmasked are dependent upon the currently operating processor context.
Table 5-11. Supported Actions for GETSEC[SMCTRL(0)]

<table>
<thead>
<tr>
<th>ILP Mode of Operation</th>
<th>SMCTRL execution action</th>
</tr>
</thead>
<tbody>
<tr>
<td>In VMX non-root operation</td>
<td>VM exit</td>
</tr>
<tr>
<td>SENTERFLAG = 0</td>
<td>#GP(0), illegal context</td>
</tr>
<tr>
<td>In authenticated code execution mode (ACMODEFLAG = 1)</td>
<td>#GP(0), illegal context</td>
</tr>
<tr>
<td>SENTERFLAG = 1, not in VMX operation, not in SMM</td>
<td>Unmask SMI</td>
</tr>
<tr>
<td>SENTERFLAG = 1, in VMX root operation, not in SMM</td>
<td>Unmask SMI if SMM monitor is not configured, otherwise #GP(0)</td>
</tr>
<tr>
<td>SENTERFLAG = 1, In VMX root operation, in SMM</td>
<td>#GP(0), illegal context</td>
</tr>
</tbody>
</table>

**Operation**

(* The state of the internal flag ACMODEFLAG and SENTERFLAG persist across instruction boundary *)

If (CR4.SMXE=0)

THEN #UD;

ELSE if (in VMX non-root operation)

THEN VM Exit (reason="GETSEC instruction");

ELSE if (GETSEC leaf unsupported)

THEN #UD;

ELSE if ((CR0.PE=0) or (CPL>0) OR (EFLAGS.VM=1))

THEN #GP(0);

ELSE if (EBX=0) and (SENTERFLAG=1) and (ACMODEFLAG=0) and (IN_SMM=0) and

(((in VMX root operation) and (SMM monitor not configured)) or (not in VMX operation))

THEN unmask SMI;

ELSE

#GP(0);

END

**Flags Affected**

None.

**Use of Prefixes**

LOCK Causes #UD

#SMCTRL — SMX Mode Control
REP*                     Cause #UD (includes REPNE/REPNZ and REP/REPE/REPZ)
Operand size             Causes #UD
Segment overrides        Ignored
Address size             Ignored
REX                      Ignored

Protected Mode Exceptions
#UD                      If CR4.SMXE = 0.
                        If GETSEC[SMCTRL] is not reported as supported by
                        GETSEC[CAPABILITIES].
#GP(0)                   If CR0.PE = 0 or CPL > 0 or EFLAGS.VM = 1.
                        If in VMX root operation.
                        If a protected partition is not already active or the processor is
                        currently in authenticated code mode.
                        If the processor is in SMM.
                        If the SMM monitor is not configured

Real-Address Mode Exceptions
#UD                      If CR4.SMXE = 0.
                        If GETSEC[SMCTRL] is not reported as supported by
                        GETSEC[CAPABILITIES].
#GP(0)                   GETSEC[SMCTRL] is not recognized in real-address mode.

Virtual-8086 Mode Exceptions
#UD                      If CR4.SMXE = 0.
                        If GETSEC[SMCTRL] is not reported as supported by
                        GETSEC[CAPABILITIES].
#GP(0)                   GETSEC[SMCTRL] is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
All protected mode exceptions apply.

64-Bit Mode Exceptions
All protected mode exceptions apply.

VM-exit Condition
Reason (GETSEC)        IF in VMX non-root operation.
GETSEC[WAKEUP]—Wake up sleeping processors in measured environment

**Description**

The GETSEC[WAKEUP] leaf function broadcasts a wake-up message to all logical processors currently in the SENTER sleep state. This GETSEC leaf must be executed only by the ILP, in order to wake-up the RLPs. Responding logical processors (RLPs) enter the SENTER sleep state after completion of the SENTER rendezvous sequence.

The GETSEC[WAKEUP] instruction may only be executed:

- In a measured environment as initiated by execution of GETSEC[SENTER].
- Outside of authenticated code execution mode.
- Execution is not allowed unless the processor is in protected mode with CPL = 0 and EFLAGS.VM = 0.
- In addition, the logical processor must be designated as the boot-strap processor as configured by setting IA32_APIC_BASE.BSP = 1.

If these conditions are not met, attempts to execute GETSEC[WAKEUP] result in a general protection violation.

An RLP exits the SENTER sleep state and start execution in response to a WAKEUP signal initiated by ILP's execution of GETSEC[WAKEUP]. The RLP retrieves a pointer to a data structure that contains information to enable execution from a defined entry point. This data structure is located using a physical address held in the Intel® TXT-capable chipset configuration register LT.MLE.JOIN. The register is publicly writable in the chipset by all processors and is not restricted by the Intel® TXT-capable chipset configuration register lock status. The format of this data structure is defined in Table 5-12.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 37</td>
<td>GETSEC[WAKEUP]</td>
<td>Wake up the responding logical processors from the SENTER sleep state.</td>
</tr>
</tbody>
</table>

**Table 5-12. RLP MVMM JOIN Data Structure**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GDT limit</td>
</tr>
<tr>
<td>4</td>
<td>GDT base pointer</td>
</tr>
<tr>
<td>8</td>
<td>Segment selector initializer</td>
</tr>
<tr>
<td>12</td>
<td>EIP</td>
</tr>
</tbody>
</table>
The MLE JOIN data structure contains the information necessary to initialize RLP processor state and permit the processor to join the measured environment. The GDTR, LIP, and CS, DS, SS, and ES selector values are initialized using this data structure. The CS selector index is derived directly from the segment selector initializer field; DS, SS, and ES selectors are initialized to CS+8. The segment descriptor fields are initialized implicitly with BASE = 0, LIMIT = FFFFFH, G = 1, D = 1, P = 1, S = 1; read/write/access for DS, SS, and ES; and execute/read/access for CS. It is the responsibility of external software to establish a GDT pointed to by the MLE JOIN data structure that contains descriptor entries consistent with the implicit settings initialized by the processor (see Table 5-6). Certain states from the content of Table 5-12 are checked for consistency by the processor prior to execution. A failure of any consistency check results in the RLP aborting entry into the protected environment and signaling an Intel® TXT shutdown condition. The specific checks performed are documented later in this section. After successful completion of processor consistency checks and subsequent initialization, RLP execution in the measured environment begins from the entry point at offset 12 (as indicated in Table 5-12).

**Operation**

(* The state of the internal flag ACMODEFLAG and SENTERFLAG persist across instruction boundary *)

IF (CR4.SMXE=0)
   THEN #UD;
ELSE IF (in VMX non-root operation)
   THEN VM Exit (reason="GETSEC instruction");
ELSE IF (GETSEC leaf unsupported)
   THEN #UD;
ELSE IF ((CR0.PE=0) or (CPL>0) or (EFLAGS.VM=1) or (SENTERFLAG=0) or (ACMODEFLAG=1) or (IN_SMM=0) or (in VMX operation) or (IA32_APIC_BASE.BSP=0) or (TXT chipset not present))
   THEN #GP(0);
ELSE
   SignalTXTMsg(WAKEUP);
END;

**RLP_SIPI_WAKEUP_FROM_SENTER_ROUTINE**: (RLP only)

WHILE (no SignalWAKEUP event);

IF (IA32_SMM_MONITOR_CTL[0] != ILP.IA32_SMM_MONITOR_CTL[0])
   THEN TXT-SHUTDOWN(#IllegalEvent)
IF (IA32_SMM_MONITOR_CTL[0] = 0)
   THEN Unmask SMI pin event;
ELSE
   Mask SMI pin event;
Mask A20M, and NMI external pin events (unmask INIT);
Mask SignalWAKEUP event;

**GETSEC[WAKEUP]**—Wake up sleeping processors in measured environment
Invalid procedure call.

Flags Affected

None.

Use of Prefixes

LOCK Causes #UD
REP* Cause #UD (includes REPNE/REPNZ and REP/REPE/REPZ)
Operand size Causes #UD
Segment overrides Ignored
Address size Ignored
REX Ignored

Protected Mode Exceptions
#UD If CR4.SMXE = 0.
   If GETSEC[WAKEUP] is not reported as supported by
   GETSEC[CAPABILITIES].
#GP(0) If CR0.PE = 0 or CPL > 0 or EFLAGS.VM = 1.
   If in VMX operation.
   If a protected partition is not already active or the processor is
   currently in authenticated code mode.
   If the processor is in SMM.
#UD If CR4.SMXE = 0.
   If GETSEC[WAKEUP] is not reported as supported by
   GETSEC[CAPABILITIES].
#GP(0) GETSEC[WAKEUP] is not recognized in real-address mode.

Virtual-8086 Mode Exceptions
#UD If CR4.SMXE = 0.
   If GETSEC[WAKEUP] is not reported as supported by
   GETSEC[CAPABILITIES].
#GP(0) GETSEC[WAKEUP] is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
All protected mode exceptions apply.

64-Bit Mode Exceptions
All protected mode exceptions apply.

VM-exit Condition
Reason (GETSEC) IF in VMX non-root operation.
Use the opcode tables in this chapter to interpret IA-32 and Intel 64 architecture object code. Instructions are divided into encoding groups:

- 1-byte, 2-byte and 3-byte opcode encodings are used to encode integer, system, MMX technology, SSE/SSE2/SSE3/SSSE3/SSE4, and VMX instructions. Maps for these instructions are given in Table A-2 through Table A-6.
- Escape opcodes (in the format: ESC character, opcode, ModR/M byte) are used for floating-point instructions. The maps for these instructions are provided in Table A-7 through Table A-22.

**NOTE**
All blanks in opcode maps are reserved and must not be used. Do not depend on the operation of undefined or blank opcodes.

### A.1 USING OPCODE TABLES

Tables in this appendix list opcodes of instructions (including required instruction prefixes, opcode extensions in associated ModR/M byte). Blank cells in the tables indicate opcodes that are reserved or undefined.

The opcode map tables are organized by hex values of the upper and lower 4 bits of an opcode byte. For 1-byte encodings (Table A-2), use the four high-order bits of an opcode to index a row of the opcode table; use the four low-order bits to index a column of the table. For 2-byte opcodes beginning with 0FH (Table A-3), skip any instruction prefixes, the 0FH byte (0FH may be preceded by 66H, F2H, or F3H) and use the upper and lower 4-bit values of the next opcode byte to index table rows and columns. Similarly, for 3-byte opcodes beginning with 0F38H or 0F3AH (Table A-4), skip any instruction prefixes, 0F38H or 0F3AH and use the upper and lower 4-bit values of the third opcode byte to index table rows and columns. See Section A.2.4, “Opcode Look-up Examples for One, Two, and Three-Byte Opcodes.”

When a ModR/M byte provides opcode extensions, this information qualifies opcode execution. For information on how an opcode extension in the ModR/M byte modifies the opcode map in Table A-2 and Table A-3, see Section A.4.

The escape (ESC) opcode tables for floating point instructions identify the eight high order bits of opcodes at the top of each page. See Section A.5. If the accompanying ModR/M byte is in the range of 00H-BFH, bits 3-5 (the top row of the third table on each page) along with the reg bits of ModR/M determine the opcode. ModR/M bytes
OPCODE MAP

outside the range of 00H-BFH are mapped by the bottom two tables on each page of the section.

A.2 KEY TO ABBREVIATIONS

Operands are identified by a two-character code of the form Zz. The first character, an uppercase letter, specifies the addressing method; the second character, a lowercase letter, specifies the type of operand.

A.2.1 Codes for Addressing Method

The following abbreviations are used to document addressing methods:

A  Direct address: the instruction has no ModR/M byte; the address of the operand is encoded in the instruction. No base register, index register, or scaling factor can be applied (for example, far JMP (EA)).

B  The VEX.vvvv field of the VEX prefix selects a general purpose register.

C  The reg field of the ModR/M byte selects a control register (for example, MOV (0F20, 0F22)).

D  The reg field of the ModR/M byte selects a debug register (for example, MOV (0F21,0F23)).

E  A ModR/M byte follows the opcode and specifies the operand. The operand is either a general-purpose register or a memory address. If it is a memory address, the address is computed from a segment register and any of the following values: a base register, an index register, a scaling factor, a displacement.

F  EFLAGS/RFLAGS Register.

G  The reg field of the ModR/M byte selects a general register (for example, AX (000)).

H  The VEX.vvvv field of the VEX prefix selects a 128-bit XMM register or a 256-bit YMM register, determined by operand type. For legacy SSE encodings this operand does not exist, changing the instruction to destructive form.

I  Immediate data: the operand value is encoded in subsequent bytes of the instruction.

J  The instruction contains a relative offset to be added to the instruction pointer register (for example, JMP (0E9), LOOP).

L  The upper 4 bits of the 8-bit immediate selects a 128-bit XMM register or a 256-bit YMM register, determined by operand type. (the MSB is ignored in 32-bit mode)
M The ModR/M byte may refer only to memory (for example, BOUND, LES, LDS, LSS, LFS, LGS, CMPXCHG8B).

N The R/M field of the ModR/M byte selects a packed-quadword, MMX technology register.

O The instruction has no ModR/M byte. The offset of the operand is coded as a word or double word (depending on address size attribute) in the instruction. No base register, index register, or scaling factor can be applied (for example, MOV (A0–A3)).

P The reg field of the ModR/M byte selects a packed quadword MMX technology register.

Q A ModR/M byte follows the opcode and specifies the operand. The operand is either an MMX technology register or a memory address. If it is a memory address, the address is computed from a segment register and any of the following values: a base register, an index register, a scaling factor, and a displacement.

R The R/M field of the ModR/M byte may refer only to a general register (for example, MOV (0F20-0F23)).

S The reg field of the ModR/M byte selects a segment register (for example, MOV (8C,8E)).

U The R/M field of the ModR/M byte selects a 128-bit XMM register or a 256-bit YMM register, determined by operand type.

V The reg field of the ModR/M byte selects a 128-bit XMM register or a 256-bit YMM register, determined by operand type.

W A ModR/M byte follows the opcode and specifies the operand. The operand is either a 128-bit XMM register, a 256-bit YMM register (determined by operand type), or a memory address. If it is a memory address, the address is computed from a segment register and any of the following values: a base register, an index register, a scaling factor, and a displacement.

X Memory addressed by the DS:rSI register pair (for example, MOV, CMPS, OUTS, or LODS).

Y Memory addressed by the ES:rDI register pair (for example, MOV, CMPS, INS, STOS, or SCAS).

### A.2.2 Codes for Operand Type

The following abbreviations are used to document operand types:

- **a** Two one-word operands in memory or two double-word operands in memory, depending on operand-size attribute (used only by the BOUND instruction).
- **b** Byte, regardless of operand-size attribute.
- **c** Byte or word, depending on operand-size attribute.
- **d** Doubleword, regardless of operand-size attribute.
OPCODE MAP

dq Double-quadword, regardless of operand-size attribute.
p 32-bit, 48-bit, or 80-bit pointer, depending on operand-size attribute.
pd 128-bit or 256-bit packed double-precision floating-point data.
pi Quadword MMX technology register (for example: mm0).
ps 128-bit or 256-bit packed single-precision floating-point data.
q Quadword, regardless of operand-size attribute.
qq Quad-Quadword (256-bits), regardless of operand-size attribute.
s 6-byte or 10-byte pseudo-descriptor.
sd Scalar element of a 128-bit double-precision floating data.
ss Scalar element of a 128-bit single-precision floating data.
si Doubleword integer register (for example: eax).
v Word, doubleword or quadword (in 64-bit mode), depending on operand-size attribute.
w Word, regardless of operand-size attribute.
x dq or qq based on the operand-size attribute.
y Doubleword or quadword (in 64-bit mode), depending on operand-size attribute.
z Word for 16-bit operand-size or doubleword for 32 or 64-bit operand-size.

A.2.3 Register Codes

When an opcode requires a specific register as an operand, the register is identified by name (for example, AX, CL, or ESI). The name indicates whether the register is 64, 32, 16, or 8 bits wide.

A register identifier of the form eXX or rXX is used when register width depends on the operand-size attribute. eXX is used when 16 or 32-bit sizes are possible; rXX is used when 16, 32, or 64-bit sizes are possible. For example: eAX indicates that the AX register is used when the operand-size attribute is 16 and the EAX register is used when the operand-size attribute is 32. rAX can indicate AX, EAX or RAX.

When the REX.B bit is used to modify the register specified in the reg field of the opcode, this fact is indicated by adding "/x" to the register name to indicate the additional possibility. For example, rCX/r9 is used to indicate that the register could either be rCX or r9. Note that the size of r9 in this case is determined by the operand size attribute (just as for rCX).
A.2.4 Opcode Look-up Examples for One, Two, and Three-Byte Opcodes

This section provides examples that demonstrate how opcode maps are used.

A.2.4.1 One-Byte Opcode Instructions

The opcode map for 1-byte opcodes is shown in Table A-2. The opcode map for 1-byte opcodes is arranged by row (the least-significant 4 bits of the hexadecimal value) and column (the most-significant 4 bits of the hexadecimal value). Each entry in the table lists one of the following types of opcodes:

- Instruction mnemonics and operand types using the notations listed in Section A.2
- Opcodes used as an instruction prefix

For each entry in the opcode map that corresponds to an instruction, the rules for interpreting the byte following the primary opcode fall into one of the following cases:

- A ModR/M byte is required and is interpreted according to the abbreviations listed in Section A.1 and Chapter 2, "Instruction Format," of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A. Operand types are listed according to notations listed in Section A.2.
- A ModR/M byte is required and includes an opcode extension in the reg field in the ModR/M byte. Use Table A-6 when interpreting the ModR/M byte.
- Use of the ModR/M byte is reserved or undefined. This applies to entries that represent an instruction prefix or entries for instructions without operands that use ModR/M (for example: 60H, PUSHA; 06H, PUSH ES).

Example A-1. Look-up Example for 1-Byte Opcodes

Opcode 030500000000H for an ADD instruction is interpreted using the 1-byte opcode map (Table A-2) as follows:

- The first digit (0) of the opcode indicates the table row and the second digit (3) indicates the table column. This locates an opcode for ADD with two operands.
- The first operand (type Gv) indicates a general register that is a word or doubleword depending on the operand-size attribute. The second operand (type Ev) indicates a ModR/M byte follows that specifies whether the operand is a word or doubleword general-purpose register or a memory address.
- The ModR/M byte for this instruction is 05H, indicating that a 32-bit displacement follows (00000000H). The reg/opcode portion of the ModR/M byte (bits 3-5) is 000, indicating the EAX register.

The instruction for this opcode is ADD EAX, mem_op, and the offset of mem_op is 00000000H.
OPCODE MAP

Some 1- and 2-byte opcodes point to group numbers (shaded entries in the opcode map table). Group numbers indicate that the instruction uses the reg(opcode bits in the ModR/M byte as an opcode extension (refer to Section A.4).

A.2.4.2 Two-Byte Opcode Instructions

The two-byte opcode map shown in Table A-3 includes primary opcodes that are either two bytes or three bytes in length. Primary opcodes that are 2 bytes in length begin with an escape opcode 0FH. The upper and lower four bits of the second opcode byte are used to index a particular row and column in Table A-3.

Two-byte opcodes that are 3 bytes in length begin with a mandatory prefix (66H, F2H, or F3H) and the escape opcode (0FH). The upper and lower four bits of the third byte are used to index a particular row and column in Table A-3 (except when the second opcode byte is the 3-byte escape opcodes 38H or 3AH; in this situation refer to Section A.2.4.3).

For each entry in the opcode map, the rules for interpreting the byte following the primary opcode fall into one of the following cases:

- A ModR/M byte is required and is interpreted according to the abbreviations listed in Section A.1 and Chapter 2, "Instruction Format," of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A. The operand types are listed according to notations listed in Section A.2.
- A ModR/M byte is required and includes an opcode extension in the reg field in the ModR/M byte. Use Table A-6 when interpreting the ModR/M byte.
- Use of the ModR/M byte is reserved or undefined. This applies to entries that represent an instruction without operands that are encoded using ModR/M (for example: 0F77H, EMMS).

Example A-2. Look-up Example for 2-Byte Opcodes

Look-up opcode 0FA4050000000003H for a SHLD instruction using Table A-3.

- The opcode is located in row A, column 4. The location indicates a SHLD instruction with operands Ev, Gv, and Ib. Interpret the operands as follows:
  - Ev: The ModR/M byte follows the opcode to specify a word or doubleword operand.
  - Gv: The reg field of the ModR/M byte selects a general-purpose register.
  - Ib: Immediate data is encoded in the subsequent byte of the instruction.
- The third byte is the ModR/M byte (05H). The mod and opcode/reg fields of ModR/M indicate that a 32-bit displacement is used to locate the first operand in memory and eAX as the second operand.
- The next part of the opcode is the 32-bit displacement for the destination memory operand (00000000H). The last byte stores immediate byte that provides the count of the shift (03H).
• By this breakdown, it has been shown that this opcode represents the instruction: SHLD DS:00000000H, EAX, 3.

A.2.4.3 Three-Byte Opcode Instructions

The three-byte opcode maps shown in Table A-4 and Table A-5 includes primary opcodes that are either 3 or 4 bytes in length. Primary opcodes that are 3 bytes in length begin with two escape bytes 0F38H or 0F3A. The upper and lower four bits of the third opcode byte are used to index a particular row and column in Table A-4 or Table A-5.

Three-byte opcodes that are 4 bytes in length begin with a mandatory prefix (66H, F2H, or F3H) and two escape bytes (0F38H or 0F3AH). The upper and lower four bits of the fourth byte are used to index a particular row and column in Table A-4 or Table A-5.

For each entry in the opcode map, the rules for interpreting the byte following the primary opcode fall into the following case:
• A ModR/M byte is required and is interpreted according to the abbreviations listed in A.1 and Chapter 2, “Instruction Format,” of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A. The operand types are listed according to notations listed in Section A.2.

Example A-3. Look-up Example for 3-Byte Opcodes

Look-up opcode 660F3A0FC108H for a PALIGNR instruction using Table A-5.

• 66H is a prefix and 0F3AH indicate to use Table A-5. The opcode is located in row 0, column F indicating a PALIGNR instruction with operands Vdq, Wdq, and Ib. Interpret the operands as follows:
  — Vdq: The reg field of the ModR/M byte selects a 128-bit XMM register.
  — Wdq: The R/M field of the ModR/M byte selects either a 128-bit XMM register or memory location.
  — Ib: Immediate data is encoded in the subsequent byte of the instruction.
• The next byte is the ModR/M byte (C1H). The reg field indicates that the first operand is XMM0. The mod shows that the R/M field specifies a register and the R/M indicates that the second operand is XMM1.
• The last byte is the immediate byte (08H).
• By this breakdown, it has been shown that this opcode represents the instruction: PALIGNR XMM0, XMM1, 8.

A.2.4.4 VEX Prefix Instructions

Instructions that include a VEX prefix are organized relative to the 2-byte and 3-byte opcode maps, based on the VEX.mmmmm field encoding of implied 0F, 0F38H, 0F3AH, respectively. Each entry in the opcode map of a VEX-encoded instruction is based on the value of the opcode byte, similar to non-VEX-encoded instructions.
A VEX prefix includes several bit fields that encode implied 66H, F2H, F3H prefix functionality (VEX.pp) and operand size/opcode information (VEX.L). See chapter 4 for details.

Opcode tables A2-A6 include both instructions with a VEX prefix and instructions without a VEX prefix. Many entries are only made once, but represent both the VEX and non-VEX forms of the instruction. If the VEX prefix is present all the operands are valid and the mnemonic is usually prefixed with a “v”. If the VEX prefix is not present the VEX.vvvv operand is not available and the prefix “v” is dropped from the mnemonic.

A few instructions exist only in VEX form and these are marked with a superscript “v”.

Operand size of VEX prefix instructions can be determined by the operand type code. 128-bit vectors are indicated by 'dq', 256-bit vectors are indicated by 'qq', and instructions with operands supporting either 128 or 256-bit, determined by VEX.L, are indicated by 'x'. For example, the entry "VMOVUPD Vx,Wx" indicates both VEX.L=0 and VEX.L=1 are supported.

### A.2.5 Superscripts Utilized in Opcode Tables

Table A-1 contains notes on particular encodings. These notes are indicated in the following opcode maps by superscripts. Gray cells indicate instruction groupings.

**Table A-1. Superscripts Utilized in Opcode Tables**

<table>
<thead>
<tr>
<th>Superscript Symbol</th>
<th>Meaning of Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1A</td>
<td>Bits 5, 4, and 3 of ModR/M byte used as an opcode extension (refer to Section A.4, &quot;Opcode Extensions For One-Byte And Two-byte Opcodes&quot;).</td>
</tr>
<tr>
<td>1B</td>
<td>Use the 0F0B opcode (UD2 instruction) or the 0FB9H opcode when deliberately trying to generate an invalid opcode exception (#UD).</td>
</tr>
<tr>
<td>1C</td>
<td>Some instructions use the same two-byte opcode. If the instruction has variations, or the opcode represents different instructions, the ModR/M byte will be used to differentiate the instruction. For the value of the ModR/M byte needed to decode the instruction, see Table A-6.</td>
</tr>
<tr>
<td>i64</td>
<td>The instruction is invalid or not encodable in 64-bit mode. 40 through 4F (single-byte INC and DEC) are REX prefix combinations when in 64-bit mode (use FE/FF Grp 4 and 5 for INC and DEC).</td>
</tr>
<tr>
<td>o64</td>
<td>Instruction is only available when in 64-bit mode.</td>
</tr>
<tr>
<td>d64</td>
<td>When in 64-bit mode, instruction defaults to 64-bit operand size and cannot encode 32-bit operand size.</td>
</tr>
<tr>
<td>f64</td>
<td>The operand size is forced to a 64-bit operand size when in 64-bit mode (prefixes that change operand size are ignored for this instruction in 64-bit mode).</td>
</tr>
</tbody>
</table>
A.3 ONE, TWO, AND THREE-BYTE OPCODE MAPS

See Table A-2 through Table A-5 below. The tables are multiple page presentations. Rows and columns with sequential relationships are placed on facing pages to make look-up tasks easier. Note that table footnotes are not presented on each page. Table footnotes for each table are presented on the last page of the table.

<table>
<thead>
<tr>
<th>Superscript Symbol</th>
<th>Meaning of Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>v</td>
<td>VEX form only exists. There is no legacy SSE form of the instruction. For Integer GPR instructions it means VEX prefix required.</td>
</tr>
<tr>
<td>v1</td>
<td>VEX128 &amp; SSE forms only exist (no VEX256), when can’t be inferred from the data size.</td>
</tr>
</tbody>
</table>
## Table A-2. One-byte Opcode Map: (00H — F7H) *

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>Eb, Gb</td>
<td>Ev, Gv</td>
<td>Gb, Eb</td>
<td>Gv, Ev</td>
<td>AL, Ib</td>
<td>rAX, Iz</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Eb, Gb</td>
<td>Ev, Gv</td>
<td>Gb, Eb</td>
<td>Gv, Ev</td>
<td>AL, Ib</td>
<td>rAX, Iz</td>
</tr>
<tr>
<td>2</td>
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<td>Ev, Gv</td>
<td>Gb, Eb</td>
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<td>rAX, Iz</td>
</tr>
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<td>rAX, Iz</td>
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<td>5</td>
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<td>rAX/r8</td>
<td>rCX/r9</td>
<td>rDX/r10</td>
<td>rSP/r11</td>
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<td>rSI/r14</td>
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<td>Ev, Izb</td>
<td>Eb, Izb</td>
<td>Ev, Izb</td>
</tr>
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*OPCODE MAP*
# OPCODE MAP

## Table A-2. One-byte Opcode Map: (08H — FFH) *

<table>
<thead>
<tr>
<th>B</th>
<th>9</th>
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<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
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<td>GB</td>
<td>EV</td>
<td>GV</td>
<td>GB</td>
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<td>EV</td>
<td>GV</td>
<td>GB</td>
<td>EB</td>
</tr>
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<td>GB</td>
<td>EV</td>
<td>GV</td>
<td>GB</td>
<td>EB</td>
</tr>
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<td>GV</td>
<td>GB</td>
<td>EB</td>
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<td>EB</td>
</tr>
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<td>EB</td>
</tr>
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<td>GB</td>
<td>EV</td>
<td>GV</td>
<td>GB</td>
<td>EB</td>
</tr>
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</table>

### Notes:

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
# Opcode Map

**Table A-3. Two-byte Opcode Map: 00H — 77H (First Byte is OFH)**

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<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Grp 6**</td>
<td>Grp 7**</td>
<td>LAR Gv, Ew</td>
<td>LSL Gv, Ew</td>
<td>SYSCALL**</td>
<td>CLTS</td>
<td>SYSRET**</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>vmovups</td>
<td>vmovups</td>
<td>vmovlps Vq, Hq, Mq</td>
<td>vmovlps Vq, Hq, Uq</td>
<td>vunpcklps Vx, Hx, Wx</td>
<td>vunpcklps Vx, Hx, Wx</td>
<td>vmovhps Vd, Hq, Mq</td>
<td>vmovhps Vd, Hq, Uq</td>
</tr>
<tr>
<td>2</td>
<td>vmovqps</td>
<td>vmovqps</td>
<td>vmovlhps Vq, Hq, Mq</td>
<td>vmovlhps Vq, Hq, Uq</td>
<td>vunpckhps Vx, Hx, Wx</td>
<td>vunpckhps Vx, Hx, Wx</td>
<td>vmovhps Vd, Hq, Mq</td>
<td>vmovhps Vd, Hq, Uq</td>
</tr>
<tr>
<td>3</td>
<td>vmovss</td>
<td>vmovdups Vq, Hq, Mq</td>
<td>vmovlps Mq, Vq</td>
<td>vunpcklps Vx, Hx, Wx</td>
<td>vunpckhps Vx, Hx, Wx</td>
<td>vmovhps Vd, Hq, Mq</td>
<td>vmovhps Vd, Hq, Uq</td>
<td>vmovhps Vd, Hq, Mq</td>
</tr>
<tr>
<td>4</td>
<td>vmovsd</td>
<td>vmovdups Vq, Hq, Mq</td>
<td>vmovlps Mq, Vq</td>
<td>vunpcklps Vx, Hx, Wx</td>
<td>vunpckhps Vx, Hx, Wx</td>
<td>vmovhps Vd, Hq, Mq</td>
<td>vmovhps Vd, Hq, Uq</td>
<td>vmovhps Vd, Hq, Mq</td>
</tr>
<tr>
<td>6</td>
<td>vunpcklps Vx, Hx, Wx</td>
<td>vunpckhps Vx, Hx, Wx</td>
<td>vpacksswb Vq, Hq, Mq</td>
<td>vpcmpgtb Vq, Hq, Mq</td>
<td>vpcmpgtw Vq, Hq, Mq</td>
<td>vpcmpgtd Vq, Hq, Mq</td>
<td>vpackuswb Vq, Hq, Mq</td>
<td>vpackuswb Vq, Hq, Mq</td>
</tr>
<tr>
<td>7</td>
<td>vunpckhdps Vx, Hx, Wx</td>
<td>vunpckhps Vx, Hx, Wx</td>
<td>vpacksswb Vq, Hq, Mq</td>
<td>vpcmpgtb Vq, Hq, Mq</td>
<td>vpcmpgtw Vq, Hq, Mq</td>
<td>vpcmpgtd Vq, Hq, Mq</td>
<td>vpackuswb Vq, Hq, Mq</td>
<td>vpackuswb Vq, Hq, Mq</td>
</tr>
</tbody>
</table>

**Notes:**
- **Grp 6** and **Grp 7** are groups of instructions that start with the specified prefixes.
- **LAR** and **LSL** are logical arithmetic and logical shift instructions.
- **SYSCALL** and **CLTS** are system calls and clearing the trap flag.
- **SYSRET** is a system return instruction.
- **CMOVcc** is a conditional move instruction.
- **BE/NA** and **ANBE** are flags for branch conditions.
- **VZEROU** and **VZERALL** are zero-related instructions.

**Prefixes:**
- **F3** and **F2** prefixes are used for specific instructions.
- **66** and **F3** are used for 32-bit and 64-bit operations.
- **F2** is used for 32-bit operations.

**Instructions:**
- **vmovups**, **vmovlps**, **vunpcklps**, etc., are move instructions.
- **vsqrtss**, **vrcpss**, **vandps**, etc., are mathematical operations.
- **vandnps**, **vorcps**, **vpacksswb**, etc., are logical operations.
- **vpcmpgtb**, **vpackuswb**, etc., are comparison operations.
- **vzeroupper** and **vzerall** are zero-related instructions.

---

* This table is exclusive to the first byte being OFH.
Table A-3. Two-byte Opcode Map: 08H — 7FH (First Byte is 0FH) *

<table>
<thead>
<tr>
<th>Prefix</th>
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<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>INVD WBINVD</td>
<td>2-byte Illegal</td>
<td>0FH</td>
<td>NOP Ev</td>
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</tr>
<tr>
<td>1</td>
<td>Prefetch&lt;sup&gt;1C&lt;/sup&gt; (Grp 16)&lt;sup&gt;2A&lt;/sup&gt;</td>
<td>NOP Ev</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>vmovaps Vps, Wps</td>
<td>vmovaps Vps, Wps</td>
<td>vcmovaps Vps, Wps</td>
<td>vcmovaps Vps, Wps</td>
<td>vcmovaps Vps, Wps</td>
</tr>
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<td>3-byte escape (Table A-4)</td>
<td>3-byte escape (Table A-5)</td>
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</tr>
<tr>
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<td>S</td>
<td>NS</td>
<td>P/PE</td>
<td>NP/PO</td>
<td>L/NGE</td>
</tr>
<tr>
<td>5</td>
<td>vaddps Vps, Hps, Wps</td>
<td>vmulps Vps, Hps, Wps</td>
<td>vcvtsi2ps Vps, Qpi</td>
<td>vmovntps Qps, Wps</td>
<td>cvtsi2ps Qpi, Wps</td>
</tr>
<tr>
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<td>vaddpd Vpd, Hpd, Wpd</td>
<td>vmulpd Vpd, Hpd, Wpd</td>
<td>vcvtsi2pd Vpd, Qpi</td>
<td>vmovntpd Qpd, Wpd</td>
<td>cvtsi2pd Qpi, Wpd</td>
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<td>7</td>
<td>VMREAD Ey, Gy</td>
<td>VMWRITE Gy, Ey</td>
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<td></td>
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* OPCodes UD2<sup>1B</sup> and UD2<sup>1D</sup> are 2-byte illegal.
### Table A-3. Two-byte Opcode Map: 80H — F7H (First Byte is 0FH) *

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<th>6</th>
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<tbody>
<tr>
<td>8</td>
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<td>NO</td>
<td>B/CNAE</td>
<td>AE/NB/NC</td>
<td>E/Z</td>
<td>NE/NZ</td>
<td>BE/NA</td>
<td>A/NBE</td>
</tr>
<tr>
<td></td>
<td>Jcc&lt;sup&gt;T&lt;/sup&gt;, Jz - Long-displacement jump on condition</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>O</td>
<td>NO</td>
<td>B/CNAE</td>
<td>AE/NB/NC</td>
<td>E/Z</td>
<td>NE/NZ</td>
<td>BE/NA</td>
<td>A/NBE</td>
</tr>
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<td></td>
<td>SETcc, Eb - Byte Set on condition</td>
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<td>PUSH&lt;sup&gt;8&lt;/sup&gt; FS</td>
<td>POP&lt;sup&gt;8&lt;/sup&gt; FS</td>
<td>CPUID</td>
<td>BT</td>
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<td>Ev, Gv, CL</td>
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<td>Gv, Mp</td>
<td>Ev, Gv</td>
<td>Gv, Mp</td>
<td>Gv, Gv</td>
<td>Gv, Hv</td>
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<td>movnti</td>
<td>pinnr</td>
<td>vpmadd</td>
<td>vshufps</td>
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<td>Ev, Gv</td>
<td>Vps, Wps, Wps, Ib</td>
<td>My, Gy</td>
<td>Pq, Ry, Mw, Ib</td>
<td>Vps, Wps, Wps, Ib</td>
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<td>vpsldq</td>
<td>vpadld</td>
<td>vpmullw</td>
<td>pmovmskb</td>
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<td></td>
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<td>Vg, Gv</td>
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<td>movntq</td>
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<td>Vx, Hx, Wx</td>
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<td>Vx, Hx, Wx</td>
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<td>vpslllq</td>
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<td>vmovntdq</td>
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<td>Vx, Hx, Wx</td>
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<sup>T</sup> Clp 9<sup>TA</sup>
## Table A-3. Two-byte Opcode Map: 88H — FFH (First Byte is 0FH) *

<table>
<thead>
<tr>
<th>pfx</th>
<th>8</th>
<th>9</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>S</td>
<td>NS</td>
<td>P/PE</td>
<td>NP/PO</td>
<td>L/NGE</td>
<td>NL/GE</td>
<td>LE/NG</td>
<td>NLE/G</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td>Jcc&lt;sup&gt;±&lt;/sup&gt;, Jz - Long-displacement jump on condition</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>9</td>
<td>S</td>
<td>NS</td>
<td>P/PE</td>
<td>NP/PO</td>
<td>L/NGE</td>
<td>NL/GE</td>
<td>LE/NG</td>
<td>NLE/G</td>
</tr>
<tr>
<td>A</td>
<td>PUSHd64 GS</td>
<td>POPd64 GS</td>
<td>RSM</td>
<td>BTS</td>
<td>SHRD</td>
<td>SHRD</td>
<td>(Gpr 15&lt;sup&gt;15/16&lt;sup&gt;)&lt;sup&gt;16&lt;/sup&gt;</td>
<td>IMUL</td>
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<tr>
<td>B</td>
<td>JMP&lt;sup&gt;±&lt;/sup&gt; (reserved for emulator on IPF)</td>
<td>Grp 10&lt;sup&gt;15/16&lt;sup&gt;</td>
<td>Grp 8&lt;sup&gt;15/16&lt;sup&gt;</td>
<td>Grp 1&lt;sup&gt;15/16&lt;sup&gt;</td>
<td>BTC</td>
<td>BSF</td>
<td>BSR</td>
<td>MOV/SX</td>
</tr>
<tr>
<td>D</td>
<td>psubb Pq, Qq</td>
<td>psubw Pq, Qq</td>
<td>pmmin Hx, Wx</td>
<td>pand Hx, Wx</td>
<td>paddusw Pq, Qq</td>
<td>paddus Pq, Qq</td>
<td>paddpsw Pq, Qq</td>
<td>paddps Pq, Qq</td>
</tr>
<tr>
<td>E</td>
<td>vpsubb Vx, Hx, Wx</td>
<td>vpsubw Vx, Hx, Wx</td>
<td>vpmmin Vx, Hx, Wx</td>
<td>vpand Vx, Hx, Wx</td>
<td>vpaddusw Vx, Hx, Wx</td>
<td>vpaddus Vx, Hx, Wx</td>
<td>vpaddpsw Vx, Hx, Wx</td>
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### NOTES:

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
## Three-byte Opcode Map: 00H — F7H (First Two Bytes are 0F 38H)

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**NOTES:**
* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
### Table A-5. Three-byte Opcode Map: 00H — F7H (First two bytes are OF 3AH) *

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*Note: px refers to the first byte of the three-byte opcode. The opcodes listed are for the Intel x86 architecture.*
### Table A-5. Three-byte Opcode Map: 08H — FFH (First Two Bytes are 0F 3AH) *

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<td>Vx, Hz, Wx, lb</td>
<td>Vx, Hz, Wx, lb</td>
<td>Vx, Hz, Wx, lb</td>
<td>Pq, Qq, lb</td>
</tr>
<tr>
<td>1</td>
<td>66</td>
<td>vinsertf128</td>
<td>vextractf128</td>
<td>vinsertf128</td>
<td>vextractf128</td>
<td>vinsertf128</td>
<td>vextractf128</td>
<td>vinsertf128</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>66</td>
<td>vinserti128</td>
<td>vextracti128</td>
<td>vinserti128</td>
<td>vextracti128</td>
<td>vinserti128</td>
<td>vextracti128</td>
<td>vinserti128</td>
</tr>
<tr>
<td>4</td>
<td>66</td>
<td>vblendvps</td>
<td>vblendvpd</td>
<td>vblendvps</td>
<td>vblendvpd</td>
<td>vblendvps</td>
<td>vblendvpd</td>
<td>vblendvps</td>
</tr>
<tr>
<td></td>
<td>Vx, Hx, Wx, lb</td>
<td>Vx, Hx, Wx, lb</td>
<td>Vx, Hx, Wx, lb</td>
<td>Vx, Hx, Wx, lb</td>
<td>Vx, Hx, Wx, lb</td>
<td>Vx, Hx, Wx, lb</td>
<td>Vx, Hx, Wx, lb</td>
<td>Vx, Hx, Wx, lb</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>66</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
A.4  OPCODE EXTENSIONS FOR ONE-BYTE AND TWO-BYTE OPCODES

Some 1-byte and 2-byte opcodes use bits 3-5 of the ModR/M byte (the nnn field in Figure A-1) as an extension of the opcode.

<table>
<thead>
<tr>
<th>mod</th>
<th>nnn</th>
<th>R/M</th>
</tr>
</thead>
</table>

Figure A-1. ModR/M Byte nnn Field (Bits 5, 4, and 3)

Opcodes that have opcode extensions are indicated in Table A-6 and organized by group number. Group numbers (from 1 to 16, second column) provide a table entry point. The encoding for the r/m field for each instruction can be established using the third column of the table.

A.4.1  Opcode Look-up Examples Using Opcode Extensions

An Example is provided below.

Example A-4. Interpreting an ADD Instruction

An ADD instruction with a 1-byte opcode of 80H is a Group 1 instruction:
• Table A-6 indicates that the opcode extension field encoded in the ModR/M byte for this instruction is 000B.
• The r/m field can be encoded to access a register (11B) or a memory address using a specified addressing mode (for example: mem = 00B, 01B, 10B).

Example A-5. Looking Up 0F01C3H

Look up opcode 0F01C3 for a VMRESUME instruction by using Table A-2, Table A-3 and Table A-6:
• 0F tells us that this instruction is in the 2-byte opcode map.
• 01 (row 0, column 1 in Table A-3) reveals that this opcode is in Group 7 of Table A-6.
• C3 is the ModR/M byte. The first two bits of C3 are 11B. This tells us to look at the second of the Group 7 rows in Table A-6.
• The Op/Reg bits [5,4,3] are 000B. This tells us to look in the 000 column for Group 7.
• Finally, the R/M bits [2,1,0] are 011B. This identifies the opcode as the VMRESUME instruction.
### A.4.2 Opcode Extension Tables

See Table A-6 below.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Group</th>
<th>Mod 7,6</th>
<th>pfx</th>
<th>000</th>
<th>001</th>
<th>010</th>
<th>011</th>
<th>100</th>
<th>101</th>
<th>110</th>
<th>111</th>
</tr>
</thead>
<tbody>
<tr>
<td>80-83</td>
<td>1</td>
<td>mem, 11B</td>
<td>ADD</td>
<td>OR</td>
<td>ADC</td>
<td>SBB</td>
<td>AND</td>
<td>SUB</td>
<td>XOR</td>
<td>CMP</td>
<td></td>
</tr>
<tr>
<td>8F</td>
<td>1A</td>
<td>mem, 11B</td>
<td>POP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>03, C1 reg, imm</td>
<td>2</td>
<td>mem, 11B</td>
<td>ROL</td>
<td>ROR</td>
<td>RCL</td>
<td>RCR</td>
<td>SHL/SAL</td>
<td>SHR</td>
<td>SAR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F6, F7</td>
<td>3</td>
<td>mem, 11B</td>
<td>TEST</td>
<td>NOT</td>
<td>NEG</td>
<td>MUL</td>
<td>AL/iAX</td>
<td>IMUL</td>
<td>AL/iAX</td>
<td>DIV</td>
<td>IDIV</td>
</tr>
<tr>
<td>FF</td>
<td>4</td>
<td>mem, 11B</td>
<td>INC</td>
<td>Eb</td>
<td>DEC</td>
<td>Eb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F 00</td>
<td>5</td>
<td>mem, 11B</td>
<td>INC</td>
<td>Eb</td>
<td>DEC</td>
<td>Eb</td>
<td>CALL</td>
<td>CALL</td>
<td>JMPN</td>
<td>JMPF</td>
<td>PUSH</td>
</tr>
<tr>
<td>0F 01</td>
<td>6</td>
<td>mem, 11B</td>
<td>TRY</td>
<td>Rv/Mw</td>
<td>STR</td>
<td>Rv/Mw</td>
<td>LLDT</td>
<td>Ew</td>
<td>LTR</td>
<td>Ew</td>
<td>VERR</td>
</tr>
<tr>
<td>0F BA</td>
<td>7</td>
<td>mem, 11B</td>
<td>SGET</td>
<td>Mq</td>
<td>VLSTR</td>
<td>Mq</td>
<td>MMONITOR</td>
<td>Mq</td>
<td>XMGETBV</td>
<td>XMSETBV</td>
<td>VMFUNC</td>
</tr>
<tr>
<td>0F C7</td>
<td>8</td>
<td>mem, 11B</td>
<td>CMPXCHSB</td>
<td>Mq</td>
<td>VMXADD</td>
<td>Mq</td>
<td>VMXADD16</td>
<td>Mq</td>
<td>VMXADD</td>
<td>VMXADD16</td>
<td>Mq</td>
</tr>
<tr>
<td>0F B9</td>
<td>9</td>
<td>mem, 11B</td>
<td>VMCLR</td>
<td>Mq</td>
<td>VMXON</td>
<td>Mq</td>
<td>VMXON</td>
<td>Mq</td>
<td>VMXON</td>
<td>Mq</td>
<td></td>
</tr>
<tr>
<td>C6</td>
<td>10</td>
<td>mem, 11B</td>
<td>MOV</td>
<td>Eb, Ib</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C7</td>
<td>11</td>
<td>mem, 11B</td>
<td>MOV</td>
<td>Ev, lz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Table A-6. Opcode Extensions for One- and Two-byte Opcodes by Group Number *

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Group</th>
<th>Mem</th>
<th>Mod 7, 6</th>
<th>pfx</th>
<th>Encoding of Bits 5,4,3 of the ModR/M Byte (bits 2,1,0 in parenthesis)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 71</td>
<td>12</td>
<td>mem</td>
<td>11B</td>
<td></td>
<td>pslw Nq, lb, Nq, lb, Nq, lb</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>66</td>
<td></td>
<td>vpsrlw Hx, Ux, lb, vpsraw Hx, Ux, lb, vpsllw Hx, Ux, lb</td>
</tr>
<tr>
<td>0F 72</td>
<td>13</td>
<td>mem</td>
<td>11B</td>
<td></td>
<td>psrlid Nq, lb, psrad Nq, lb, psllid Nq, lb</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>66</td>
<td></td>
<td>vpsrlid Hx, Ux, lb, vpsrad Hx, Ux, lb, vpsllid Hx, Ux, lb</td>
</tr>
<tr>
<td>0F 73</td>
<td>14</td>
<td>mem</td>
<td>11B</td>
<td></td>
<td>pslq Nq, lb, pslq Nq, lb</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>66</td>
<td></td>
<td>vpsrlq Hx, Ux, lb, vpsrlq Hx, Ux, lb, vpsllq Hx, Ux, lb, vpsllq Hx, Ux, lb</td>
</tr>
<tr>
<td>0F AE</td>
<td>15</td>
<td>mem</td>
<td>11B</td>
<td></td>
<td>fxsave, fxstor, ldmxcsr, stmxcsr, XSAVE, XRSTOR, XSAVEOPT, clflush</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>lience, mfence, sfence</td>
</tr>
<tr>
<td>0F 18</td>
<td>16</td>
<td>mem</td>
<td>11B</td>
<td></td>
<td>prefetch NTA, prefetch T0, prefetch T1, prefetch T2</td>
</tr>
<tr>
<td>VEX:0F38 F3</td>
<td>17</td>
<td>mem</td>
<td>11B</td>
<td></td>
<td>BLSR7 By, Ey, BLSMSK7 By, Ey, BLS7 By, Ey</td>
</tr>
</tbody>
</table>

### NOTES:

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
A.5  ESCAPE OPCODE INSTRUCTIONS

Opcode maps for coprocessor escape instruction opcodes (x87 floating-point instruction opcodes) are in Table A-7 through Table A-22. These maps are grouped by the first byte of the opcode, from D8-DF. Each of these opcodes has a ModR/M byte. If the ModR/M byte is within the range of 00H-BFH, bits 3-5 of the ModR/M byte are used as an opcode extension, similar to the technique used for 1-and 2-byte opcodes (see A.4). If the ModR/M byte is outside the range of 00H through BFH, the entire ModR/M byte is used as an opcode extension.

A.5.1  Opcode Look-up Examples for Escape Instruction Opcodes

Examples are provided below.

Example A-6.  Opcode with ModR/M Byte in the 00H through BFH Range

DD0504000000H can be interpreted as follows:

• The instruction encoded with this opcode can be located in Section. Since the ModR/M byte (05H) is within the 00H through BFH range, bits 3 through 5 (000) of this byte indicate the opcode for an FLD double-real instruction (see Table A-9).

• The double-real value to be loaded is at 00000004H (the 32-bit displacement that follows and belongs to this opcode).

Example A-7.  Opcode with ModR/M Byte outside the 00H through BFH Range

D8C1H can be interpreted as follows:

• This example illustrates an opcode with a ModR/M byte outside the range of 00H through BFH. The instruction can be located in Section A.4.

• In Table A-8, the ModR/M byte C1H indicates row C, column 1 (the FADD instruction using ST(0), ST(1) as operands).

A.5.2  Escape Opcode Instruction Tables

Tables are listed below.
### OPCODE MAP

#### A.5.2.1 Escape Opcodes with D8 as First Byte

Table A-7 and A-8 contain maps for the escape instruction opcodes that begin with D8H. Table A-7 shows the map if the ModR/M byte is in the range of 00H-BFH. Here, the value of bits 3-5 (the nnn field in Figure A-1) selects the instruction.

**Table A-7. D8 Opcode Map When ModR/M Byte is Within 00H to BFH * **

<table>
<thead>
<tr>
<th>nnn Field of ModR/M Byte (refer to Figure A.4)</th>
<th>000B</th>
<th>001B</th>
<th>010B</th>
<th>011B</th>
<th>100B</th>
<th>101B</th>
<th>110B</th>
<th>111B</th>
</tr>
</thead>
<tbody>
<tr>
<td>FADD single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FMUL single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FCOM single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FCOMP single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSUB single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSUBR single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FDIV single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FDIVR single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.

Table A-8 shows the map if the ModR/M byte is outside the range of 00H-BFH. Here, the first digit of the ModR/M byte selects the table row and the second digit selects the column.

**Table A-8. D8 Opcode Map When ModR/M Byte is Outside 00H to BFH * **

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>FADD</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>D</td>
<td>FCOM</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>E</td>
<td>FSUB</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>F</td>
<td>FDIV</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
</tbody>
</table>

**NOTES:**

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
### A.5.2.2 Escape Opcodes with D9 as First Byte

Table A-9 and A-10 contain maps for escape instruction opcodes that begin with D9H. Table A-9 shows the map if the ModR/M byte is in the range of 00H-BFH. Here, the value of bits 3-5 (the nnn field in Figure A-1) selects the instruction.

#### Table A-9. D9 Opcode Map When ModR/M Byte is Within 00H to BFH *

<table>
<thead>
<tr>
<th>nnn Field of ModR/M Byte</th>
<th>000B</th>
<th>001B</th>
<th>010B</th>
<th>011B</th>
<th>100B</th>
<th>101B</th>
<th>110B</th>
<th>111B</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLD single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FST single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSTP single-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLDENV 14/28 bytes</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLDCW 2 bytes</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSTENV 14/28 bytes</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSTCW 2 bytes</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.

Table A-10 shows the map if the ModR/M byte is outside the range of 00H-BFH. Here, the first digit of the ModR/M byte selects the table row and the second digit selects the column.

#### Table A-10. D9 Opcode Map When ModR/M Byte is Outside 00H to BFH *

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>FLD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>FNOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>FCHS</td>
<td>FABS</td>
<td>FTST</td>
<td>FXAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>F2XM1</td>
<td>FYL2X</td>
<td>FPTAN</td>
<td>FPATAN</td>
<td>FXTRACT</td>
<td>FPREM1</td>
<td>FDECSTP</td>
<td>FINCSTP</td>
</tr>
</tbody>
</table>

**NOTES:**
* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
A.5.2.3  Escape Opcodes with DA as First Byte

Table A-11 and A-12 contain maps for escape instruction opcodes that begin with DAH. Table A-11 shows the map if the ModR/M byte is in the range of 00H-BFH. Here, the value of bits 3-5 (the nnn field in Figure A-1) selects the instruction.

**Table A-11. DA Opcode Map When ModR/M Byte is Within 00H to BFH *

<table>
<thead>
<tr>
<th>nnn Field of ModR/M Byte</th>
<th>000B</th>
<th>001B</th>
<th>010B</th>
<th>011B</th>
<th>100B</th>
<th>101B</th>
<th>110B</th>
<th>111B</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIADD</td>
<td>dword-integer</td>
<td>FIMUL</td>
<td>dword-integer</td>
<td>FICOM</td>
<td>dword-integer</td>
<td>FICOMP</td>
<td>dword-integer</td>
<td>FISUB</td>
</tr>
</tbody>
</table>

**NOTES:**
* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.

Table A-11 shows the map if the ModR/M byte is outside the range of 00H-BFH. Here, the first digit of the ModR/M byte selects the table row and the second digit selects the column.

**Table A-12. DA Opcode Map When ModR/M Byte is Outside 00H to BFH *

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>FCMOVB</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>D</td>
<td>FCMOVBE</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>8</th>
<th>9</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>FCMOVE</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>D</td>
<td>FCMOVU</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>E</td>
<td>FUCOMPP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
**A.5.2.4 Escape Opcodes with DB as First Byte**

Table A-13 and A-14 contain maps for escape instruction opcodes that begin with DBH. Table A-13 shows the map if the ModR/M byte is in the range of 00H-BFH. Here, the value of bits 3-5 (the nnn field in Figure A-1) selects the instruction.

### Table A-13. DB Opcode Map When ModR/M Byte is Within 00H to BFH *

<table>
<thead>
<tr>
<th>nnn Field of ModR/M Byte</th>
<th>000B</th>
<th>001B</th>
<th>010B</th>
<th>011B</th>
<th>100B</th>
<th>101B</th>
<th>110B</th>
<th>111B</th>
</tr>
</thead>
<tbody>
<tr>
<td>FILD</td>
<td>dword-integer</td>
<td>FISTTP</td>
<td>FISTP</td>
<td>FISTTP</td>
<td>dword-integer</td>
<td>extended-real</td>
<td>extended-real</td>
<td></td>
</tr>
<tr>
<td>FISTP</td>
<td>dword-integer</td>
<td>FISTP</td>
<td>dword-integer</td>
<td>FISTP</td>
<td>dword-integer</td>
<td>extended-real</td>
<td>extended-real</td>
<td></td>
</tr>
<tr>
<td>FIST</td>
<td>dword-integer</td>
<td>FISTP</td>
<td>dword-integer</td>
<td>FISTP</td>
<td>dword-integer</td>
<td>extended-real</td>
<td>extended-real</td>
<td></td>
</tr>
<tr>
<td>FISTP</td>
<td>dword-integer</td>
<td>FISTP</td>
<td>dword-integer</td>
<td>FISTP</td>
<td>dword-integer</td>
<td>extended-real</td>
<td>extended-real</td>
<td></td>
</tr>
<tr>
<td>FLDF</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td></td>
</tr>
<tr>
<td>FSTP</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td>extended-real</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.

Table A-14 shows the map if the ModR/M byte is outside the range of 00H-BFH. Here, the first digit of the ModR/M byte selects the table row and the second digit selects the column.

### Table A-14. DB Opcode Map When ModR/M Byte is Outside 00H to BFH *

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>FCMOVNB</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>D</td>
<td>FCMOVNBE</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>E</td>
<td>FCLEX</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
<tr>
<td>F</td>
<td>FCOMI</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
</tr>
</tbody>
</table>

**NOTES:**

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
### A.5.2.5 Escape Opcodes with DC as First Byte

Table A-15 and A-16 contain maps for escape instruction opcodes that begin with DCH. Table A-15 shows the map if the ModR/M byte is in the range of 00H-BFH. Here, the value of bits 3-5 (the nnn field in Figure A-1) selects the instruction.

**Table A-15. DC Opcode Map When ModR/M Byte is Within 00H to BFH *

<table>
<thead>
<tr>
<th>nnn Field of ModR/M Byte (refer to Figure A-1)</th>
<th>000B</th>
<th>001B</th>
<th>010B</th>
<th>011B</th>
<th>100B</th>
<th>101B</th>
<th>110B</th>
<th>111B</th>
</tr>
</thead>
<tbody>
<tr>
<td>FADD double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FMUL double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FCOM double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FCOMP double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSUB double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSUBR double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FDIV double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FDIVR double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.

Table A-16 shows the map if the ModR/M byte is outside the range of 00H-BFH. In this case the first digit of the ModR/M byte selects the table row and the second digit selects the column.

**Table A-16. DC Opcode Map When ModR/M Byte is Outside 00H to BFH *

<table>
<thead>
<tr>
<th>C</th>
<th>FADD</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>ST(0),ST(0)</td>
<td>ST(1),ST(0)</td>
<td>ST(2),ST(0)</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(0)</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(0)</td>
</tr>
<tr>
<td>F</td>
<td></td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(0)</td>
</tr>
</tbody>
</table>

**NOTES:**
* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
### A.5.2.6 Escape Opcodes with DD as First Byte

Table A-17 and A-18 contain maps for escape instruction opcodes that begin with DDH. Table A-17 shows the map if the ModR/M byte is in the range of 00H-BFH. Here, the value of bits 3-5 (the nnn field in Figure A-1) selects the instruction.

**Table A-17. DD Opcode Map When ModR/M Byte is Within 00H to BFH**

<table>
<thead>
<tr>
<th>nnn Field of ModR/M Byte</th>
<th>000B</th>
<th>001B</th>
<th>010B</th>
<th>011B</th>
<th>100B</th>
<th>101B</th>
<th>110B</th>
<th>111B</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLD</td>
<td>double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FISTTP</td>
<td>integer64</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FST</td>
<td>double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSTP</td>
<td>double-real</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FRSTOR</td>
<td>98/108bytes</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSAVE</td>
<td>98/108bytes</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSTSW</td>
<td>2 bytes</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
- * All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.

Table A-18 shows the map if the ModR/M byte is outside the range of 00H-BFH. The first digit of the ModR/M byte selects the table row and the second digit selects the column.

**Table A-18. DD Opcode Map When ModR/M Byte is Outside 00H to BFH**

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>FFREE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>FST</td>
<td>ST(0)</td>
<td>ST(1)</td>
<td>ST(2)</td>
<td>ST(3)</td>
<td>ST(4)</td>
<td>ST(5)</td>
</tr>
<tr>
<td>E</td>
<td>FUCOM</td>
<td>ST(0),ST(0)</td>
<td>ST(1),ST(0)</td>
<td>ST(2),ST(0)</td>
<td>ST(3),ST(0)</td>
<td>ST(4),ST(0)</td>
<td>ST(5),ST(0)</td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
- * All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
## A.5.2.7 Escape Opcodes with DE as First Byte

Table A-19 and A-20 contain opcode maps for escape instruction opcodes that begin with DEH. Table A-19 shows the opcode map if the ModR/M byte is in the range of 00H-BFH. In this case, the value of bits 3-5 (the nnn field in Figure A-1) selects the instruction.

### Table A-19. DE Opcode Map When ModR/M Byte is Within 00H to BFH *

<table>
<thead>
<tr>
<th>nnn Field of ModR/M Byte</th>
<th>00B</th>
<th>01B</th>
<th>010B</th>
<th>011B</th>
<th>10B</th>
<th>11B</th>
<th>101B</th>
<th>110B</th>
<th>111B</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIADD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIMUL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FICOM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FICOMP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FISUB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FISUBR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIDIV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIDIVR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.

Table A-20 shows the opcode map if the ModR/M byte is outside the range of 00H-BFH. The first digit of the ModR/M byte selects the table row and the second digit selects the column.

### Table A-20. DE Opcode Map When ModR/M Byte is Outside 00H to BFH *

<table>
<thead>
<tr>
<th>C</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FADDP</td>
<td>ST(0),ST(0)</td>
<td>ST(1),ST(0)</td>
<td>ST(2),ST(0)</td>
<td>ST(3),ST(0)</td>
<td>ST(4),ST(0)</td>
<td>ST(5),ST(0)</td>
<td>ST(6),ST(0)</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>FSUBRP</td>
<td>ST(0),ST(0)</td>
<td>ST(1),ST(0)</td>
<td>ST(2),ST(0)</td>
<td>ST(3),ST(0)</td>
<td>ST(4),ST(0)</td>
<td>ST(5),ST(0)</td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
### A.5.2.8 Escape Opcodes with DF As First Byte

Table A-21 and A-22 contain the opcode maps for escape instruction opcodes that begin with DFH. Table A-21 shows the opcode map if the ModR/M byte is in the range of 00H-BFH. Here, the value of bits 3-5 (the nnn field in Figure A-1) selects the instruction.

**Table A-21. DF Opcode Map When ModR/M Byte is Within 00H to BFH**

<table>
<thead>
<tr>
<th>nnn Field of ModR/M Byte</th>
<th>00B</th>
<th>001B</th>
<th>010B</th>
<th>011B</th>
<th>100B</th>
<th>101B</th>
<th>110B</th>
<th>111B</th>
</tr>
</thead>
<tbody>
<tr>
<td>FILD</td>
<td>word-integer</td>
<td>FISTTP</td>
<td>word-integer</td>
<td>FISTP</td>
<td>word-integer</td>
<td>FBLD</td>
<td>packed-BCD</td>
<td>FILD</td>
</tr>
</tbody>
</table>

**NOTES:**

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.

Table A-22 shows the opcode map if the ModR/M byte is outside the range of 00H-BFH. The first digit of the ModR/M byte selects the table row and the second digit selects the column.

**Table A-22. DF Opcode Map When ModR/M Byte is Outside 00H to BFH**

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>FSTSW AX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>FCOMIP</td>
<td>ST(0),ST(0)</td>
<td>ST(0),ST(1)</td>
<td>ST(0),ST(2)</td>
<td>ST(0),ST(3)</td>
<td>ST(0),ST(4)</td>
<td>ST(0),ST(5)</td>
<td>ST(0),ST(6)</td>
</tr>
</tbody>
</table>

**NOTES:**

* All blanks in all opcode maps are reserved and must not be used. Do not depend on the operation of undefined or reserved locations.
This appendix provides machine instruction formats and encodings of IA-32 instructions. The first section describes the IA-32 architecture’s machine instruction format. The remaining sections show the formats and encoding of general-purpose, MMX, P6 family, SSE/SSE2/SSE3, x87 FPU instructions, and VMX instructions. Those instruction formats also apply to Intel 64 architecture. Instruction formats used in 64-bit mode are provided as supersets of the above.

### B.1 MACHINE INSTRUCTION FORMAT

All Intel Architecture instructions are encoded using subsets of the general machine instruction format shown in Figure B-1. Each instruction consists of:

- an opcode
- a register and/or address mode specifier consisting of the ModR/M byte and sometimes the scale-index-base (SIB) byte (if required)
- a displacement and an immediate data field (if required)

![Figure B-1. General Machine Instruction Format](image)

The following sections discuss this format.
INSTRUCTION FORMATS AND ENCODINGS

B.1.1 Legacy Prefixes

The legacy prefixes noted in Figure B-1 include 66H, 67H, F2H and F3H. They are optional, except when F2H, F3H and 66H are used in new instruction extensions. Legacy prefixes must be placed before REX prefixes.


B.1.2 REX Prefixes

REX prefixes are a set of 16 opcodes that span one row of the opcode map and occupy entries 40H to 4FH. These opcodes represent valid instructions (INC or DEC) in IA-32 operating modes and in compatibility mode. In 64-bit mode, the same opcodes represent the instruction prefix REX and are not treated as individual instructions.


B.1.3 Opcode Fields

The primary opcode for an instruction is encoded in one to three bytes of the instruction. Within the primary opcode, smaller encoding fields may be defined. These fields vary according to the class of operation being performed.

Almost all instructions that refer to a register and/or memory operand have a register and/or address mode byte following the opcode. This byte, the ModR/M byte, consists of the mod field (2 bits), the reg field (3 bits; this field is sometimes an opcode extension), and the R/M field (3 bits). Certain encodings of the ModR/M byte indicate that a second address mode byte, the SIB byte, must be used.

If the addressing mode specifies a displacement, the displacement value is placed immediately following the ModR/M byte or SIB byte. Possible sizes are 8, 16, or 32 bits. If the instruction specifies an immediate value, the immediate value follows any displacement bytes. The immediate, if specified, is always the last field of the instruction.


B.1.4 Special Fields

Table B-1 lists bit fields that appear in certain instructions, sometimes within the opcode bytes. All of these fields (except the d bit) occur in the general-purpose instruction formats in Table B-13.
B.1.4.1  Reg Field (reg) for Non-64-Bit Modes

The reg field in the ModR/M byte specifies a general-purpose register operand. The group of registers specified is modified by the presence and state of the w bit in an encoding (refer to Section B.1.4.3). Table B-2 shows the encoding of the reg field when the w bit is not present in an encoding; Table B-3 shows the encoding of the reg field when the w bit is present.

### Table B-1. Special Fields Within Instruction Encodings

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Description</th>
<th>Number of Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>reg</td>
<td>General-register specifier (see Table B-4 or B-5)</td>
<td>3</td>
</tr>
<tr>
<td>w</td>
<td>Specifies if data is byte or full-sized, where full-sized is 16 or 32 bits (see Table B-6)</td>
<td>1</td>
</tr>
<tr>
<td>s</td>
<td>Specifies sign extension of an immediate field (see Table B-7)</td>
<td>1</td>
</tr>
<tr>
<td>sreg2</td>
<td>Segment register specifier for CS, SS, DS, ES (see Table B-8)</td>
<td>2</td>
</tr>
<tr>
<td>sreg3</td>
<td>Segment register specifier for CS, SS, DS, ES, FS, GS (see Table B-8)</td>
<td>3</td>
</tr>
<tr>
<td>eee</td>
<td>Specifies a special-purpose (control or debug) register (see Table B-9)</td>
<td>3</td>
</tr>
<tr>
<td>tttn</td>
<td>For conditional instructions, specifies a condition asserted or negated (see Table B-12)</td>
<td>4</td>
</tr>
<tr>
<td>d</td>
<td>Specifies direction of data operation (see Table B-11)</td>
<td>1</td>
</tr>
</tbody>
</table>

### Table B-2. Encoding of reg Field When w Field is Not Present in Instruction

<table>
<thead>
<tr>
<th>reg Field</th>
<th>Register Selected during 16-Bit Data Operations</th>
<th>Register Selected during 32-Bit Data Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>AX</td>
<td>EAX</td>
</tr>
<tr>
<td>001</td>
<td>CX</td>
<td>ECX</td>
</tr>
<tr>
<td>010</td>
<td>DX</td>
<td>EDX</td>
</tr>
<tr>
<td>011</td>
<td>BX</td>
<td>EBX</td>
</tr>
<tr>
<td>100</td>
<td>SP</td>
<td>ESP</td>
</tr>
<tr>
<td>101</td>
<td>BP</td>
<td>EBP</td>
</tr>
<tr>
<td>110</td>
<td>SI</td>
<td>ESI</td>
</tr>
<tr>
<td>111</td>
<td>DI</td>
<td>EDI</td>
</tr>
</tbody>
</table>
INSTRUCTION FORMATS AND ENCODINGS

Table B-3. Encoding of reg Field When w Field is Present in Instruction

<table>
<thead>
<tr>
<th>Function of w Field</th>
<th>Register Specified by reg Field During 16-Bit Data Operations</th>
<th>Register Specified by reg Field During 32-Bit Data Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>reg</td>
<td>When w = 0</td>
<td>When w = 1</td>
</tr>
<tr>
<td>000</td>
<td>AL</td>
<td>AX</td>
</tr>
<tr>
<td>001</td>
<td>CL</td>
<td>CX</td>
</tr>
<tr>
<td>010</td>
<td>DL</td>
<td>DX</td>
</tr>
<tr>
<td>011</td>
<td>BL</td>
<td>BX</td>
</tr>
<tr>
<td>100</td>
<td>AH</td>
<td>SP</td>
</tr>
<tr>
<td>101</td>
<td>CH</td>
<td>BP</td>
</tr>
<tr>
<td>110</td>
<td>DH</td>
<td>SI</td>
</tr>
<tr>
<td>111</td>
<td>BH</td>
<td>DI</td>
</tr>
</tbody>
</table>

B.1.4.2 Reg Field (reg) for 64-Bit Mode

Just like in non-64-bit modes, the reg field in the ModR/M byte specifies a general-purpose register operand. The group of registers specified is modified by the presence of and state of the w bit in an encoding (refer to Section B.1.4.3). Table B-4 shows the encoding of the reg field when the w bit is not present in an encoding; Table B-5 shows the encoding of the reg field when the w bit is present.

Table B-4. Encoding of reg Field When w Field is Not Present in Instruction

<table>
<thead>
<tr>
<th>reg Field</th>
<th>Register Selected during 16-Bit Data Operations</th>
<th>Register Selected during 32-Bit Data Operations</th>
<th>Register Selected during 64-Bit Data Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>AX</td>
<td>EAX</td>
<td>RAX</td>
</tr>
<tr>
<td>001</td>
<td>CX</td>
<td>ECX</td>
<td>RCX</td>
</tr>
<tr>
<td>010</td>
<td>DX</td>
<td>EDX</td>
<td>RDX</td>
</tr>
<tr>
<td>011</td>
<td>BX</td>
<td>EBX</td>
<td>RBX</td>
</tr>
<tr>
<td>100</td>
<td>SP</td>
<td>ESP</td>
<td>RSP</td>
</tr>
<tr>
<td>101</td>
<td>BP</td>
<td>EBP</td>
<td>RBP</td>
</tr>
<tr>
<td>110</td>
<td>SI</td>
<td>ESI</td>
<td>RSI</td>
</tr>
<tr>
<td>111</td>
<td>DI</td>
<td>EDI</td>
<td>RDI</td>
</tr>
</tbody>
</table>
B.1.4.3 Encoding of Operand Size (w) Bit

The current operand-size attribute determines whether the processor is performing 16-bit, 32-bit or 64-bit operations. Within the constraints of the current operand-size attribute, the operand-size bit (w) can be used to indicate operations on 8-bit operands or the full operand size specified with the operand-size attribute. Table B-6 shows the encoding of the w bit depending on the current operand-size attribute.

<table>
<thead>
<tr>
<th>Function of w Field</th>
<th>Register Specified by reg Field During 16-Bit Data Operations</th>
<th>Register Specified by reg Field During 32-Bit Data Operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>reg</td>
<td>When w = 0</td>
<td>When w = 1</td>
</tr>
<tr>
<td>000</td>
<td>AL</td>
<td>AX</td>
</tr>
<tr>
<td>001</td>
<td>CL</td>
<td>CX</td>
</tr>
<tr>
<td>010</td>
<td>DL</td>
<td>DX</td>
</tr>
<tr>
<td>011</td>
<td>BL</td>
<td>BX</td>
</tr>
<tr>
<td>100</td>
<td>AH</td>
<td>SP</td>
</tr>
<tr>
<td>101</td>
<td>CH</td>
<td>BP</td>
</tr>
<tr>
<td>110</td>
<td>DH</td>
<td>SI</td>
</tr>
<tr>
<td>111</td>
<td>BH</td>
<td>DI</td>
</tr>
</tbody>
</table>

NOTES:
1. AH, CH, DH, BH can not be encoded when REX prefix is used. Such an expression defaults to the low byte.

B.1.4.4 Sign-Extend (s) Bit

The sign-extend (s) bit occurs in instructions with immediate data fields that are being extended from 8 bits to 16 or 32 bits. See Table B-7.
INSTRUCTION FORMATS AND ENCODINGS

Table B-7. Encoding of Sign-Extend (s) Bit

<table>
<thead>
<tr>
<th>s</th>
<th>Effect on 8-Bit Immediate Data</th>
<th>Effect on 16- or 32-Bit Immediate Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>1</td>
<td>Sign-extend to fill 16-bit or 32-bit destination</td>
<td>None</td>
</tr>
</tbody>
</table>

B.1.4.5 Segment Register (sreg) Field

When an instruction operates on a segment register, the reg field in the ModR/M byte is called the sreg field and is used to specify the segment register. Table B-8 shows the encoding of the sreg field. This field is sometimes a 2-bit field (sreg2) and other times a 3-bit field (sreg3).

Table B-8. Encoding of the Segment Register (sreg) Field

<table>
<thead>
<tr>
<th>2-Bit sreg2 Field</th>
<th>Segment Register Selected</th>
<th>3-Bit sreg3 Field</th>
<th>Segment Register Selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>ES</td>
<td>000</td>
<td>ES</td>
</tr>
<tr>
<td>01</td>
<td>CS</td>
<td>001</td>
<td>CS</td>
</tr>
<tr>
<td>10</td>
<td>SS</td>
<td>010</td>
<td>SS</td>
</tr>
<tr>
<td>11</td>
<td>DS</td>
<td>011</td>
<td>DS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100</td>
<td>FS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>101</td>
<td>GS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>110</td>
<td>Reserved&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>111</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

NOTES:
1. Do not use reserved encodings.

B.1.4.6 Special-Purpose Register (eee) Field

When control or debug registers are referenced in an instruction they are encoded in the eee field, located in bits 5 through 3 of the ModR/M byte (an alternate encoding of the sreg field). See Table B-9.
For conditional instructions (such as conditional jumps and set on condition), the condition test field (tttn) is encoded for the condition being tested. The ttt part of the field gives the condition to test and the n part indicates whether to use the condition (n = 0) or its negation (n = 1).

- For 1-byte primary opcodes, the tttn field is located in bits 3, 2, 1, and 0 of the opcode byte.
- For 2-byte primary opcodes, the tttn field is located in bits 3, 2, 1, and 0 of the second opcode byte.

Table B-10 shows the encoding of the tttn field.

<table>
<thead>
<tr>
<th>eee</th>
<th>Control Register</th>
<th>Debug Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>CR0</td>
<td>DR0</td>
</tr>
<tr>
<td>001</td>
<td>Reserved$^1$</td>
<td>DR1</td>
</tr>
<tr>
<td>010</td>
<td>CR2</td>
<td>DR2</td>
</tr>
<tr>
<td>011</td>
<td>CR3</td>
<td>DR3</td>
</tr>
<tr>
<td>100</td>
<td>CR4</td>
<td>Reserved</td>
</tr>
<tr>
<td>101</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>110</td>
<td>Reserved</td>
<td>DR6</td>
</tr>
<tr>
<td>111</td>
<td>Reserved</td>
<td>DR7</td>
</tr>
</tbody>
</table>

NOTES:
1. Do not use reserved encodings.
INSTRUCTION FORMATS AND ENCODINGS

Table B-10. Encoding of Conditional Test (tttn) Field

<table>
<thead>
<tr>
<th>tttn</th>
<th>Mnemonic</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>O</td>
<td>Overflow</td>
</tr>
<tr>
<td>0001</td>
<td>NO</td>
<td>No overflow</td>
</tr>
<tr>
<td>0010</td>
<td>B, NAE</td>
<td>Below, Not above or equal</td>
</tr>
<tr>
<td>0011</td>
<td>NB, AE</td>
<td>Not below, Above or equal</td>
</tr>
<tr>
<td>0100</td>
<td>E, Z</td>
<td>Equal, Zero</td>
</tr>
<tr>
<td>0101</td>
<td>NE, NZ</td>
<td>Not equal, Not zero</td>
</tr>
<tr>
<td>0110</td>
<td>BE, NA</td>
<td>Below or equal, Not above</td>
</tr>
<tr>
<td>0111</td>
<td>NBE, A</td>
<td>Not below or equal, Above</td>
</tr>
<tr>
<td>1000</td>
<td>S</td>
<td>Sign</td>
</tr>
<tr>
<td>1001</td>
<td>NS</td>
<td>Not sign</td>
</tr>
<tr>
<td>1010</td>
<td>P, PE</td>
<td>Parity, Parity Even</td>
</tr>
<tr>
<td>1011</td>
<td>NP, PO</td>
<td>Not parity, Parity Odd</td>
</tr>
<tr>
<td>1100</td>
<td>L, NGE</td>
<td>Less than, Not greater than or equal to</td>
</tr>
<tr>
<td>1101</td>
<td>NL, GE</td>
<td>Not less than, Greater than or equal to</td>
</tr>
<tr>
<td>1110</td>
<td>LE, NG</td>
<td>Less than or equal to, Not greater than</td>
</tr>
<tr>
<td>1111</td>
<td>NLE, G</td>
<td>Not less than or equal to, Greater than</td>
</tr>
</tbody>
</table>

B.1.4.8 Direction (d) Bit

In many two-operand instructions, a direction bit (d) indicates which operand is considered the source and which is the destination. See Table B-11.

- When used for integer instructions, the d bit is located at bit 1 of a 1-byte primary opcode. Note that this bit does not appear as the symbol “d” in Table B-13; the actual encoding of the bit as 1 or 0 is given.
- When used for floating-point instructions (in Table B-16), the d bit is shown as bit 2 of the first byte of the primary opcode.

Table B-11. Encoding of Operation Direction (d) Bit

<table>
<thead>
<tr>
<th>d</th>
<th>Source</th>
<th>Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>reg Field</td>
<td>ModR/M or SIB Byte</td>
</tr>
<tr>
<td>1</td>
<td>ModR/M or SIB Byte</td>
<td>reg Field</td>
</tr>
</tbody>
</table>
B.1.5 Other Notes

Table B-12 contains notes on particular encodings. These notes are indicated in the tables shown in the following sections by superscripts.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>A value of 11B in bits 7 and 6 of the ModR/M byte is reserved.</td>
</tr>
<tr>
<td>B</td>
<td>A value of 01B (or 10B) in bits 7 and 6 of the ModR/M byte is reserved.</td>
</tr>
</tbody>
</table>

B.2 General-Purpose Instruction Formats and Encodings for Non-64-Bit Modes

Table B-13 shows machine instruction formats and encodings for general purpose instructions in non-64-bit modes.

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>AAA – ASCII Adjust after Addition</td>
<td>0011 0111</td>
</tr>
<tr>
<td>AAD – ASCII Adjust AX before Division</td>
<td>1101 0101 : 0000 1010</td>
</tr>
<tr>
<td>AAM – ASCII Adjust AX after Multiply</td>
<td>1101 0100 : 0000 1010</td>
</tr>
<tr>
<td>AAS – ASCII Adjust AL after Subtraction</td>
<td>0011 1111</td>
</tr>
<tr>
<td>ADC – ADD with Carry</td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0001 000w : 11 reg1 reg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0001 001w : 11 reg1 reg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0001 001w : mod reg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0001 000w : mod reg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>1000 00sw : 11 010 reg : immediate data</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0001 010w : immediate data</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>1000 00sw : mod 010 r/m : immediate data</td>
</tr>
<tr>
<td>ADD – Add</td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0000 000w : 11 reg1 reg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0000 001w : 11 reg1 reg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0000 001w : mod reg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0000 000w : mod reg r/m</td>
</tr>
</tbody>
</table>
### Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>immediate to register</td>
<td>1000 00sw : 11 000 reg : immediate data</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0000 010w : immediate data</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>1000 00sw : mod 000 r/m : immediate data</td>
</tr>
</tbody>
</table>

**AND - Logical AND**

| register1 to register2 | 0010 000w : 11 reg1 reg2 |
| register2 to register1 | 0010 001w : 11 reg1 reg2 |
| memory to register     | 0010 001w : mod reg r/m |
| register to memory     | 0010 000w : mod reg r/m |
| immediate to register  | 1000 00sw : 11 100 reg : immediate data |
| immediate to AL, AX, or EAX | 0010 010w : immediate data |
| immediate to memory    | 1000 00sw : mod 100 r/m : immediate data |

**ARPL - Adjust RPL Field of Selector**

| from register          | 0110 0011 : 11 reg1 reg2 |
| from memory            | 0110 0011 : mod reg r/m |

**BOUND - Check Array Against Bounds**

| 0110 0010 : modA reg r/m |

**BSF - Bit Scan Forward**

| register1, register2   | 0000 1111 : 1101 1100 : 11 reg1 reg2 |
| memory, register       | 0000 1111 : 1101 1100 : mod reg r/m |

**BSR - Bit Scan Reverse**

| register1, register2   | 0000 1111 : 1101 1101 : 11 reg1 reg2 |
| memory, register       | 0000 1111 : 1101 1101 : mod reg r/m |

**BSWAP - Byte Swap**

| 0000 1111 : 1100 1 reg |

**BT - Bit Test**

| register, immediate   | 0000 1111 : 1011 1010 : 11 100 reg: imm8 data |
| memory, immediate     | 0000 1111 : 1011 1010 : mod 100 r/m : imm8 data |
| register1, register2  | 0000 1111 : 1010 0011 : 11 reg2 reg1 |
| memory, reg           | 0000 1111 : 1010 0011 : mod reg r/m |

**BTC - Bit Test and Complement**


Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register, immediate</td>
<td>0000 1111 : 1011 1010 : 11 111 reg: imm8 data</td>
</tr>
<tr>
<td>memory, immediate</td>
<td>0000 1111 : 1011 1010 : mod 111 r/m : imm8 data</td>
</tr>
<tr>
<td>register1, register2</td>
<td>0000 1111 : 1011 1011 : 11 reg2 reg1</td>
</tr>
<tr>
<td>memory, reg</td>
<td>0000 1111 : 1011 1011 : mod reg r/m</td>
</tr>
</tbody>
</table>

**BTR – Bit Test and Reset**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register, immediate</td>
<td>0000 1111 : 1011 1010 : 11 110 reg: imm8 data</td>
</tr>
<tr>
<td>memory, immediate</td>
<td>0000 1111 : 1011 1010 : mod 110 r/m : imm8 data</td>
</tr>
<tr>
<td>register1, register2</td>
<td>0000 1111 : 1011 1011 : 11 reg2 reg1</td>
</tr>
<tr>
<td>memory, reg</td>
<td>0000 1111 : 1011 0011 : mod reg r/m</td>
</tr>
</tbody>
</table>

**BTS – Bit Test and Set**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register, immediate</td>
<td>0000 1111 : 1011 1010 : 11 101 reg: imm8 data</td>
</tr>
<tr>
<td>memory, immediate</td>
<td>0000 1111 : 1011 1010 : mod 101 r/m : imm8 data</td>
</tr>
<tr>
<td>register1, register2</td>
<td>0000 1111 : 1011 1011 : 11 reg2 reg1</td>
</tr>
<tr>
<td>memory, reg</td>
<td>0000 1111 : 1010 1011 : mod reg r/m</td>
</tr>
</tbody>
</table>

**CALL – Call Procedure (in same segment)**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>direct</td>
<td>1110 1000 : full displacement</td>
</tr>
<tr>
<td>register indirect</td>
<td>1111 1111 : 11 010 reg</td>
</tr>
<tr>
<td>memory indirect</td>
<td>1111 1111 : mod 010 r/m</td>
</tr>
</tbody>
</table>

**CALL – Call Procedure (in other segment)**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>direct</td>
<td>1001 1010 : unsigned full offset, selector</td>
</tr>
<tr>
<td>indirect</td>
<td>1111 1111 : mod 011 r/m</td>
</tr>
</tbody>
</table>

**CBW – Convert Byte to Word**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1001 1000</td>
</tr>
</tbody>
</table>

**CDQ – Convert Doubleword to Qword**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1001 1001</td>
</tr>
</tbody>
</table>

**CLC – Clear Carry Flag**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1111 1000</td>
</tr>
</tbody>
</table>

**CLD – Clear Direction Flag**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1111 1100</td>
</tr>
</tbody>
</table>
### Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CLI - Clear Interrupt Flag</strong></td>
<td>1111 1010</td>
</tr>
<tr>
<td><strong>CLTS - Clear Task-Switched Flag in CR0</strong></td>
<td>0000 1111 : 0000 0110</td>
</tr>
<tr>
<td><strong>CMC - Complement Carry Flag</strong></td>
<td>1111 0101</td>
</tr>
<tr>
<td><strong>CMP - Compare Two Operands</strong></td>
<td></td>
</tr>
<tr>
<td>register1 with register2</td>
<td>0011 100w : 11 reg1 reg2</td>
</tr>
<tr>
<td>register2 with register1</td>
<td>0011 101w : 11 reg1 reg2</td>
</tr>
<tr>
<td>memory with register</td>
<td>0011 100w : mod reg r/m</td>
</tr>
<tr>
<td>register with memory</td>
<td>0011 101w : mod reg r/m</td>
</tr>
<tr>
<td>immediate with register</td>
<td>1000 00sw : 11 111 reg : immediate data</td>
</tr>
<tr>
<td>immediate with AL, AX, or EAX</td>
<td>0011 110w : immediate data</td>
</tr>
<tr>
<td>immediate with memory</td>
<td>1000 00sw : mod 111 r/m : immediate data</td>
</tr>
<tr>
<td><strong>CMPS/CMPSB/CMPSW/CMPSD - Compare String Operands</strong></td>
<td>1010 011w</td>
</tr>
<tr>
<td><strong>CMPXCHG - Compare and Exchange</strong></td>
<td></td>
</tr>
<tr>
<td>register1, register2</td>
<td>0000 1111 : 1011 000w : 11 reg2 reg1</td>
</tr>
<tr>
<td>memory, register</td>
<td>0000 1111 : 1011 000w : mod reg r/m</td>
</tr>
<tr>
<td><strong>CPUID - CPU Identification</strong></td>
<td>0000 1111 : 1010 0010</td>
</tr>
<tr>
<td><strong>CWD - Convert Word to Doubleword</strong></td>
<td>1001 1001</td>
</tr>
<tr>
<td><strong>CWDE - Convert Word to Doubleword</strong></td>
<td>1001 1000</td>
</tr>
<tr>
<td><strong>DAA - Decimal Adjust AL after Addition</strong></td>
<td>0010 0111</td>
</tr>
<tr>
<td><strong>DAS - Decimal Adjust AL after Subtraction</strong></td>
<td>0010 1111</td>
</tr>
<tr>
<td><strong>DEC - Decrement by 1</strong></td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>1111 111w : 11 001 reg</td>
</tr>
<tr>
<td>register (alternate encoding)</td>
<td>0100 1 reg</td>
</tr>
<tr>
<td>memory</td>
<td>1111 111w : mod 001 r/m</td>
</tr>
<tr>
<td><strong>DIV - Unsigned Divide</strong></td>
<td></td>
</tr>
<tr>
<td>AL, AX, or EAX by register</td>
<td>1111 011w : 11 110 reg</td>
</tr>
<tr>
<td>AL, AX, or EAX by memory</td>
<td>1111 011w : mod 110 r/m</td>
</tr>
<tr>
<td><strong>HLT - Halt</strong></td>
<td>1111 0100</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------</td>
<td>----------</td>
</tr>
<tr>
<td><strong>IDIV – Signed Divide</strong></td>
<td></td>
</tr>
<tr>
<td>AL, AX, or EAX by register</td>
<td>1111 011w : 11 111 reg</td>
</tr>
<tr>
<td>AL, AX, or EAX by memory</td>
<td>1111 011w : mod 111 r/m</td>
</tr>
<tr>
<td><strong>IMUL – Signed Multiply</strong></td>
<td></td>
</tr>
<tr>
<td>AL, AX, or EAX with register</td>
<td>1111 011w : 11 101 reg</td>
</tr>
<tr>
<td>AL, AX, or EAX with memory</td>
<td>1111 011w : mod 101 reg</td>
</tr>
<tr>
<td>register1 with register2</td>
<td>0000 1111 : 1010 1111 : 11 : reg1 reg2</td>
</tr>
<tr>
<td>register with memory</td>
<td>0000 1111 : 1010 1111 : mod reg r/m</td>
</tr>
<tr>
<td>register1 with immediate to register2</td>
<td>0110 10s1 : 11 reg1 reg2 : immediate data</td>
</tr>
<tr>
<td>memory with immediate to register</td>
<td>0110 10s1 : mod reg r/m : immediate data</td>
</tr>
<tr>
<td><strong>IN – Input From Port</strong></td>
<td></td>
</tr>
<tr>
<td>fixed port</td>
<td>1110 010w : port number</td>
</tr>
<tr>
<td>variable port</td>
<td>1110 110w</td>
</tr>
<tr>
<td><strong>INC – Increment by 1</strong></td>
<td></td>
</tr>
<tr>
<td>reg</td>
<td>1111 111w : 11 000 reg</td>
</tr>
<tr>
<td>reg (alternate encoding)</td>
<td>0100 0 reg</td>
</tr>
<tr>
<td>memory</td>
<td>1111 111w : mod 000 r/m</td>
</tr>
<tr>
<td><strong>INS – Input from DX Port</strong></td>
<td>0110 110w</td>
</tr>
<tr>
<td><strong>INT n – Interrupt Type n</strong></td>
<td>1100 1101 : type</td>
</tr>
<tr>
<td><strong>INT – Single-Step Interrupt 3</strong></td>
<td>1100 1100</td>
</tr>
<tr>
<td><strong>INTO – Interrupt 4 on Overflow</strong></td>
<td>1100 1110</td>
</tr>
<tr>
<td><strong>INVD – Invalidate Cache</strong></td>
<td>0000 1111 : 0000 1000</td>
</tr>
<tr>
<td><strong>INVLPG – Invalidate TLB Entry</strong></td>
<td>0000 1111 : 0000 0001 : mod 111 r/m</td>
</tr>
<tr>
<td><strong>INVPIDC – Invalidate Process-Context Identifier</strong></td>
<td>0110 0110 : 0000 1111 : 0011 1000 : 1000</td>
</tr>
<tr>
<td><strong>IRET/IRETD – Interrupt Return</strong></td>
<td>1100 1111</td>
</tr>
<tr>
<td><strong>Jcc – Jump if Condition is Met</strong></td>
<td></td>
</tr>
<tr>
<td>8-bit displacement</td>
<td>0111 tttn : 8-bit displacement</td>
</tr>
<tr>
<td>full displacement</td>
<td>0000 1111 : 1000 tttn : full displacement</td>
</tr>
</tbody>
</table>
## Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>JCXZ/JECXZ – Jump on CX/ECX Zero Address-size prefix differentiates Jcxz and JECXZ</td>
<td>1110 0011 : 8-bit displacement</td>
</tr>
<tr>
<td>JMP – Unconditional Jump (to same segment)</td>
<td></td>
</tr>
<tr>
<td>short</td>
<td>1110 1011 : 8-bit displacement</td>
</tr>
<tr>
<td>direct</td>
<td>1110 1001 : full displacement</td>
</tr>
<tr>
<td>register indirect</td>
<td>1111 1111 : 11 100 reg</td>
</tr>
<tr>
<td>memory indirect</td>
<td>1111 1111 : mod 100 r/m</td>
</tr>
<tr>
<td>JMP – Unconditional Jump (to other segment)</td>
<td></td>
</tr>
<tr>
<td>direct intersegment</td>
<td>1110 1010 : unsigned full offset, selector</td>
</tr>
<tr>
<td>indirect intersegment</td>
<td>1111 1111 : mod 101 r/m</td>
</tr>
<tr>
<td>LAHF – Load Flags into AHRegister</td>
<td>1001 1111</td>
</tr>
<tr>
<td>LAR – Load Access Rights Byte</td>
<td></td>
</tr>
<tr>
<td>from register</td>
<td>0000 1111 : 0000 0010 : 11 reg1 reg2</td>
</tr>
<tr>
<td>from memory</td>
<td>0000 1111 : 0000 0010 : mod reg r/m</td>
</tr>
<tr>
<td>LDS – Load Pointer to DS</td>
<td>1100 0101 : modA,B reg r/m</td>
</tr>
<tr>
<td>LEA – Load Effective Address</td>
<td>1000 1101 : modA reg r/m</td>
</tr>
<tr>
<td>LEAVE – High Level Procedure Exit</td>
<td>1100 1001</td>
</tr>
<tr>
<td>LES – Load Pointer to ES</td>
<td>1100 0100 : modA,B reg r/m</td>
</tr>
<tr>
<td>LFS – Load Pointer to FS</td>
<td>0000 1111 : 1011 0100 : modA,B reg r/m</td>
</tr>
<tr>
<td>LGDT – Load Global Descriptor Table Register</td>
<td>0000 1111 : 0000 0001 : modA 010 r/m</td>
</tr>
<tr>
<td>LGS – Load Pointer to GS</td>
<td>0000 1111 : 1011 0101 : modA reg r/m</td>
</tr>
<tr>
<td>LIDT – Load Interrupt Descriptor Table Register</td>
<td>0000 1111 : 0000 0001 : modA 011 r/m</td>
</tr>
<tr>
<td>LLDT – Load Local Descriptor Table Register</td>
<td></td>
</tr>
<tr>
<td>LDTR from register</td>
<td>0000 1111 : 0000 0000 : 11 010 reg</td>
</tr>
<tr>
<td>LDTR from memory</td>
<td>0000 1111 : 0000 0000 : mod 010 r/m</td>
</tr>
<tr>
<td>LMSW – Load Machine Status Word</td>
<td></td>
</tr>
<tr>
<td>from register</td>
<td>0000 1111 : 0000 0001 : 11 110 reg</td>
</tr>
<tr>
<td>from memory</td>
<td>0000 1111 : 0000 0001 : mod 110 r/m</td>
</tr>
<tr>
<td>LOCK – Assert LOCK# Signal Prefix</td>
<td>1111 0000</td>
</tr>
</tbody>
</table>
### INSTRUCTION FORMATS AND ENCODINGS

Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>LODS/LODSB/LODSW/LODSD - Load String Operand</strong></td>
<td>1010 110w</td>
</tr>
<tr>
<td><strong>LOOP - Loop Count</strong></td>
<td>1110 0010 : 8-bit displacement</td>
</tr>
<tr>
<td><strong>LOOPZ/LOOPE - Loop Count while Zero/Equal</strong></td>
<td>1110 0001 : 8-bit displacement</td>
</tr>
<tr>
<td><strong>LOOPNZ/LOOPNE - Loop Count while not Zero/Equal</strong></td>
<td>1110 0000 : 8-bit displacement</td>
</tr>
<tr>
<td><strong>LSL - Load Segment Limit</strong></td>
<td>0000 1111 : 0000 0011 : 11 reg1 reg2</td>
</tr>
<tr>
<td></td>
<td>0000 1111 : 0000 0011 : mod reg r/m</td>
</tr>
<tr>
<td><strong>LSS - Load Pointer to SS</strong></td>
<td>0000 1111 : 1011 0010 : modA reg r/m</td>
</tr>
<tr>
<td><strong>LTR - Load Task Register</strong></td>
<td>0000 1111 : 0000 0000 : 11 011 reg</td>
</tr>
<tr>
<td></td>
<td>0000 1111 : 0000 0000 : mod 011 r/m</td>
</tr>
<tr>
<td><strong>MOV - Move Data</strong></td>
<td>1000 100w : 11 reg1 reg2</td>
</tr>
<tr>
<td>register1 to register2</td>
<td>1000 101w : 11 reg1 reg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>1000 101w : mod reg r/m</td>
</tr>
<tr>
<td>memory to reg</td>
<td>1000 101w : mod reg r/m</td>
</tr>
<tr>
<td>reg to memory</td>
<td>1100 011w : 11 000 reg : immediate data</td>
</tr>
<tr>
<td>immediate to register</td>
<td>1100 011w : 11 000 reg : immediate data</td>
</tr>
<tr>
<td>immediate to register (alternate encoding)</td>
<td>1011 w reg : immediate data</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>1100 011w : mod 000 r/m : immediate data</td>
</tr>
<tr>
<td>memory to AL, AX, or EAX</td>
<td>1010 000w : full displacement</td>
</tr>
<tr>
<td>AL, AX, or EAX to memory</td>
<td>1010 001w : full displacement</td>
</tr>
<tr>
<td><strong>MOV - Move to/from Control Registers</strong></td>
<td>0000 1111 : 0010 0010 : 11 000 reg</td>
</tr>
<tr>
<td>CR0 from register</td>
<td>0000 1111 : 0010 0010 : 11 010reg</td>
</tr>
<tr>
<td>CR2 from register</td>
<td>0000 1111 : 0010 0010 : 11 011 reg</td>
</tr>
<tr>
<td>CR3 from register</td>
<td>0000 1111 : 0010 0010 : 11 100 reg</td>
</tr>
<tr>
<td>CR4 from register</td>
<td>0000 1111 : 0010 0010 : 11 100 reg</td>
</tr>
<tr>
<td>register from CR0-CR4</td>
<td>0000 1111 : 0010 0000 : 11 eee reg</td>
</tr>
<tr>
<td><strong>MOV - Move to/from Debug Registers</strong></td>
<td></td>
</tr>
</tbody>
</table>
### Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>DR0-DR3 from register</td>
<td>0000 1111 : 0010 0011 : 11 eee reg</td>
</tr>
<tr>
<td>DR4-DR5 from register</td>
<td>0000 1111 : 0010 0011 : 11 eee reg</td>
</tr>
<tr>
<td>DR6-DR7 from register</td>
<td>0000 1111 : 0010 0011 : 11 eee reg</td>
</tr>
<tr>
<td>register from DR6-DR7</td>
<td>0000 1111 : 0010 0001 : 11 eee reg</td>
</tr>
<tr>
<td>register from DR4-DR5</td>
<td>0000 1111 : 0010 0001 : 11 eee reg</td>
</tr>
<tr>
<td>register from DR0-DR3</td>
<td>0000 1111 : 0010 0001 : 11 eee reg</td>
</tr>
<tr>
<td><strong>MOV – Move to/from Segment Registers</strong></td>
<td></td>
</tr>
<tr>
<td>register to segment register</td>
<td>1000 1110 : 11 sreg3 reg</td>
</tr>
<tr>
<td>register to SS</td>
<td>1000 1110 : 11 sreg3 reg</td>
</tr>
<tr>
<td>memory to segment reg</td>
<td>1000 1110 : mod sreg3 r/m</td>
</tr>
<tr>
<td>memory to SS</td>
<td>1000 1110 : mod sreg3 r/m</td>
</tr>
<tr>
<td>segment register to register</td>
<td>1000 1100 : 11 sreg3 reg</td>
</tr>
<tr>
<td>segment register to memory</td>
<td>1000 1100 : mod sreg3 r/m</td>
</tr>
<tr>
<td><strong>MOVBE – Move data after swapping bytes</strong></td>
<td></td>
</tr>
<tr>
<td>memory to register</td>
<td>0000 1111 : 0011 1000:1111 0000 : mod reg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0000 1111 : 0011 1000:1111 0001 : mod reg r/m</td>
</tr>
<tr>
<td><strong>MOVS/MOVSB/MOVSW/MOVSD – Move Data from String to String</strong></td>
<td>1010 010w</td>
</tr>
<tr>
<td><strong>MOVSX – Move with Sign-Extend</strong></td>
<td>0000 1111 : 1011 111w : mod reg r/m</td>
</tr>
<tr>
<td><strong>MOVZX – Move with Zero-Extend</strong></td>
<td>0000 1111 : 1011 011w : 11 reg1 reg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0000 1111 : 1011 011w : mod reg r/m</td>
</tr>
<tr>
<td><strong>MUL – Unsigned Multiply</strong></td>
<td></td>
</tr>
<tr>
<td>AL, AX, or EAX with register</td>
<td>1111 011w : 11 100 reg</td>
</tr>
<tr>
<td>AL, AX, or EAX with memory</td>
<td>1111 011w : mod 100 r/m</td>
</tr>
<tr>
<td><strong>NEG – Two’s Complement Negation</strong></td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>1111 011w : 11 011 reg</td>
</tr>
<tr>
<td>memory</td>
<td>1111 011w : mod 011 r/m</td>
</tr>
</tbody>
</table>
### Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NOP – No Operation</strong></td>
<td>1001 0000</td>
</tr>
<tr>
<td><strong>NOP – Multi-byte No Operation</strong>&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>0000 1111 0001 1111: 11 000 reg</td>
</tr>
<tr>
<td>memory</td>
<td>0000 1111 0001 1111: mod 000 r/m</td>
</tr>
<tr>
<td><strong>NOT – One’s Complement Negation</strong></td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>1111 011w: 11 010 reg</td>
</tr>
<tr>
<td>memory</td>
<td>1111 011w: mod 010 r/m</td>
</tr>
<tr>
<td><strong>OR – Logical Inclusive OR</strong></td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0000 100w: 11 reg1 reg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0000 101w: 11 reg1 reg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0000 101w: mod reg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0000 100w: mod reg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>1000 00sw: 11 001 reg: immediate data</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0000 110w: immediate data</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>1000 00sw: mod 001 r/m: immediate data</td>
</tr>
<tr>
<td><strong>OUT – Output to Port</strong></td>
<td></td>
</tr>
<tr>
<td>fixed port</td>
<td>1110 011w: port number</td>
</tr>
<tr>
<td>variable port</td>
<td>1110 111w</td>
</tr>
<tr>
<td><strong>OUTS – Output to DX Port</strong></td>
<td>0110 111w</td>
</tr>
<tr>
<td><strong>POP – Pop a Word from the Stack</strong></td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>1000 1111: 11 000 reg</td>
</tr>
<tr>
<td>register (alternate encoding)</td>
<td>0101 1 reg</td>
</tr>
<tr>
<td>memory</td>
<td>1000 1111: mod 000 r/m</td>
</tr>
<tr>
<td><strong>POP – Pop a Segment Register from the Stack</strong>&lt;sup&gt;2&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>segment register DS, ES</td>
<td>000 sreg2 111</td>
</tr>
<tr>
<td>segment register SS</td>
<td>000 sreg2 111</td>
</tr>
<tr>
<td>segment register FS, GS</td>
<td>0000 1111: 10 sreg3 001</td>
</tr>
<tr>
<td><strong>POPA/POPAD – Pop All General Registers</strong></td>
<td>0110 0001</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>POPF/POPFD – Pop Stack into FLAGS or EFLAGS Register</td>
<td>1001 1101</td>
</tr>
<tr>
<td>PUSH – Push Operand onto the Stack</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>1111 1111 : 11 110 reg</td>
</tr>
<tr>
<td>register (alternate encoding)</td>
<td>0101 0 reg</td>
</tr>
<tr>
<td>memory</td>
<td>1111 1111 : mod 110 r/m</td>
</tr>
<tr>
<td>immediate</td>
<td>0110 10s0 : immediate data</td>
</tr>
<tr>
<td>PUSH – Push Segment Register onto the Stack</td>
<td>21</td>
</tr>
<tr>
<td>segment register CS,DS,ES,SS</td>
<td>000 sreg2 110</td>
</tr>
<tr>
<td>segment register FS,GS</td>
<td>000 01111 : 10 sreg3 000</td>
</tr>
<tr>
<td>PUSHA/PUSHAD – Push All General Registers</td>
<td>0110 0000</td>
</tr>
<tr>
<td>PUSHF/PUSHF – Push Flags Register onto the Stack</td>
<td>1001 1100</td>
</tr>
<tr>
<td>RCL – Rotate thru Carry Left</td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>1101 000w : 11 010 reg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>1101 000w : mod 010 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>1101 001w : 11 010 reg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>1101 001w : mod 010 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>1100 000w : 11 010 reg : imm8 data</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>1100 000w : mod 010 r/m : imm8 data</td>
</tr>
<tr>
<td>RCR – Rotate thru Carry Right</td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>1101 000w : 11 011 reg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>1101 000w : mod 011 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>1101 001w : 11 011 reg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>1101 001w : mod 011 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>1100 000w : 11 011 reg : imm8 data</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>1100 000w : mod 011 r/m : imm8 data</td>
</tr>
<tr>
<td>RDMSR – Read from Model-Specific Register</td>
<td>0000 1111 : 0011 0010</td>
</tr>
</tbody>
</table>
### Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDPMC – Read Performance Monitoring Counters</td>
<td>0000 1111 : 0011 0011</td>
</tr>
<tr>
<td>RDTSC – Read Time-Stamp Counter</td>
<td>0000 1111 : 0011 0001</td>
</tr>
<tr>
<td>RDTSCP – Read Time-Stamp Counter and Processor ID</td>
<td>0000 1111 : 0000 0001 : 1111 1001</td>
</tr>
<tr>
<td>REP INS – Input String</td>
<td>1111 0011 : 0110 110w</td>
</tr>
<tr>
<td>REP LODS – Load String</td>
<td>1111 0011 : 1010 110w</td>
</tr>
<tr>
<td>REP MOVS – Move String</td>
<td>1111 0011 : 1010 010w</td>
</tr>
<tr>
<td>REP OUTS – Output String</td>
<td>1111 0011 : 0110 111w</td>
</tr>
<tr>
<td>REP STOS – Store String</td>
<td>1111 0011 : 1010 101w</td>
</tr>
<tr>
<td>REP CMPS – Compare String</td>
<td>1111 0011 : 1010 011w</td>
</tr>
<tr>
<td>REP SCAS – Scan String</td>
<td>1111 0011 : 1010 111w</td>
</tr>
<tr>
<td>REPNE CMPS – Compare String</td>
<td>1111 0010 : 1010 011w</td>
</tr>
<tr>
<td>REPNE SCAS – Scan String</td>
<td>1111 0010 : 1010 111w</td>
</tr>
<tr>
<td>RET – Return from Procedure (to same segment)</td>
<td></td>
</tr>
<tr>
<td>no argument</td>
<td>1100 001</td>
</tr>
<tr>
<td>adding immediate to SP</td>
<td>1100 0010 : 16-bit displacement</td>
</tr>
<tr>
<td>RET – Return from Procedure (to other segment)</td>
<td></td>
</tr>
<tr>
<td>intersegment</td>
<td>1100 101</td>
</tr>
<tr>
<td>adding immediate to SP</td>
<td>1100 1010 : 16-bit displacement</td>
</tr>
<tr>
<td>ROL – Rotate Left</td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>1101 000w : 11 000 reg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>1101 000w : mod 000 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>1101 001w : 11 000 reg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>1101 001w : mod 000 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>1100 000w : 11 000 reg : imm8 data</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>1100 000w : mod 000 r/m : imm8 data</td>
</tr>
<tr>
<td>ROR – Rotate Right</td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>1101 000w : 11 001 reg</td>
</tr>
</tbody>
</table>
## Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory by 1</td>
<td>1101 000w : mod 001 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>1101 001w : 11 001 reg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>1101 001w : mod 001 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>1100 000w : 11 001 reg : imm8 data</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>1100 000w : mod 001 r/m : imm8 data</td>
</tr>
<tr>
<td><strong>RSM – Resume from System Management Mode</strong></td>
<td>0000 1111 : 1010 1010</td>
</tr>
<tr>
<td><strong>SAHF – Store AH into Flags</strong></td>
<td>1001 1110</td>
</tr>
<tr>
<td><strong>SAL – Shift Arithmetic Left</strong></td>
<td>same instruction as SHL</td>
</tr>
<tr>
<td><strong>SAR – Shift Arithmetic Right</strong></td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>1101 000w : 11 111 reg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>1101 000w : mod 111 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>1101 001w : 11 111 reg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>1101 001w : mod 111 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>1100 000w : 11 111 reg : imm8 data</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>1100 000w : mod 111 r/m : imm8 data</td>
</tr>
<tr>
<td><strong>SBB – Integer Subtraction with Borrow</strong></td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0001 100w : 11 reg1 reg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0001 101w : 11 reg1 reg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0001 101w : mod reg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0001 100w : mod reg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>1000 00sw : 11 011 reg : immediate data</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0001 110w : immediate data</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>1000 00sw : mod 011 r/m : immediate data</td>
</tr>
<tr>
<td><strong>SCAS/SCASB/SCASW/SCASD – Scan String</strong></td>
<td>1010 111w</td>
</tr>
<tr>
<td><strong>SETcc – Byte Set on Condition</strong></td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>0000 1111 : 1001 ttn : 11 000 reg</td>
</tr>
<tr>
<td>memory</td>
<td>0000 1111 : 1001 ttn : mod 000 r/m</td>
</tr>
<tr>
<td><strong>SGDT – Store Global Descriptor Table Register</strong></td>
<td>0000 1111 : 0000 0001 : modA 000 r/m</td>
</tr>
</tbody>
</table>
### Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SHL – Shift Left</strong></td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>1101 000w : 11 100 reg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>1101 000w : mod 100 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>1101 001w : 11 100 reg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>1101 001w : mod 100 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>1100 000w : 11 100 reg : imm8 data</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>1100 000w : mod 100 r/m : imm8 data</td>
</tr>
<tr>
<td><strong>SHLD – Double Precision Shift Left</strong></td>
<td></td>
</tr>
<tr>
<td>register by immediate count</td>
<td>0000 1111 : 1010 0100 : 11 reg2 reg1 : imm8</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0000 1111 : 1010 0100 : mod reg r/m : imm8</td>
</tr>
<tr>
<td>register by CL</td>
<td>0000 1111 : 1010 0101 : 11 reg2 reg1</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0000 1111 : 1010 0101 : mod reg r/m</td>
</tr>
<tr>
<td><strong>SHR – Shift Right</strong></td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>1101 000w : 11 101 reg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>1101 000w : mod 101 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>1101 001w : 11 101 reg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>1101 001w : mod 101 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>1100 000w : 11 101 reg : imm8 data</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>1100 000w : mod 101 r/m : imm8 data</td>
</tr>
<tr>
<td><strong>SHRD – Double Precision Shift Right</strong></td>
<td></td>
</tr>
<tr>
<td>register by immediate count</td>
<td>0000 1111 : 1010 1100 : 11 reg2 reg1 : imm8</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0000 1111 : 1010 1100 : mod reg r/m : imm8</td>
</tr>
<tr>
<td>register by CL</td>
<td>0000 1111 : 1010 1101 : 11 reg2 reg1</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0000 1111 : 1010 1101 : mod reg r/m</td>
</tr>
<tr>
<td><strong>SIDT – Store Interrupt Descriptor Table Register</strong></td>
<td></td>
</tr>
<tr>
<td>to register</td>
<td>0000 1111 : 0000 0000 : 11 000 reg</td>
</tr>
<tr>
<td>to memory</td>
<td>0000 1111 : 0000 0000 : mod 000 r/m</td>
</tr>
<tr>
<td><strong>SLDT – Store Local Descriptor Table Register</strong></td>
<td></td>
</tr>
<tr>
<td><strong>SMSW – Store Machine Status Word</strong></td>
<td></td>
</tr>
</tbody>
</table>
### Table B-13. General Purpose Instruction Formats and Encodings for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>to register</td>
<td>0000 1111 : 0000 0001 : 11 100 reg</td>
</tr>
<tr>
<td>to memory</td>
<td>0000 1111 : 0000 0001 : mod 100 r/m</td>
</tr>
<tr>
<td><strong>STC – Set Carry Flag</strong></td>
<td>1111 1001</td>
</tr>
<tr>
<td><strong>STD – Set Direction Flag</strong></td>
<td>1111 1101</td>
</tr>
<tr>
<td><strong>STI – Set Interrupt Flag</strong></td>
<td>1111 1011</td>
</tr>
<tr>
<td><strong>STOS/STOSB/STOSw/STOSD – Store String Data</strong></td>
<td>1010 101w</td>
</tr>
<tr>
<td>STR – Store Task Register</td>
<td>to register 0000 1111 : 0000 0000 : 11 001 reg to memory 0000 1111 : 0000 0000 : mod 001 r/m</td>
</tr>
<tr>
<td><strong>SUB – Integer Subtraction</strong></td>
<td>register1 to register2 0010 100w : 11 reg1 reg2 register2 to register1 0010 101w : 11 reg1 reg2 memory to register 0010 101w : mod reg r/m register to memory 0010 100w : mod reg r/m immediate to register 1000 00sw : 11 101 reg : immediate data immediate to AL, AX, or EAX 0010 110w : immediate data immediate to memory 1000 00sw : mod 101 r/m : immediate data</td>
</tr>
<tr>
<td><strong>TEST – Logical Compare</strong></td>
<td>register1 and register2 1000 010w : 11 reg1 reg2 memory and register 1000 010w : mod reg r/m immediate and register 1111 011w : 11 000 reg : immediate data immediate and AL, AX, or EAX 1010 100w : immediate data immediate and memory 1111 011w : mod 000 r/m : immediate data</td>
</tr>
<tr>
<td><strong>UD2 – Undefined instruction</strong></td>
<td>0000 FFFF : 0000 1011</td>
</tr>
<tr>
<td><strong>VERR – Verify a Segment for Reading</strong></td>
<td>register 0000 1111 : 0000 0000 : 11 100 reg memory 0000 1111 : 0000 0000 : mod 100 r/m</td>
</tr>
<tr>
<td><strong>VERW – Verify a Segment for Writing</strong></td>
<td>register 0000 1111 : 0000 0000 : 11 101 reg</td>
</tr>
</tbody>
</table>
## Table B-13. General Purpose Instruction Formats and Encodings
### for Non-64-Bit Modes (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory</td>
<td>0000 1111 : 0000 0000 : mod 101 r/m</td>
</tr>
<tr>
<td>WAIT – Wait</td>
<td>1001 1011</td>
</tr>
<tr>
<td>WBINVD – Writeback and Invalidate Data Cache</td>
<td>0000 1111 : 0000 1001</td>
</tr>
<tr>
<td>WRMSR – Write to Model-Specific Register</td>
<td>0000 1111 : 0011 0000</td>
</tr>
<tr>
<td>XADD – Exchange and Add</td>
<td></td>
</tr>
<tr>
<td>register1, register2</td>
<td>0000 1111 : 1100 0000w : 11 reg2 reg1</td>
</tr>
<tr>
<td>memory, reg</td>
<td>0000 1111 : 1100 0000w : mod reg r/m</td>
</tr>
<tr>
<td>XCHG – Exchange Register/Memory with Register</td>
<td></td>
</tr>
<tr>
<td>register1 with register2</td>
<td>1000 0111w : 11 reg1 reg2</td>
</tr>
<tr>
<td>AX or EAX with reg</td>
<td>1001 0 reg</td>
</tr>
<tr>
<td>memory with reg</td>
<td>1000 0111w : mod reg r/m</td>
</tr>
<tr>
<td>XLAT/XLATB – Table Look-up Translation</td>
<td>1101 0111</td>
</tr>
<tr>
<td>XOR – Logical Exclusive OR</td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0011 000w : 11 reg1 reg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0011 001w : 11 reg1 reg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0011 001w : mod reg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0011 000w : mod reg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>1000 00sw : 11 110 reg : immediate data</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0011 010w : immediate data</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>1000 00sw : mod 110 r/m : immediate data</td>
</tr>
<tr>
<td>Prefix Bytes</td>
<td></td>
</tr>
<tr>
<td>address size</td>
<td>0110 0111</td>
</tr>
<tr>
<td>LOCK</td>
<td>1111 0000</td>
</tr>
<tr>
<td>operand size</td>
<td>0110 0110</td>
</tr>
<tr>
<td>CS segment override</td>
<td>0010 1110</td>
</tr>
<tr>
<td>DS segment override</td>
<td>0011 1110</td>
</tr>
<tr>
<td>ES segment override</td>
<td>0010 0110</td>
</tr>
<tr>
<td>FS segment override</td>
<td>0110 0100</td>
</tr>
</tbody>
</table>
B.2.1 General Purpose Instruction Formats and Encodings for 64-Bit Mode

Table B-15 shows machine instruction formats and encodings for general purpose instructions in 64-bit mode.

Table B-14. Special Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>If the value of REX.W. is 1, it overrides the presence of 66H.</td>
</tr>
<tr>
<td>w</td>
<td>The value of bit W. in REX is has no effect.</td>
</tr>
</tbody>
</table>

Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC – ADD with Carry</td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0100 0R0B : 0001 000w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1 to qwordregister2</td>
<td>0100 1R0B : 0001 0001 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0R0B : 0001 001w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1 to qwordregister2</td>
<td>0100 1R0B : 0001 0011 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0100 ORXB : 0001 001w : mod reg r/m</td>
</tr>
<tr>
<td>memory to qwordregister</td>
<td>0100 1RXB : 0001 0011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0100 ORXB : 0001 000w : mod reg r/m</td>
</tr>
<tr>
<td>qwordregister to memory</td>
<td>0100 1RXB : 0001 0001 : mod qwordreg r/m</td>
</tr>
</tbody>
</table>

NOTES:
1. The multi-byte NOP instruction does not alter the content of the register and will not issue a memory operation.
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>immediate to register</td>
<td>0100 0000B : 1000 00sw : 11 010 reg : immediate</td>
</tr>
<tr>
<td>immediate to qwordregister</td>
<td>0100 100B : 1000 0001 : 11 010 qwordreg : imm32</td>
</tr>
<tr>
<td>immediate to qwordregister</td>
<td>0100 1ROB : 1000 0011 : 11 010 qwordreg : imm8</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0001 010w : immediate data</td>
</tr>
<tr>
<td>immediate to RAX</td>
<td>0100 1000 : 0000 0101 : imm32</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>0100 0XB : 1000 00sw : mod 010 r/m : immediate</td>
</tr>
<tr>
<td>immediate32 to memory64</td>
<td>0100 10XB : 1000 0001 : mod 010 r/m : imm32</td>
</tr>
<tr>
<td>immediate8 to memory64</td>
<td>0100 10XB : 1000 0031 : mod 010 r/m : imm8</td>
</tr>
<tr>
<td>ADD – Add</td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0100 0ROB : 0000 000w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1 to qwordregister2</td>
<td>0100 1ROB 0000 0000 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0ROB : 0000 001w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1 to qwordregister2</td>
<td>0100 1ROB 0000 0010 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0100 0RXB : 0000 001w : mod reg r/m</td>
</tr>
<tr>
<td>memory64 to qwordregister</td>
<td>0100 1RXB : 0000 0000 : mod qwordreg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0100 0RXB : 0000 000w : mod reg r/m</td>
</tr>
<tr>
<td>qwordregister to memory64</td>
<td>0100 1RXB : 0000 0011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>0100 0000B : 1000 00sw : 11 000 reg : immediate data</td>
</tr>
<tr>
<td>immediate32 to qwordregister</td>
<td>0100 100B : 1000 0001 : 11 010 qwordreg : imm</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0000 010w : immediate8</td>
</tr>
<tr>
<td>immediate to RAX</td>
<td>0100 1000 : 0000 0101 : imm32</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>0100 00XB : 1000 00sw : mod 000 r/m : immediate</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>immediate32 to memory64</td>
<td>0100 10XB : 1000 0001 : mod 010 r/m : imm32</td>
</tr>
<tr>
<td>immediate8 to memory64</td>
<td>0100 10XB : 1000 0011 : mod 010 r/m : imm8</td>
</tr>
<tr>
<td><strong>AND - Logical AND</strong></td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0100 0R0B 0010 000w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1 to qwordregister2</td>
<td>0100 1R0B 0010 0001 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0R0B 0010 001w : 11 reg1 reg2</td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0100 1R0B 0010 0011 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0100 0RXB 0010 001w : mod reg r/m</td>
</tr>
<tr>
<td>memory64 to qwordregister</td>
<td>0100 1RXB : 0010 0011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0100 0RXB : 0010 000w : mod reg r/m</td>
</tr>
<tr>
<td>qwordregister to memory64</td>
<td>0100 1RXB : 0010 0001 : mod qwordreg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>0100 000B : 1000 00sw : 11 100 reg : immediate</td>
</tr>
<tr>
<td>immediate32 to qwordregister</td>
<td>0100 100B 1000 0001 : 11 100 qwordreg : imm32</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0010 010w : immediate</td>
</tr>
<tr>
<td>immediate32 to RAX</td>
<td>0100 1000 0010 1001 : imm32</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>0100 00XB : 1000 00sw : mod 100 r/m : immediate</td>
</tr>
<tr>
<td>immediate32 to memory64</td>
<td>0100 10XB : 1000 0001 : mod 100 r/m : immediate32</td>
</tr>
<tr>
<td>immediate8 to memory64</td>
<td>0100 10XB : 1000 0011 : mod 100 r/m : imm8</td>
</tr>
<tr>
<td><strong>BSF - Bit Scan Forward</strong></td>
<td></td>
</tr>
<tr>
<td>register1, register2</td>
<td>0100 0R0B 0000 1111 : 1011 1100 : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1, qwordregister2</td>
<td>0100 1R0B 0000 1111 : 1011 1100 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory, register</td>
<td>0100 0RXB 0000 1111 : 1011 1100 : mod reg r/m</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory64, qwordregister</td>
<td>0100 1RXB 0000 1111 : 1011 1100 : mod qwordreg r/m</td>
</tr>
<tr>
<td><strong>BSR – Bit Scan Reverse</strong></td>
<td></td>
</tr>
<tr>
<td>register1, register2</td>
<td>0100 0R0B 0000 1111 : 1011 1101 : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1, qwordregister2</td>
<td>0100 1R0B 0000 1111 : 1011 1101 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory, register</td>
<td>0100 0RXB 0000 1111 : 1011 1101 : mod reg r/m</td>
</tr>
<tr>
<td>memory64, qwordregister</td>
<td>0100 1RXB 0000 1111 : 1011 1101 : mod qwordreg r/m</td>
</tr>
<tr>
<td><strong>BSWAP – Byte Swap</strong></td>
<td></td>
</tr>
<tr>
<td>BSWAP – Byte Swap</td>
<td>0000 1111 : 1100 1 reg</td>
</tr>
<tr>
<td>BSWAP – Byte Swap</td>
<td>0100 100B 0000 1111 : 1100 1 qwordreg</td>
</tr>
<tr>
<td><strong>BT – Bit Test</strong></td>
<td></td>
</tr>
<tr>
<td>register, immediate</td>
<td>0100 000B 0000 1111 : 1011 1010 : 11 100 reg: imm8</td>
</tr>
<tr>
<td>qwordregister, immediate8</td>
<td>0100 100B 1111 : 1011 1010 : 11 100 qwordreg: imm8 data</td>
</tr>
<tr>
<td>memory, immediate</td>
<td>0100 00XB 0000 1111 : 1011 1010 : mod 100 r/m : imm8</td>
</tr>
<tr>
<td>memory64, immediate8</td>
<td>0100 10XB 0000 1111 : 1011 1010 : mod 100 r/m : imm8 data</td>
</tr>
<tr>
<td>register1, register2</td>
<td>0100 0R0B 0000 1111 : 1010 0011 : 11 reg2 reg1</td>
</tr>
<tr>
<td>qwordregister1, qwordregister2</td>
<td>0100 1R0B 0000 1111 : 1010 0011 : 11 qwordreg2 qwordreg1</td>
</tr>
<tr>
<td>memory, reg</td>
<td>0100 0RXB 0000 1111 : 1010 0011 : mod reg r/m</td>
</tr>
<tr>
<td>memory, qwordreg</td>
<td>0100 1RXB 0000 1111 : 1010 0011 : mod qwordreg r/m</td>
</tr>
<tr>
<td><strong>BTC – Bit Test and Complement</strong></td>
<td></td>
</tr>
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</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register, immediate</td>
<td>0100 000B 0000 1111 : 1011 1010 : 11 111 reg: imm8</td>
</tr>
<tr>
<td>qwordregister, immediate8</td>
<td>0100 100B 0000 1111 : 1011 1010 : 11 111 qwordreg: imm8</td>
</tr>
<tr>
<td>memory, immediate</td>
<td>0100 00XB 0000 1111 : 1011 1010 : mod 111 r/m : imm8</td>
</tr>
<tr>
<td>memory64, immediate8</td>
<td>0100 10XB 0000 1111 : 1011 1010 : mod 111 r/m : imm8</td>
</tr>
<tr>
<td>register1, register2</td>
<td>0100 0R0B 0000 1111 : 1011 1011 : 11 reg2 reg1</td>
</tr>
<tr>
<td>qwordregister1, qwordregister2</td>
<td>0100 1R0B 0000 1111 : 1011 1011 : 11 qwordreg2 qwordreg1</td>
</tr>
<tr>
<td>memory, register</td>
<td>0100 0RXB 0000 1111 : 1011 1011 : mod reg r/m</td>
</tr>
<tr>
<td>memory, qwordreg</td>
<td>0100 1RXB 0000 1111 : 1011 1011 : mod qwordreg r/m</td>
</tr>
</tbody>
</table>

#### BTR – Bit Test and Reset

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register, immediate</td>
<td>0100 000B 0000 1111 : 1011 1010 : 11 110 reg: imm8</td>
</tr>
<tr>
<td>qwordregister, immediate8</td>
<td>0100 100B 0000 1111 : 1011 1010 : 11 110 qwordreg: imm8</td>
</tr>
<tr>
<td>memory, immediate</td>
<td>0100 00XB 0000 1111 : 1011 1010 : mod 110 r/m : imm8</td>
</tr>
<tr>
<td>memory64, immediate8</td>
<td>0100 10XB 0000 1111 : 1011 1010 : mod 110 r/m : imm8</td>
</tr>
<tr>
<td>register1, register2</td>
<td>0100 0R0B 0000 1111 : 1011 0011 : 11 reg2 reg1</td>
</tr>
<tr>
<td>qwordregister1, qwordregister2</td>
<td>0100 1R0B 0000 1111 : 1011 0011 : 11 qwordreg2 qwordreg1</td>
</tr>
<tr>
<td>memory, register</td>
<td>0100 0RXB 0000 1111 : 1011 0011 : mod reg r/m</td>
</tr>
<tr>
<td>memory64, qwordreg</td>
<td>0100 1RXB 0000 1111 : 1011 0011 : mod qwordreg r/m</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BTS – Bit Test and Set</strong></td>
<td></td>
</tr>
<tr>
<td>register, immediate</td>
<td>0100 000B 0000 1111 : 1011 1010 : 11 101 reg: imm8</td>
</tr>
<tr>
<td>qwordregister, immediate8</td>
<td>0100 100B 0000 1111 : 1011 1010 : 11 101 qwordreg: imm8</td>
</tr>
<tr>
<td>memory, immediate</td>
<td>0100 00XB 0000 1111 : 1011 1010 : mod 101 r/m : imm8</td>
</tr>
<tr>
<td>memory64, immediate8</td>
<td>0100 10XB 0000 1111 : 1011 1010 : mod 101 r/m : imm8</td>
</tr>
<tr>
<td>register1, register2</td>
<td>0100 0R0B 0000 1111 : 1010 1011 : 11 reg2</td>
</tr>
<tr>
<td>qwordregister1, qwordregister2</td>
<td>0100 1R0B 0000 1111 : 1010 1011 : 11 qwordreg2 qwordreg1</td>
</tr>
<tr>
<td>memory, register</td>
<td>0100 0RXB 0000 1111 : 1010 1011 : mod reg r/m</td>
</tr>
<tr>
<td>memory64, qwordreg</td>
<td>0100 1RXB 0000 1111 : 1010 1011 : mod qwordreg r/m</td>
</tr>
<tr>
<td><strong>CALL – Call Procedure (in same segment)</strong></td>
<td></td>
</tr>
<tr>
<td>direct</td>
<td>1110 1000 : displacement32</td>
</tr>
<tr>
<td>register indirect</td>
<td>0100 WRO0W 1111 1111 : 11 010 reg</td>
</tr>
<tr>
<td>memory indirect</td>
<td>0100 W0XBW 1111 1111 : mod 010 r/m</td>
</tr>
<tr>
<td><strong>CALL – Call Procedure (in other segment)</strong></td>
<td></td>
</tr>
<tr>
<td>indirect</td>
<td>1111 1111 : mod 011 r/m</td>
</tr>
<tr>
<td>indirect</td>
<td>0100 10XB 0100 1000 1111 1111 : mod 011 r/m</td>
</tr>
<tr>
<td><strong>CBW – Convert Byte to Word</strong></td>
<td>1001 1000</td>
</tr>
<tr>
<td><strong>CDQ – Convert Doubleword to Qword</strong></td>
<td>1001 1001</td>
</tr>
<tr>
<td><strong>CDQE – RAX, Sign-Extend of EAX</strong></td>
<td>0100 1000 1001 1001</td>
</tr>
<tr>
<td><strong>CLC – Clear Carry Flag</strong></td>
<td>1111 1000</td>
</tr>
<tr>
<td><strong>CLD – Clear Direction Flag</strong></td>
<td>1111 1100</td>
</tr>
<tr>
<td><strong>CLI – Clear Interrupt Flag</strong></td>
<td>1111 1010</td>
</tr>
<tr>
<td><strong>CLTS – Clear Task-Switched Flag in CR0</strong></td>
<td>0000 1111 : 0000 0110</td>
</tr>
<tr>
<td><strong>CMC – Complement Carry Flag</strong></td>
<td>1111 0101</td>
</tr>
</tbody>
</table>
### INSTRUCTION FORMATS AND ENCODINGS

#### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CMP – Compare Two Operands</strong></td>
<td></td>
</tr>
<tr>
<td>register1 with register2</td>
<td>0100 0R0B 0011 100w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1 with qwordregister2</td>
<td>0100 1R0B 0011 1001 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register2 with register1</td>
<td>0100 0R0B 0011 101w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister2 with qwordregister1</td>
<td>0100 1R0B 0011 101w : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory with register</td>
<td>0100 0RXB 0011 100w : mod reg r/m</td>
</tr>
<tr>
<td>memory64 with qwordregister</td>
<td>0100 1RXB 0011 1001 : mod qwordreg r/m</td>
</tr>
<tr>
<td>register with memory</td>
<td>0100 0RXB 0011 101w : mod reg r/m</td>
</tr>
<tr>
<td>qwordregister with memory64</td>
<td>0100 1RXB 0011 101w1 : mod qwordreg r/m</td>
</tr>
<tr>
<td>immediate with register</td>
<td>0100 000B 1000 00sw : 11 111 reg : imm</td>
</tr>
<tr>
<td>immediate32 with qwordregister</td>
<td>0100 100B 1000 0001 : 11 111 qwordreg : imm64</td>
</tr>
<tr>
<td>immediate with AL, AX, or EAX</td>
<td>0011 110w : imm</td>
</tr>
<tr>
<td>immediate32 with RAX</td>
<td>0100 1000 0011 1101 : imm32</td>
</tr>
<tr>
<td>immediate with memory</td>
<td>0100 000B 1000 00sw : mod 111 r/m : imm</td>
</tr>
<tr>
<td>immediate32 with memory64</td>
<td>0100 1RXB 1000 0001 : mod 111 r/m : imm64</td>
</tr>
<tr>
<td>immediate8 with memory64</td>
<td>0100 1RXB 1000 0011 : mod 111 r/m : imm8</td>
</tr>
<tr>
<td><strong>CMPS/CMPSB/CMPSW/CMPSD/CMPSQ – Compare String Operands</strong></td>
<td></td>
</tr>
<tr>
<td>compare string operands [ X at DS:(E)SI with Y at ES:(E)DI ]</td>
<td>1010 011w</td>
</tr>
<tr>
<td>qword at address RSI with qword at address RDI</td>
<td>0100 1000 1010 0111</td>
</tr>
<tr>
<td><strong>CMPXCHG – Compare and Exchange</strong></td>
<td></td>
</tr>
<tr>
<td>register1, register2</td>
<td>0000 1111 : 1011 000w : 11 reg2 reg1</td>
</tr>
<tr>
<td>byteregister1, byteregister2</td>
<td>0100 000B 0000 1111 : 1011 0000 : 11 bytereg2 reg1</td>
</tr>
<tr>
<td>qwordregister1, qwordregister2</td>
<td>0100 100B 0000 1111 : 1011 0001 : 11 qwordreg2 reg1</td>
</tr>
<tr>
<td>memory, register</td>
<td>0000 1111 : 1011 000w : mod reg r/m</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>----------------------------------------</td>
<td>-----------------------------------------------</td>
</tr>
<tr>
<td>memory8, byteregister</td>
<td>0100 00XB 0000 1111 : 1011 0000 : mod bytereg r/m</td>
</tr>
<tr>
<td>memory64, qwordregister</td>
<td>0100 10XB 0000 1111 : 1011 0001 : mod qwordreg r/m</td>
</tr>
<tr>
<td>CPUID – CPU Identification</td>
<td>0000 1111 : 1010 0010</td>
</tr>
<tr>
<td>CQO – Sign-Extend RAX</td>
<td>0100 1000 1001 1001</td>
</tr>
<tr>
<td>CWD – Convert Word to Doubleword</td>
<td>1001 1001</td>
</tr>
<tr>
<td>CWDE – Convert Word to Doubleword</td>
<td>1001 1000</td>
</tr>
<tr>
<td>DEC – Decrement by 1</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>0100 000B 1111 1111w : 11 001 reg</td>
</tr>
<tr>
<td>qwordregister</td>
<td>0100 100B 1111 1111 : 11 001 qwordreg</td>
</tr>
<tr>
<td>memory</td>
<td>0100 00XB 1111 1111w : mod 001 r/m</td>
</tr>
<tr>
<td>memory64</td>
<td>0100 10XB 1111 1111 : mod 001 r/m</td>
</tr>
<tr>
<td>DIV – Unsigned Divide</td>
<td></td>
</tr>
<tr>
<td>AL, AX, or EAX by register</td>
<td>0100 000B 1111 0111w : 11 110 reg</td>
</tr>
<tr>
<td>Divide RDX:RAX by qwordregister</td>
<td>0100 100B 1111 0111 : 11 110 qwordreg</td>
</tr>
<tr>
<td>AL, AX, or EAX by memory</td>
<td>0100 00XB 1111 0111w : mod 110 r/m</td>
</tr>
<tr>
<td>Divide RDX:RAX by memory64</td>
<td>0100 10XB 1111 0111 : mod 110 r/m</td>
</tr>
<tr>
<td>ENTER – Make Stack Frame for High Level Procedure</td>
<td>1100 1000 : 16-bit displacement : 8-bit level (L)</td>
</tr>
<tr>
<td>HLT – Halt</td>
<td>1111 0100</td>
</tr>
<tr>
<td>IDIV – Signed Divide</td>
<td></td>
</tr>
<tr>
<td>AL, AX, or EAX by register</td>
<td>0100 000B 1111 0111w : 11 111 reg</td>
</tr>
<tr>
<td>RDX:RAX by qwordregister</td>
<td>0100 100B 1111 0111 : 11 111 qwordreg</td>
</tr>
<tr>
<td>AL, AX, or EAX by memory</td>
<td>0100 00XB 1111 0111w : mod 111 r/m</td>
</tr>
<tr>
<td>RDX:RAX by memory64</td>
<td>0100 10XB 1111 0111 : mod 111 r/m</td>
</tr>
<tr>
<td>IMUL – Signed Multiply</td>
<td></td>
</tr>
<tr>
<td>AL, AX, or EAX with register</td>
<td>0100 000B 1111 0111w : 11 101 reg</td>
</tr>
<tr>
<td>RDX:RAX &lt;- RAX with qwordregister</td>
<td>0100 100B 1111 0111 : 11 101 qwordreg</td>
</tr>
<tr>
<td>AL, AX, or EAX with memory</td>
<td>0100 00XB 1111 0111w : mod 101 r/m</td>
</tr>
<tr>
<td>RDX:RAX &lt;- RAX with memory64</td>
<td>0100 10XB 1111 0111 : mod 101 r/m</td>
</tr>
</tbody>
</table>
### INSTRUCTION FORMATS AND ENCODINGS

#### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
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<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register1 with register2</td>
<td>0000 1111 : 1010 1111 : 11 : reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1 &lt;- qwordregister1 with qwordregister2</td>
<td>0100 1ROB 0000 1111 : 1010 1111 : 11 : qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register with memory</td>
<td>0100 ORXB 0000 1111 : 1010 1111 : mod reg r/m</td>
</tr>
<tr>
<td>qwordregister &lt;- qwordregister with memory64</td>
<td>0100 1RXB 0000 1111 : 1010 1111 : mod qwordreg r/m</td>
</tr>
<tr>
<td>register1 with immediate to register2</td>
<td>0100 0ROB 0110 10s1 : 11 reg1 reg2 : imm</td>
</tr>
<tr>
<td>qwordregister1 &lt;- qwordregister2 with sign-extended immediate8</td>
<td>0100 1ROB 0110 1011 : 11 qwordreg1 qwordreg2 : imm8</td>
</tr>
<tr>
<td>qwordregister1 &lt;- qwordregister2 with immediate32</td>
<td>0100 1ROB 0110 1001 : 11 qwordreg1 qwordreg2 : imm32</td>
</tr>
<tr>
<td>memory with immediate to register</td>
<td>0100 ORXB 0110 10s1 : mod reg r/m : imm</td>
</tr>
<tr>
<td>qwordregister &lt;- memory64 with sign-extended immediate8</td>
<td>0100 1RXB 0110 1011 : mod qwordreg r/m : imm8</td>
</tr>
<tr>
<td>qwordregister &lt;- memory64 with immediate32</td>
<td>0100 1RXB 0110 1001 : mod qwordreg r/m : imm32</td>
</tr>
<tr>
<td><strong>IN – Input From Port</strong></td>
<td></td>
</tr>
<tr>
<td>fixed port</td>
<td>1110 010w : port number</td>
</tr>
<tr>
<td>variable port</td>
<td>1110 110w</td>
</tr>
<tr>
<td><strong>INC – Increment by 1</strong></td>
<td></td>
</tr>
<tr>
<td>reg</td>
<td>0100 000B 1111 111w : 11 000 reg</td>
</tr>
<tr>
<td>qwordreg</td>
<td>0100 100B 1111 1111 : 11 000 qwordreg</td>
</tr>
<tr>
<td>memory</td>
<td>0100 00XB 1111 111w : mod 000 r/m</td>
</tr>
<tr>
<td>memory64</td>
<td>0100 10XB 1111 1111 : mod 000 r/m</td>
</tr>
<tr>
<td><strong>INS – Input from DX Port</strong></td>
<td>0110 110w</td>
</tr>
<tr>
<td><strong>INT n – Interrupt Type n</strong></td>
<td>1100 1101 : type</td>
</tr>
<tr>
<td><strong>INT – Single-Step Interrupt 3</strong></td>
<td>1100 1100</td>
</tr>
<tr>
<td><strong>INTO – Interrupt 4 on Overflow</strong></td>
<td>1100 1110</td>
</tr>
<tr>
<td><strong>INVD – Invalidate Cache</strong></td>
<td>0000 1111 : 0000 1000</td>
</tr>
<tr>
<td><strong>INVLPG – Invalidate TLB Entry</strong></td>
<td>0000 1111 : 0000 0001 : mod 111 r/m</td>
</tr>
</tbody>
</table>
Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>INVPCID – Invalidate Process-Context Identifier</td>
<td>0110 0110:0000 1111:0011 1000:1000 0010: mod reg r/m</td>
</tr>
<tr>
<td>IRETO – Interrupt Return</td>
<td>1100 1111</td>
</tr>
<tr>
<td>Jcc – Jump if Condition is Met</td>
<td>0111 tttn : 8-bit displacement</td>
</tr>
<tr>
<td></td>
<td>0000 1111 : 1000 tttn : displacement32</td>
</tr>
<tr>
<td>JCXZ/JECXZ – Jump on CX/ECX Zero</td>
<td>1110 0011 : 8-bit displacement</td>
</tr>
<tr>
<td>JMP – Unconditional Jump (to same segment)</td>
<td>1110 1011 : 8-bit displacement</td>
</tr>
<tr>
<td>short</td>
<td>1110 1001 : displacement32</td>
</tr>
<tr>
<td>direct</td>
<td>0100 W0XB : 1111 1111 : 11 100 reg</td>
</tr>
<tr>
<td>register indirect</td>
<td>0100 WR0B : 0000 1111 : 0000 0010 : mod reg r/m</td>
</tr>
<tr>
<td>memory indirect</td>
<td>0100 WRXB : 0000 1111 : 0000 0010 : mod r/m</td>
</tr>
<tr>
<td>JMP – Unconditional Jump (to other segment)</td>
<td>0100 00XB : 1111 1111 : mod 101 r/m</td>
</tr>
<tr>
<td>indirect intersegment</td>
<td>0100 10XB : 1111 1111 : mod 101 r/m</td>
</tr>
<tr>
<td>LAR – Load Access Rights Byte</td>
<td>0100 0R0B : 0000 1111 : 0000 0010 : 11 reg1 reg2</td>
</tr>
<tr>
<td>from register</td>
<td>0100 WR0B : 0000 1111 : 0000 0010 : 11 qwordreg1 dwordreg2</td>
</tr>
<tr>
<td>from dwordregister to qwordregister, masked by 00FxFF00H</td>
<td>0100 0RXB : 0000 1111 : 0000 0010 : mod r/m</td>
</tr>
<tr>
<td>from memory</td>
<td>0100 WRXB 0000 1111 : 0000 0010 : mod r/m</td>
</tr>
<tr>
<td>LEA – Load Effective Address</td>
<td>0100 ORXB : 1000 1111 : mod^A reg r/m</td>
</tr>
<tr>
<td>in wordregister/dwordregister</td>
<td>0100 1RXB : 1000 1111 : mod^A qwordreg r/m</td>
</tr>
<tr>
<td>LEAVE – High Level Procedure Exit</td>
<td>1100 1001</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>LFS – Load Pointer to FS</td>
<td>0100 0RXB : 0000 1111 : 1011 0100 : modA reg r/m</td>
</tr>
<tr>
<td>FS:r16/r32 with far pointer from memory</td>
<td></td>
</tr>
<tr>
<td>FS:r64 with far pointer from memory</td>
<td>0100 1RXB : 0000 1111 : 1011 0100 : modA qwordreg r/m</td>
</tr>
<tr>
<td>LGDT – Load Global Descriptor Table Register</td>
<td>0100 10XB : 0000 1111 : 0000 0001 : modA 010 r/m</td>
</tr>
<tr>
<td>LGS – Load Pointer to GS</td>
<td></td>
</tr>
<tr>
<td>GS:r16/r32 with far pointer from memory</td>
<td>0100 0RXB : 0000 1111 : 1011 0101 : modA reg r/m</td>
</tr>
<tr>
<td>GS:r64 with far pointer from memory</td>
<td>0100 1RXB : 0000 1111 : 1011 0101 : modA qwordreg r/m</td>
</tr>
<tr>
<td>LIDT – Load Interrupt Descriptor Table Register</td>
<td>0100 10XB : 0000 1111 : 0000 0001 : modA 011 r/m</td>
</tr>
<tr>
<td>LLDT – Load Local Descriptor Table Register</td>
<td></td>
</tr>
<tr>
<td>LDTR from register</td>
<td>0100 000B : 0000 1111 : 0000 0000 : 11 010 reg</td>
</tr>
<tr>
<td>LDTR from memory</td>
<td>0100 00XB : 0000 1111 : 0000 0000 : mod 010 r/m</td>
</tr>
<tr>
<td>LMSW – Load Machine Status Word</td>
<td></td>
</tr>
<tr>
<td>from register</td>
<td>0100 000B : 0000 1111 : 0000 0001 : 11 110 reg</td>
</tr>
<tr>
<td>from memory</td>
<td>0100 00XB : 0000 1111 : 0000 0001 : mod 110 r/m</td>
</tr>
<tr>
<td>LOCK – Assert LOCK# Signal Prefix</td>
<td>1111 0000</td>
</tr>
<tr>
<td>LODS/LODSB/LODSW/LODSP – Load String Operand</td>
<td></td>
</tr>
<tr>
<td>at DS:(E)SI to AL/EAX/EAX</td>
<td>1010 110w</td>
</tr>
<tr>
<td>at (R)SI to RAX</td>
<td>0100 1000 1010 1101</td>
</tr>
<tr>
<td>LOOP – Loop Count</td>
<td></td>
</tr>
<tr>
<td>if count != 0, 8-bit displacement</td>
<td>1110 0010</td>
</tr>
<tr>
<td>if count != 0, RIP + 8-bit displacement sign-extended to 64-bits</td>
<td>0100 1000 1110 0010</td>
</tr>
<tr>
<td>LOOPE – Loop Count while Zero/Equal</td>
<td></td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>if count $\neq 0$ &amp; ZF = 1, 8-bit displacement</td>
<td>1110 0001</td>
</tr>
<tr>
<td>if count $\neq 0$ &amp; ZF = 1, RIP + 8-bit displacement</td>
<td>0100 1000 1110 0001</td>
</tr>
<tr>
<td>sign-extended to 64-bits</td>
<td></td>
</tr>
<tr>
<td>LOOPNE/LOOPNZ – Loop Count while not Zero/Equal</td>
<td></td>
</tr>
<tr>
<td>if count $\neq 0$ &amp; ZF = 0, 8-bit displacement</td>
<td>1110 0000</td>
</tr>
<tr>
<td>if count $\neq 0$ &amp; ZF = 0, RIP + 8-bit displacement</td>
<td>0100 1000 1110 0000</td>
</tr>
<tr>
<td>sign-extended to 64-bits</td>
<td></td>
</tr>
<tr>
<td>LSL – Load Segment Limit</td>
<td></td>
</tr>
<tr>
<td>from register</td>
<td>0000 1111 : 0000 0011 : 11 reg1 reg2</td>
</tr>
<tr>
<td>from qwordregister</td>
<td>0100 1R00 0000 1111 : 0000 0011 : 11 qwordreg1 reg2</td>
</tr>
<tr>
<td>from memory16</td>
<td>0000 1111 : 0000 0011 : mod reg r/m</td>
</tr>
<tr>
<td>from memory64</td>
<td>0100 1RXB 0000 1111 : 0000 0011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>LSS – Load Pointer to SS</td>
<td></td>
</tr>
<tr>
<td>SS:r16/r32 with far pointer from memory</td>
<td>0100 0RXB : 0000 1111 : 1011 0010 : modA reg r/m</td>
</tr>
<tr>
<td>SS:r64 with far pointer from memory</td>
<td>0100 1wXB : 0000 1111 : 1011 0010 : modA qwordreg r/m</td>
</tr>
<tr>
<td>LTR – Load Task Register</td>
<td></td>
</tr>
<tr>
<td>from register</td>
<td>0100 0R00 : 0000 1111 : 0000 0000 : 11 011 reg</td>
</tr>
<tr>
<td>from memory</td>
<td>0100 00XB : 0000 1111 : 0000 0000 : mod 011 r/m</td>
</tr>
<tr>
<td>MOV – Move Data</td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0100 0R0B : 1000 100w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister1 to qwordregister2</td>
<td>0100 1R0B 1000 1001 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0R0B : 1000 101w : 11 reg1 reg2</td>
</tr>
<tr>
<td>qwordregister2 to qwordregister1</td>
<td>0100 1R0B 1000 1011 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory to reg</td>
<td>0100 0RXB : 1000 101w : mod reg r/m</td>
</tr>
</tbody>
</table>
## INSTRUCTION FORMATS AND ENCODINGS

### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory64 to qwordregister</td>
<td>0100 1RXB 1000 1011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>reg to memory</td>
<td>0100 0RXB: 1000 100w : mod reg r/m</td>
</tr>
<tr>
<td>qwordregister to memory64</td>
<td>0100 1RXB 1000 1001 : mod qwordreg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>0100 000B: 1100 011w: 11 000 reg : imm</td>
</tr>
<tr>
<td>immediate32 to qwordregister (zero extend)</td>
<td>0100 100B 1100 0111 : 11 000 qwordreg : imm32</td>
</tr>
<tr>
<td>immediate to register (alternate encoding)</td>
<td>0100 000B: 1011 w reg : imm</td>
</tr>
<tr>
<td>immediate64 to qwordregister (alternate encoding)</td>
<td>0100 100B 1011 1000 reg : imm64</td>
</tr>
<tr>
<td>immediate32 to memory64 (zero extend)</td>
<td>0100 10XB 1100 0111 : mod 000 r/m : imm32</td>
</tr>
<tr>
<td>memory to AL, AX, or EAX</td>
<td>0100 0000 : 1010 001w : displacement</td>
</tr>
<tr>
<td>RAX to memory64</td>
<td>0100 1000 1010 0011 : displacement64</td>
</tr>
<tr>
<td>MOV – Move to/from Control Registers</td>
<td></td>
</tr>
<tr>
<td>CR0-CR4 from register</td>
<td>0100 0R0B: 0000 1111 : 0010 0010 : 11 eee reg (eee = CR#)</td>
</tr>
<tr>
<td>CRx from qwordregister</td>
<td>0100 1R0B: 0000 1111 : 0110 0010 : 11 eee qwordreg (Reee = CR#)</td>
</tr>
<tr>
<td>register from CR0-CR4</td>
<td>0100 0R0B: 0000 1111 : 0010 0000 : 11 eee reg (eee = CR#)</td>
</tr>
<tr>
<td>qwordregister from CRx</td>
<td>0100 1R0B 0000 1111 : 0010 0000 : 11 eee qwordreg (Reee = CR#)</td>
</tr>
<tr>
<td>MOV – Move to/from Debug Registers</td>
<td></td>
</tr>
<tr>
<td>DRO-DR7 from register</td>
<td>0000 1111 : 0010 0011 : 11 eee reg (eee = DR#)</td>
</tr>
<tr>
<td>DRO-DR7 from quadregister</td>
<td>0100 100B 0000 1111 : 0010 0011 : 11 eee reg (eee = DR#)</td>
</tr>
<tr>
<td>register from DRO-DR7</td>
<td>0000 1111 : 0010 0001 : 11 eee reg (eee = DR#)</td>
</tr>
<tr>
<td>quadregister from DRO-DR7</td>
<td>0100 100B 0000 1111 : 0010 0001 : 11 eee quadreg (eee = DR#)</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOV – Move to/from Segment Registers</td>
<td></td>
</tr>
<tr>
<td>register to segment register</td>
<td>0100 W00B: 1000 1110 : 11 sreg reg</td>
</tr>
<tr>
<td>register to SS</td>
<td>0100 000B : 1000 1110 : 11 sreg reg</td>
</tr>
<tr>
<td>memory to segment register</td>
<td>0100 00XB : 1000 1110 : mod sreg r/m</td>
</tr>
<tr>
<td>memory64 to segment register (lower 16 bits)</td>
<td>0100 10XB 1000 1110 : mod sreg r/m</td>
</tr>
<tr>
<td>memory to SS</td>
<td>0100 00XB : 1000 1110 : mod sreg r/m</td>
</tr>
<tr>
<td>segment register to register</td>
<td>0100 000B : 1000 1100 : 11 sreg reg</td>
</tr>
<tr>
<td>segment register to qwordregister (zero extended)</td>
<td>0100 000B 1000 1100 : 11 sreg qwordreg</td>
</tr>
<tr>
<td>segment register to memory</td>
<td>0100 00XB : 1000 1100 : mod sreg r/m</td>
</tr>
<tr>
<td>segment register to memory64 (zero extended)</td>
<td>0100 10XB 1000 1100 : mod sreg3 r/m</td>
</tr>
<tr>
<td>MOVBE – Move data after swapping bytes</td>
<td></td>
</tr>
<tr>
<td>memory to register</td>
<td>0100 0RXB : 0000 1111 : 0011 1000:1111 0000 : mod reg r/m</td>
</tr>
<tr>
<td>memory64 to qwordregister</td>
<td>0100 1RXB : 0000 1111 : 0011 1000:1111 0000 : mod reg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0100 0RXB : 0000 1111 : 0011 1000:1111 0001 : mod reg r/m</td>
</tr>
<tr>
<td>qwordregister to memory64</td>
<td>0100 1RXB : 0000 1111 : 0011 1000:1111 0001 : mod reg r/m</td>
</tr>
<tr>
<td>MOVS/MOVSB/MOVSW/MOVSĐ/MOVSQ – Move Data from String to String</td>
<td></td>
</tr>
<tr>
<td>Move data from string to string</td>
<td>1010 010w</td>
</tr>
<tr>
<td>Move data from string to string (qword)</td>
<td>0100 1000 1010 0101</td>
</tr>
<tr>
<td>MOVSX/MOVSEXD – Move with Sign-Extend</td>
<td></td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0R0B : 0000 1111 : 1011 111w : 11 reg1 reg2</td>
</tr>
<tr>
<td>byteregister2 to qwordregister1 (sign-extend)</td>
<td>0100 1R0B 0000 1111 : 1011 1110 : 11 quadreg1 bytereg2</td>
</tr>
<tr>
<td>wordregister2 to qwordregister1</td>
<td>0100 1R0B 0000 1111 : 1011 1111 : 11 quadreg1 wordreg2</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>dwordregister2 to qwordregister1</td>
<td>0100 1R0B 0110 0011 : 11 quadreg1 dwordreg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0100 0RXB : 0000 1111 : 1011 1111w : mod reg r/m</td>
</tr>
<tr>
<td>memory8 to qwordregister (sign-extend)</td>
<td>0100 1RXB 0000 1111 : 1011 1110 : mod qwordreg r/m</td>
</tr>
<tr>
<td>memory16 to qwordregister</td>
<td>0100 1RXB 0000 1111 : 1011 1111 : mod qwordreg r/m</td>
</tr>
<tr>
<td>memory32 to qwordregister</td>
<td>0100 1RXB 0110 0011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>MOVZX – Move with Zero-Extend</td>
<td></td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0R0B : 0000 1111 : 1011 011w : 11 reg1 reg2</td>
</tr>
<tr>
<td>dwordregister2 to qwordregister1</td>
<td>0100 1R0B 0000 1111 : 1011 0111 : 11 qwordreg1 dwordreg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0100 0RXB : 0000 1111 : 1011 011w : mod reg r/m</td>
</tr>
<tr>
<td>memory32 to qwordregister</td>
<td>0100 1RXB 0000 1111 : 1011 0111 : mod qwordreg r/m</td>
</tr>
<tr>
<td>MUL – Unsigned Multiply</td>
<td></td>
</tr>
<tr>
<td>AL, AX, or EAX with register</td>
<td>0100 000B : 1111 011w : 11 100 reg</td>
</tr>
<tr>
<td>RAX with qwordregister (to RDX:RAX)</td>
<td>0100 100B 1111 0111 : 11 100 qwordreg</td>
</tr>
<tr>
<td>AL, AX, or EAX with memory</td>
<td>0100 00XB 1111 011w : mod 100 r/m</td>
</tr>
<tr>
<td>RAX with memory64 (to RDX:RAX)</td>
<td>0100 10XB 1111 0111 : mod 100 r/m</td>
</tr>
<tr>
<td>NEG – Two’s Complement Negation</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>0100 000B : 1111 011w : 11 101 reg</td>
</tr>
<tr>
<td>qwordregister</td>
<td>0100 100B 1111 0111 : 11 011 qwordreg</td>
</tr>
<tr>
<td>memory</td>
<td>0100 00XB : 1111 011w : mod 011 r/m</td>
</tr>
<tr>
<td>memory64</td>
<td>0100 10XB 1111 0111 : mod 011 r/m</td>
</tr>
<tr>
<td>NOP – No Operation</td>
<td>1001 0000</td>
</tr>
<tr>
<td>NOT – One’s Complement Negation</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>0100 000B : 1111 011w : 11 010 reg</td>
</tr>
<tr>
<td>qwordregister</td>
<td>0100 000B 1111 0111 : 11 010 qwordreg</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory</td>
<td>0100 00XB : 1111 011w : mod 010 r/m</td>
</tr>
<tr>
<td>memory64</td>
<td>0100 1RXB 1111 0111 : mod 010 r/m</td>
</tr>
<tr>
<td>OR - Logical Inclusive OR</td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0000 100w : 11 reg1 reg2</td>
</tr>
<tr>
<td>byteregister1 to byteregister2</td>
<td>0100 0R0B 0000 1000 : 11 bytereg1 bytereg2</td>
</tr>
<tr>
<td>qwordregister1 to qwordregister2</td>
<td>0100 1R0B 0000 1001 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0000 101w : 11 reg1 reg2</td>
</tr>
<tr>
<td>byteregister2 to byteregister1</td>
<td>0100 0R0B 0000 1010 : 11 bytereg1 bytereg2</td>
</tr>
<tr>
<td>qwordregister2 to qwordregister1</td>
<td>0100 0R0B 0000 1011 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0000 101w : mod reg r/m</td>
</tr>
<tr>
<td>memory8 to byteregister</td>
<td>0100 0RXB 0000 1010 : mod bytereg r/m</td>
</tr>
<tr>
<td>memory8 to qwordregister</td>
<td>0100 0RXB 0000 1011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0000 100w : mod reg r/m</td>
</tr>
<tr>
<td>byteregister to memory8</td>
<td>0100 0RXB 0000 1000 : mod bytereg r/m</td>
</tr>
<tr>
<td>qwordregister to memory64</td>
<td>0100 1RXB 0000 1001 : mod qwordreg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>1000 00sw : 11 001 reg : imm</td>
</tr>
<tr>
<td>immediate8 to byteregister</td>
<td>0100 000B 1000 0000 : 11 001 bytereg : imm8</td>
</tr>
<tr>
<td>immediate32 to qwordregister</td>
<td>0100 000B 1000 0001 : 11 001 qwordreg : imm32</td>
</tr>
<tr>
<td>immediate8 to qwordregister</td>
<td>0100 000B 1000 0011 : 11 001 qwordreg : imm8</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0000 110w : imm</td>
</tr>
<tr>
<td>immediate64 to RAX</td>
<td>0100 1000 0000 1101 : imm64</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>1000 00sw : mod 001 r/m : imm</td>
</tr>
<tr>
<td>immediate8 to memory8</td>
<td>0100 00XB 1000 0000 : mod 001 r/m : imm8</td>
</tr>
<tr>
<td>immediate32 to memory64</td>
<td>0100 00XB 1000 0001 : mod 001 r/m : imm32</td>
</tr>
<tr>
<td>immediate8 to memory64</td>
<td>0100 00XB 1000 0011 : mod 001 r/m : imm8</td>
</tr>
</tbody>
</table>
Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OUT – Output to Port</strong></td>
<td></td>
</tr>
<tr>
<td>fixed port</td>
<td>1110 011w: port number</td>
</tr>
<tr>
<td>variable port</td>
<td>1110 111w</td>
</tr>
<tr>
<td><strong>OUTS – Output to DX Port</strong></td>
<td></td>
</tr>
<tr>
<td>output to DX Port</td>
<td>0110 111w</td>
</tr>
<tr>
<td><strong>POP – Pop a Value from the Stack</strong></td>
<td></td>
</tr>
<tr>
<td>wordregister</td>
<td>0101 0101: 0100 000B: 1000 1111: 11 000 reg16</td>
</tr>
<tr>
<td>qwordregister</td>
<td>0100 W00B^S: 1000 1111: 11 000 reg64</td>
</tr>
<tr>
<td>wordregister (alternate encoding)</td>
<td>0101 0101: 0100 000B: 0101 1 reg16</td>
</tr>
<tr>
<td>qwordregister (alternate encoding)</td>
<td>0100 W00B: 0101 1 reg64</td>
</tr>
<tr>
<td>memory64</td>
<td>0100 W0XB^S: 1000 1111: mod 000 r/m</td>
</tr>
<tr>
<td>memory16</td>
<td>0101 0101: 0100 00XB 1000 1111: mod 000 r/m</td>
</tr>
<tr>
<td><strong>POP – Pop a Segment Register from the Stack</strong></td>
<td></td>
</tr>
<tr>
<td>(Note: CS cannot be sreg2 in this usage.)</td>
<td></td>
</tr>
<tr>
<td>segment register FS, GS</td>
<td>0000 1111: 10 sreg3 001</td>
</tr>
<tr>
<td><strong>POPF/POPFQ – Pop Stack into FLAGS/RFLAGS</strong></td>
<td></td>
</tr>
<tr>
<td>Register</td>
<td></td>
</tr>
<tr>
<td>pop stack to FLAGS register</td>
<td>0101 0101: 1001 1101</td>
</tr>
<tr>
<td>pop Stack to RFLAGS register</td>
<td>0100 1000 1001 1101</td>
</tr>
<tr>
<td><strong>PUSH – Push Operand onto the Stack</strong></td>
<td></td>
</tr>
<tr>
<td>wordregister</td>
<td>0101 0101: 0100 000B: 1111 1111: 11 110 reg16</td>
</tr>
<tr>
<td>qwordregister</td>
<td>0100 W00B^S: 1111 1111: 11 110 reg64</td>
</tr>
<tr>
<td>wordregister (alternate encoding)</td>
<td>0101 0101: 0100 000B: 0101 0 reg16</td>
</tr>
<tr>
<td>qwordregister (alternate encoding)</td>
<td>0100 W00B^S: 0101 0 reg64</td>
</tr>
<tr>
<td>memory16</td>
<td>0101 0101: 0100 000B: 1111 1111: mod 110 r/m</td>
</tr>
<tr>
<td>memory64</td>
<td>0100 W00B^S: 1111 1111: mod 110 r/m</td>
</tr>
<tr>
<td>immediate8</td>
<td>0110 1010: imm8</td>
</tr>
<tr>
<td>immediate16</td>
<td>0101 0101: 0110 1000: imm16</td>
</tr>
</tbody>
</table>
Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>immediate64</td>
<td>0110 1000 : imm64</td>
</tr>
<tr>
<td><strong>PUSH – Push Segment Register onto the Stack</strong></td>
<td></td>
</tr>
<tr>
<td>segment register FS,GS</td>
<td>0000 1111: 10 sreg3 000</td>
</tr>
<tr>
<td><strong>PUSHF/PUSHFD – Push Flags Register onto the Stack</strong></td>
<td>1001 1100</td>
</tr>
<tr>
<td><strong>RCL – Rotate thru Carry Left</strong></td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>0100 000B : 1101 000w : 11 010 reg</td>
</tr>
<tr>
<td>qword register by 1</td>
<td>0100 100B 1101 0001: 11 010 qwordreg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>0100 00XB : 1101 000w : mod 010 r/m</td>
</tr>
<tr>
<td>memory64 by 1</td>
<td>0100 10XB 1101 0001 : mod 010 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 000B : 1101 001w : 11 010 reg</td>
</tr>
<tr>
<td>qword register by CL</td>
<td>0100 100B 1101 0011 : 11 010 qwordreg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0100 00XB : 1101 001w : mod 010 r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 10XB 1101 0011 : mod 010 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>0100 000B : 1100 000w : 11 010 reg : imm</td>
</tr>
<tr>
<td>qword register by immediate count</td>
<td>0100 100B 1100 0001 : 11 010 qwordreg : imm8</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0100 00XB : 1100 000w : mod 010 r/m : imm</td>
</tr>
<tr>
<td>memory64 by immediate count</td>
<td>0100 10XB 1100 0001 : mod 010 r/m : imm8</td>
</tr>
<tr>
<td><strong>RCR – Rotate thru Carry Right</strong></td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>0100 000B : 1101 000w : 11 011 reg</td>
</tr>
<tr>
<td>qword register by 1</td>
<td>0100 100B 1101 0001: 11 011 qwordreg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>0100 00XB : 1101 000w : mod 011 r/m</td>
</tr>
<tr>
<td>memory64 by 1</td>
<td>0100 10XB 1101 0001 : mod 011 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 000B : 1101 001w : 11 011 reg</td>
</tr>
<tr>
<td>qword register by CL</td>
<td>0100 000B 1101 0010 : 11 011 qwordreg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0100 00XB : 1101 001w : mod 011 r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 10XB 1101 0011 : mod 011 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>0100 000B : 1100 000w : 11 011 reg : imm8</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>qwordregister by immediate count</td>
<td>0100 100B 1100 0001 : 11 011 qwordreg : imm8</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0100 00XB : 1100 000w : mod 011 r/m : imm8</td>
</tr>
<tr>
<td>memory64 by immediate count</td>
<td>0100 10XB 1100 0001 : mod 011 r/m : imm8</td>
</tr>
<tr>
<td>RDMSR - Read from Model-Specific Register</td>
<td></td>
</tr>
<tr>
<td>load ECX-specified register into EDX:EAX</td>
<td>0000 1111 : 0011 0010</td>
</tr>
<tr>
<td>RDPMC - Read Performance Monitoring Counters</td>
<td></td>
</tr>
<tr>
<td>load ECX-specified performance counter into EDX:EAX</td>
<td>0000 1111 : 0011 0011</td>
</tr>
<tr>
<td>RDTSC - Read Time-Stamp Counter</td>
<td></td>
</tr>
<tr>
<td>read time-stamp counter into EDX:EAX</td>
<td>0000 1111 : 0011 0001</td>
</tr>
<tr>
<td>RDTSCP - Read Time-Stamp Counter and Processor ID</td>
<td>0000 1111 : 0000 0001 : 1111 1001</td>
</tr>
<tr>
<td>REP INS - Input String</td>
<td></td>
</tr>
<tr>
<td>REP LODS - Load String</td>
<td></td>
</tr>
<tr>
<td>REP MOVS - Move String</td>
<td></td>
</tr>
<tr>
<td>REP OUTS - Output String</td>
<td></td>
</tr>
<tr>
<td>REP STOS - Store String</td>
<td></td>
</tr>
<tr>
<td>REPE CMPS - Compare String</td>
<td></td>
</tr>
<tr>
<td>REPE SCAS - Scan String</td>
<td></td>
</tr>
<tr>
<td>REPNE CMPS - Compare String</td>
<td></td>
</tr>
<tr>
<td>REPNE SCAS - Scan String</td>
<td></td>
</tr>
<tr>
<td>RET - Return from Procedure (to same segment)</td>
<td></td>
</tr>
<tr>
<td>no argument</td>
<td>1100 0011</td>
</tr>
<tr>
<td>adding immediate to SP</td>
<td>1100 0010 : 16-bit displacement</td>
</tr>
<tr>
<td>RET - Return from Procedure (to other segment)</td>
<td></td>
</tr>
<tr>
<td>intersegment</td>
<td>1100 1011</td>
</tr>
<tr>
<td>adding immediate to SP</td>
<td>1100 1010 : 16-bit displacement</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ROL - Rotate Left</strong></td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>0100 000B 1101 000w : 11 000 reg</td>
</tr>
<tr>
<td>bytereg register by 1</td>
<td>0100 000B 1101 0000 : 11 000 bytereg</td>
</tr>
<tr>
<td>qword register by 1</td>
<td>0100 100B 1101 0001 : 11 000 qwordreg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>0100 00XB 1101 000w : mod 000 r/m</td>
</tr>
<tr>
<td>memory8 by 1</td>
<td>0100 00XB 1101 0000 : mod 000 r/m</td>
</tr>
<tr>
<td>memory64 by 1</td>
<td>0100 10XB 1101 0001 : mod 000 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 000B 1101 001w : 11 000 reg</td>
</tr>
<tr>
<td>bytereg register by CL</td>
<td>0100 000B 1101 0010 : 11 000 bytereg</td>
</tr>
<tr>
<td>qword register by CL</td>
<td>0100 100B 1101 0011 : 11 000 qwordreg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0100 00XB 1101 001w : mod 000 r/m</td>
</tr>
<tr>
<td>memory8 by CL</td>
<td>0100 00XB 1101 0010 : mod 000 r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 10XB 1101 0011 : mod 000 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>1100 000w : 11 000 reg : imm8</td>
</tr>
<tr>
<td>bytereg register by immediate count</td>
<td>0100 000B 1100 0000 : 11 000 bytereg : imm8</td>
</tr>
<tr>
<td>qword register by immediate count</td>
<td>0100 100B 1100 0001 : 11 000 bytereg : imm8</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>1100 000w : mod 000 r/m : imm8</td>
</tr>
<tr>
<td>memory8 by immediate count</td>
<td>0100 00XB 1100 0000 : mod 000 r/m : imm8</td>
</tr>
<tr>
<td>memory64 by immediate count</td>
<td>0100 10XB 1100 0001 : mod 000 r/m : imm8</td>
</tr>
<tr>
<td><strong>ROR - Rotate Right</strong></td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>0100 000B 1101 000w : 11 001 reg</td>
</tr>
<tr>
<td>bytereg register by 1</td>
<td>0100 000B 1101 0000 : 11 001 bytereg</td>
</tr>
<tr>
<td>qword register by 1</td>
<td>0100 100B 1101 0001 : 11 001 qwordreg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>0100 00XB 1101 000w : mod 001 r/m</td>
</tr>
<tr>
<td>memory8 by 1</td>
<td>0100 00XB 1101 0000 : mod 001 r/m</td>
</tr>
<tr>
<td>memory64 by 1</td>
<td>0100 10XB 1101 0001 : mod 001 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 000B 1101 001w : 11 001 reg</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>byte register by CL</td>
<td>0100 000B 1101 0010 : 11 001 bytereg</td>
</tr>
<tr>
<td>qword register by CL</td>
<td>0100 100B 1101 0011 : 11 001 qwordreg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0100 00XB 1101 001w : mod 001 r/m</td>
</tr>
<tr>
<td>memory8 by CL</td>
<td>0100 00XB 1101 0010 : mod 001 r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 10XB 1101 0011 : mod 001 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>0100 000B 1100 000w : 11 001 reg : imm8</td>
</tr>
<tr>
<td>byte register by immediate count</td>
<td>0100 000B 1100 0000 : 11 001 reg : imm8</td>
</tr>
<tr>
<td>qword register by immediate count</td>
<td>0100 100B 1100 0001 : 11 001 qwordreg : imm8</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0100 00XB 1100 000w : mod 001 r/m : imm8</td>
</tr>
<tr>
<td>memory8 by immediate count</td>
<td>0100 00XB 1100 0000 : mod 001 r/m : imm8</td>
</tr>
<tr>
<td>memory64 by immediate count</td>
<td>0100 10XB 1100 0001 : mod 001 r/m : imm8</td>
</tr>
<tr>
<td>RSM – Resume from System Management Mode</td>
<td>0000 1111 : 1010 1010</td>
</tr>
<tr>
<td>SAL – Shift Arithmetic Left</td>
<td>same instruction as SHL</td>
</tr>
<tr>
<td>SAR – Shift Arithmetic Right</td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>0100 000B 1101 000w : 11 111 reg</td>
</tr>
<tr>
<td>byte register by 1</td>
<td>0100 000B 1101 0000 : 11 111 bytereg</td>
</tr>
<tr>
<td>qword register by 1</td>
<td>0100 100B 1101 0001 : 11 111 qwordreg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>0100 00XB 1101 000w : mod 111 r/m</td>
</tr>
<tr>
<td>memory8 by 1</td>
<td>0100 00XB 1101 0000 : mod 111 r/m</td>
</tr>
<tr>
<td>memory64 by 1</td>
<td>0100 10XB 1101 0001 : mod 111 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 000B 1101 001w : 11 111 reg</td>
</tr>
<tr>
<td>byte register by CL</td>
<td>0100 000B 1101 0010 : 11 111 bytereg</td>
</tr>
<tr>
<td>qword register by CL</td>
<td>0100 100B 1101 0011 : 11 111 qwordreg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0100 00XB 1101 001w : mod 111 r/m</td>
</tr>
<tr>
<td>memory8 by CL</td>
<td>0100 00XB 1101 0010 : mod 111 r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 10XB 1101 0011 : mod 111 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>0100 000B 1100 000w : 11 111 reg : imm8</td>
</tr>
<tr>
<td>byte register by immediate count</td>
<td>0100 000B 1100 0000 : 11 111 bytereg : imm8</td>
</tr>
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</table>
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<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>qwordregister by immediate count</td>
<td>0100 100B 1100 0001 : 11 111 qwordreg : immB</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0100 00XB 1100 000w : mod 111 r/m : imm8</td>
</tr>
<tr>
<td>memory8 by immediate count</td>
<td>0100 00XB 1100 0000 : mod 111 r/m : imm8</td>
</tr>
<tr>
<td>memory64 by immediate count</td>
<td>0100 10XB 1100 0001 : mod 111 r/m : imm8</td>
</tr>
<tr>
<td><strong>SBB – Integer Subtraction with Borrow</strong></td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0100 0R0B 0001 100w : 11 reg1 reg2</td>
</tr>
<tr>
<td>byteregister1 to byteregister2</td>
<td>0100 0R0B 0001 1000 : 11 bytereg1 bytereg2</td>
</tr>
<tr>
<td>quadregister1 to quadregister2</td>
<td>0100 1R0B 0001 1001 : 11 quadreg1 quadreg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0R0B 0001 101w : 11 reg1 reg2</td>
</tr>
<tr>
<td>byteregister2 to byteregister1</td>
<td>0100 0R0B 0001 1010 : 11 reg1 bytereg2</td>
</tr>
<tr>
<td>byteregister2 to quadregister2</td>
<td>0100 1R0B 0001 1011 : 11 reg1 bytereg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0100 0RXB 0001 101w : mod reg r/m</td>
</tr>
<tr>
<td>memory8 to byteregister</td>
<td>0100 0RXB 0001 1010 : mod bytereg r/m</td>
</tr>
<tr>
<td>memory64 to byteregister</td>
<td>0100 1RXB 0001 1011 : mod quadreg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0100 0RXB 0001 100w : mod reg r/m</td>
</tr>
<tr>
<td>byteregister to memory8</td>
<td>0100 0RXB 0001 1000 : mod reg r/m</td>
</tr>
<tr>
<td>quadregister to memory64</td>
<td>0100 1RXB 0001 1001 : mod reg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>0100 000B 1000 00sw : 11 011 reg : imm</td>
</tr>
<tr>
<td>immediate8 to byteregister</td>
<td>0100 000B 1000 0000 : 11 011 bytereg : imm8</td>
</tr>
<tr>
<td>immediate32 to qwordregister</td>
<td>0100 100B 1000 0001 : 11 011 qwordreg : imm32</td>
</tr>
<tr>
<td>immediate8 to qwordregister</td>
<td>0100 100B 1000 0011 : 11 011 qwordreg : imm8</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0100 000B 0001 110w : imm</td>
</tr>
<tr>
<td>immediate32 to RAL</td>
<td>0100 1000 0001 1101 : imm32</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>0100 00XB 1000 00sw : mod 011 r/m : imm</td>
</tr>
<tr>
<td>immediate8 to memory8</td>
<td>0100 00XB 1000 0000 : mod 011 r/m : imm8</td>
</tr>
<tr>
<td>immediate32 to memory64</td>
<td>0100 10XB 1000 0001 : mod 011 r/m : imm32</td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>immediate8 to memory64</td>
<td>0100 10XB 1000 0011 : mod 011 r/m : imm8</td>
</tr>
<tr>
<td>SCAS/SCASB/SCASW/SCASD – Scan String</td>
<td></td>
</tr>
<tr>
<td>scan string</td>
<td>1010 111w</td>
</tr>
<tr>
<td>scan string (compare AL with byte at RDI)</td>
<td>0100 1000 1010 1110</td>
</tr>
<tr>
<td>scan string (compare RAX with qword at RDI)</td>
<td>0100 1000 1010 1111</td>
</tr>
<tr>
<td>SETcc – Byte Set on Condition</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>0100 000B 0000 1111 : 1001 tttn : 11 000 reg</td>
</tr>
<tr>
<td>register</td>
<td>0100 0000 0000 1111 : 1001 tttn : 11 000 reg</td>
</tr>
<tr>
<td>memory</td>
<td>0100 00XB 0000 1111 : 1001 tttn : mod 000 r/m</td>
</tr>
<tr>
<td>memory</td>
<td>0100 0000 0000 1111 : 1001 tttn : mod 000 r/m</td>
</tr>
<tr>
<td>SGDT – Store Global Descriptor Table Register</td>
<td>0000 1111 : 0000 0001 : modA 000 r/m</td>
</tr>
<tr>
<td>SHL – Shift Left</td>
<td></td>
</tr>
<tr>
<td>register by 1</td>
<td>0100 000B 1101 0000w : 11 100 reg</td>
</tr>
<tr>
<td>byteregister by 1</td>
<td>0100 000B 1101 0000 : 11 100 bytereg</td>
</tr>
<tr>
<td>qwordregister by 1</td>
<td>0100 100B 1101 0001 : 11 100 qwordreg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>0100 00XB 1101 000w : mod 100 r/m</td>
</tr>
<tr>
<td>memory8 by 1</td>
<td>0100 00XB 1101 0000 : mod 100 r/m</td>
</tr>
<tr>
<td>memory64 by 1</td>
<td>0100 10XB 1101 0001 : mod 100 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 000B 1101 001w : 11 100 reg</td>
</tr>
<tr>
<td>byteregister by CL</td>
<td>0100 000B 1101 0010 : 11 100 bytereg</td>
</tr>
<tr>
<td>qwordregister by CL</td>
<td>0100 100B 1101 0011 : 11 100 qwordreg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0100 00XB 1101 001w : mod 100 r/m</td>
</tr>
<tr>
<td>memory8 by CL</td>
<td>0100 00XB 1101 0010 : mod 100 r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 10XB 1101 0011 : mod 100 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>0100 000B 1100 000w : 11 100 reg : imm8</td>
</tr>
<tr>
<td>byteregister by immediate count</td>
<td>0100 000B 1100 0000 : 11 100 bytereg : imm8</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>quadregister by immediate count</td>
<td>0100 100B 1100 0001 : 11 100 quadreg : imm8</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0100 00XB 1100 000w : mod 100 r/m : imm8</td>
</tr>
<tr>
<td>memory8 by immediate count</td>
<td>0100 00XB 1100 0000 : mod 100 r/m : imm8</td>
</tr>
<tr>
<td>memory64 by immediate count</td>
<td>0100 10XB 1100 0001 : mod 100 r/m : imm8</td>
</tr>
</tbody>
</table>

**SHLD – Double Precision Shift Left**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register by immediate count</td>
<td>0100 0R0B 0000 1111 : 1010 0100 : 11 reg2</td>
</tr>
<tr>
<td>qwordregister by immediate8</td>
<td>0100 1R0B 0000 1111 : 1010 0100 : 11 qwordreg2 qwordreg1 : imm8</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0100 0RXB 0000 1111 : 1010 0100 : mod reg r/m : imm8</td>
</tr>
<tr>
<td>memory64 by immediate8</td>
<td>0100 1RXB 0000 1111 : 1010 0100 : mod qwordreg r/m : imm8</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 0R0B 0000 1111 : 1010 0101 : 11 reg2</td>
</tr>
<tr>
<td>quadregister by CL</td>
<td>0100 1R0B 0000 1111 : 1010 0101 : 11 quadreg2 quadreg1</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0100 00XB 0000 1111 : 1010 0101 : mod reg r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 1RXB 0000 1111 : 1010 0101 : mod quadreg r/m</td>
</tr>
</tbody>
</table>

**SHR – Shift Right**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register by 1</td>
<td>0100 000B 1101 000w : 11 101 reg</td>
</tr>
<tr>
<td>byteregister by 1</td>
<td>0100 000B 1101 0000 : 11 101 bytereg</td>
</tr>
<tr>
<td>qwordregister by 1</td>
<td>0100 100B 1101 0001 : 11 101 qwordreg</td>
</tr>
<tr>
<td>memory by 1</td>
<td>0100 00XB 1101 000w : mod 101 r/m</td>
</tr>
<tr>
<td>memory8 by 1</td>
<td>0100 00XB 1101 0000 : mod 101 r/m</td>
</tr>
<tr>
<td>memory64 by 1</td>
<td>0100 10XB 1101 0001 : mod 101 r/m</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 000B 1101 001w : 11 101 reg</td>
</tr>
<tr>
<td>byteregister by CL</td>
<td>0100 000B 1101 0010 : 11 101 bytereg</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>qwordregister by CL</td>
<td>0100 100B 1101 0011 : 11 101 qwordreg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0100 00XB 1101 001w : mod 101 r/m</td>
</tr>
<tr>
<td>memory8 by CL</td>
<td>0100 00XB 1101 0010 : mod 101 r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 10XB 1101 0011 : mod 101 r/m</td>
</tr>
<tr>
<td>register by immediate count</td>
<td>0100 000B 1100 000w : 11 101 reg : imm8</td>
</tr>
<tr>
<td>byteregister by immediate count</td>
<td>0100 100B 1100 0011 : 11 101 reg : imm8</td>
</tr>
<tr>
<td>qwordregister by immediate count</td>
<td>0100 000B 1100 000w : mod 101 r/m : imm8</td>
</tr>
<tr>
<td>memory8 by immediate count</td>
<td>0100 000B 1100 0000 : mod 101 r/m : imm8</td>
</tr>
<tr>
<td>memory64 by immediate count</td>
<td>0100 100B 1100 0011 : mod 101 r/m : imm8</td>
</tr>
</tbody>
</table>

**SHRD – Double Precision Shift Right**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>register by immediate count</td>
<td>0100 000B 0000 1111 : 1010 1100 : 11 reg2</td>
</tr>
<tr>
<td>qwordregister by immediate8</td>
<td>0100 100B 0000 1111 : 1010 1100 : 11 qwordreg</td>
</tr>
<tr>
<td>memory by immediate count</td>
<td>0100 000B 0000 1111 : mod reg r/m : imm8</td>
</tr>
<tr>
<td>memory64 by immediate8</td>
<td>0100 100B 0000 1111 : mod qwordreg r/m : imm8</td>
</tr>
<tr>
<td>register by CL</td>
<td>0100 000B 0000 1111 : 1010 1101 : 11 reg2</td>
</tr>
<tr>
<td>qwordregister by CL</td>
<td>0100 100B 0000 1111 : 1010 1101 : 11 qwordreg</td>
</tr>
<tr>
<td>memory by CL</td>
<td>0000 1111 : 1010 1101 : mod reg r/m</td>
</tr>
<tr>
<td>memory64 by CL</td>
<td>0100 100B 0000 1111 : mod qwordreg r/m</td>
</tr>
</tbody>
</table>

**SIDT – Store Interrupt Descriptor Table Register**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>to register</td>
<td>0000 1111 : 0000 0000 : 11 000 reg</td>
</tr>
</tbody>
</table>

**SLDT – Store Local Descriptor Table Register**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>to register</td>
<td>0100 000B 0000 1111 : 0000 0000 : 11 000 reg</td>
</tr>
</tbody>
</table>
Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>to memory</td>
<td>0100 000B 0000 1111 : 0000 0000 : mod 000 r/m</td>
</tr>
<tr>
<td><strong>SMSW – Store Machine Status Word</strong></td>
<td></td>
</tr>
<tr>
<td>to register</td>
<td>0100 000B 0000 1111 : 0000 0001 : 11 100 reg</td>
</tr>
<tr>
<td>to memory</td>
<td>0100 000B 0000 1111 : 0000 0001 : mod 100 r/m</td>
</tr>
<tr>
<td><strong>STC – Set Carry Flag</strong></td>
<td>1111 1001</td>
</tr>
<tr>
<td><strong>STD – Set Direction Flag</strong></td>
<td>1111 1101</td>
</tr>
<tr>
<td><strong>STI – Set Interrupt Flag</strong></td>
<td>1111 1011</td>
</tr>
<tr>
<td><strong>STOS/STOSB/STOSW/STOSD/STOSQ – Store String Data</strong></td>
<td></td>
</tr>
<tr>
<td>store string data</td>
<td>1010 101w</td>
</tr>
<tr>
<td>store string data (RAX at address RDI)</td>
<td>0100 1000 1010 1011</td>
</tr>
<tr>
<td><strong>STR – Store Task Register</strong></td>
<td></td>
</tr>
<tr>
<td>to register</td>
<td>0100 000B 0000 1111 : 0000 0000 : 11 001 reg</td>
</tr>
<tr>
<td>to memory</td>
<td>0100 000B 0000 1111 : 0000 0000 : mod 001 r/m</td>
</tr>
<tr>
<td><strong>SUB – Integer Subtraction</strong></td>
<td></td>
</tr>
<tr>
<td>register1 from register2</td>
<td>0100 0R0B 0010 100w : 11 reg1 reg2</td>
</tr>
<tr>
<td>byteregister1 from byteregister2</td>
<td>0100 0R0B 0010 1000 : 11 bytereg1 bytereg2</td>
</tr>
<tr>
<td>qwordregister1 from qwordregister2</td>
<td>0100 1R0B 0010 1000 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register2 from register1</td>
<td>0100 0R0B 0010 101w : 11 reg1 reg2</td>
</tr>
<tr>
<td>byteregister2 from byteregister1</td>
<td>0100 0R0B 0010 1010 : 11 bytereg1 bytereg2</td>
</tr>
<tr>
<td>qwordregister2 from qwordregister1</td>
<td>0100 1R0B 0010 1011 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory from register</td>
<td>0100 000B 0010 101w : mod reg r/m</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory8 from byteregister</td>
<td>0100 0RXB 0010 1010 : mod bytereg r/m</td>
</tr>
<tr>
<td>memory64 from qwordregister</td>
<td>0100 1RXB 0010 1011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>register from memory</td>
<td>0100 0RXB 0010 100w : mod reg r/m</td>
</tr>
<tr>
<td>byteregister from memory8</td>
<td>0100 0RXB 0010 1000 : mod bytereg r/m</td>
</tr>
<tr>
<td>qwordregister from memory8</td>
<td>0100 1RXB 0010 1000 : mod qwordreg r/m</td>
</tr>
<tr>
<td>immediate from register</td>
<td>0100 000B 1000 00sw : 11 101 reg : imm</td>
</tr>
<tr>
<td>immediate8 from byteregister</td>
<td>0100 000B 1000 0000 : 11 101 bytereg : imm8</td>
</tr>
<tr>
<td>immediate32 from qwordregister</td>
<td>0100 100B 1000 0001 : 11 101 qwordreg : imm32</td>
</tr>
<tr>
<td>immediate8 from qwordregister</td>
<td>0100 100B 1000 0011 : 11 101 qwordreg : imm8</td>
</tr>
<tr>
<td>immediate from AL, AX, or EAX</td>
<td>0100 000B 0010 110w : imm</td>
</tr>
<tr>
<td>immediate32 from RAX</td>
<td>0100 1000 0010 1101 : imm32</td>
</tr>
<tr>
<td>immediate from memory</td>
<td>0100 00XB 1000 00sw : mod 101 r/m : imm</td>
</tr>
<tr>
<td>immediate8 from memory8</td>
<td>0100 00XB 1000 0000 : mod 101 r/m : imm8</td>
</tr>
<tr>
<td>immediate32 from memory64</td>
<td>0100 10XB 1000 0001 : mod 101 r/m : imm32</td>
</tr>
<tr>
<td>immediate8 from memory64</td>
<td>0100 10XB 1000 0011 : mod 101 r/m : imm8</td>
</tr>
</tbody>
</table>

**SWAPGS – Swap GS Base Register**

- GS base register value for value in MSR C0000102H
  - 0000 1111 0000 0001 [this one incomplete]

**SYSCALL – Fast System Call**

- fast call to privilege level 0 system procedures
  - 0000 1111 0000 0101

**SYSRET – Return From Fast System Call**

- return from fast system call
  - 0000 1111 0000 0111

**TEST – Logical Compare**

- register1 and register2
  - 0100 0R0B 1000 010w : 11 reg1 reg2
- byteregister1 and byteregister2
  - 0100 0R0B 1000 0100 : 11 bytereg1 bytereg2
### INSTRUCTION FORMATS AND ENCODINGS

**Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>qwordregister1 and qwordregister2</td>
<td>0100 1R0B 1000 0101 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory and register</td>
<td>0100 0R0B 1000 010w : mod reg r/m</td>
</tr>
<tr>
<td>memory8 and byteregister</td>
<td>0100 0RXB 1000 0100 : mod bytereg r/m</td>
</tr>
<tr>
<td>memory64 and qwordregister</td>
<td>0100 1RXB 1000 0101 : mod qwordreg r/m</td>
</tr>
<tr>
<td>immediate and register</td>
<td>0100 000B 1111 011w : 11 000 reg : imm</td>
</tr>
<tr>
<td>immediate8 and byteregister</td>
<td>0100 000B 1111 0110 : 11 000 bytereg : imm8</td>
</tr>
<tr>
<td>immediate32 and qwordregister</td>
<td>0100 100B 1111 0111 : 11 000 bytereg : imm8</td>
</tr>
<tr>
<td>immediate and AL, AX, or EAX</td>
<td>0100 000B 1010 100w : imm</td>
</tr>
<tr>
<td>immediate32 and RAX</td>
<td>0100 1000 1010 1001 : imm32</td>
</tr>
<tr>
<td>immediate and memory</td>
<td>0100 00XB 1111 011w : mod 000 r/m : imm</td>
</tr>
<tr>
<td>immediate8 and memory8</td>
<td>0100 1000 1111 0110 : mod 000 r/m : imm8</td>
</tr>
<tr>
<td>immediate32 and memory64</td>
<td>0100 1000 1111 0111 : mod 000 r/m : imm32</td>
</tr>
<tr>
<td>UD2 – Undefined instruction</td>
<td>0000 FFFF : 0000 1011</td>
</tr>
<tr>
<td>VERR – Verify a Segment for Reading</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>0100 000B 0000 1111 : 0000 0000 : 11 100 reg</td>
</tr>
<tr>
<td>memory</td>
<td>0100 00XB 0000 1111 : 0000 0000 : mod 100 r/m</td>
</tr>
<tr>
<td>VERW – Verify a Segment for Writing</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>0100 000B 0000 1111 : 0000 0000 : 11 101 reg</td>
</tr>
<tr>
<td>memory</td>
<td>0100 00XB 0000 1111 : 0000 0000 : mod 101 r/m</td>
</tr>
<tr>
<td>WAIT – Wait</td>
<td>1001 1011</td>
</tr>
<tr>
<td>WBINVD – Writeback and Invalidate Data Cache</td>
<td>0000 1111 : 0000 1001</td>
</tr>
<tr>
<td>WRMSR – Write to Model-Specific Register</td>
<td></td>
</tr>
<tr>
<td>write EDX:EAX to ECX specified MSR</td>
<td>0000 1111 : 0011 0000</td>
</tr>
</tbody>
</table>
## INSTRUCTION FORMATS AND ENCODINGS

### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>write RDX[31:0]RAX[31:0] to RCX specified MSR</td>
<td>0100 1000 0000 1111 : 0011 0000</td>
</tr>
<tr>
<td><strong>XADD - Exchange and Add</strong></td>
<td></td>
</tr>
<tr>
<td>register1, register2</td>
<td>0100 0R0B 0000 1111 : 1100 000w : 11 reg2 reg1</td>
</tr>
<tr>
<td>byteregister1, byteregister2</td>
<td>0100 0R0B 0000 1111 : 1100 0000 : 11 bytereg2 bytereg1</td>
</tr>
<tr>
<td>qwordregister1, qwordregister2</td>
<td>0100 0R0B 0000 1111 : 1100 0001 : 11 qwordreg2 qwordreg1</td>
</tr>
<tr>
<td>memory, register</td>
<td>0100 ORXB 0000 1111 : 1100 000w : mod reg r/m</td>
</tr>
<tr>
<td>memory8, bytereg</td>
<td>0100 1RXB 0000 1111 : 1100 0000 : mod bytereg r/m</td>
</tr>
<tr>
<td>memory64, qwordreg</td>
<td>0100 1RXB 0000 1111 : 1100 0001 : mod qwordreg r/m</td>
</tr>
<tr>
<td><strong>XCHG - Exchange Register/Memory with Register</strong></td>
<td></td>
</tr>
<tr>
<td>register1 with register2</td>
<td>1000 011w : 11 reg1 reg2</td>
</tr>
<tr>
<td>AX or EAX with register</td>
<td>1001 0 reg</td>
</tr>
<tr>
<td>memory with register</td>
<td>1000 011w : mod reg r/m</td>
</tr>
<tr>
<td><strong>XLAT/XLATB - Table Look-up Translation</strong></td>
<td></td>
</tr>
<tr>
<td>AL to byte DS[(E)BX + unsigned AL]</td>
<td>1101 0111</td>
</tr>
<tr>
<td>AL to byte DS[RBX + unsigned AL]</td>
<td>0100 1000 1101 0111</td>
</tr>
<tr>
<td><strong>XOR - Logical Exclusive OR</strong></td>
<td></td>
</tr>
<tr>
<td>register1 to register2</td>
<td>0100 0RXB 0011 0000w : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>byteregister1 to byteregister2</td>
<td>0100 0R0B 0011 0000 : 11 bytereg1 bytereg2</td>
</tr>
<tr>
<td>qwordregister1 to qwordregister2</td>
<td>0100 1R0B 0011 0001 : 11 qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0R0B 0011 001w : 11 reg1 reg2</td>
</tr>
<tr>
<td>byteregister2 to byteregister1</td>
<td>0100 0R0B 0011 0010 : 11 bytereg1 bytereg2</td>
</tr>
<tr>
<td>qwordregister2 to qwordregister1</td>
<td>0100 1R0B 0011 0011 : 11 qwordreg1 qwordreg2</td>
</tr>
</tbody>
</table>
### Table B-15. General Purpose Instruction Formats and Encodings for 64-Bit Mode (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory to register</td>
<td>0100 0RXB 0011 001w : mod reg r/m</td>
</tr>
<tr>
<td>memory8 to byteregister</td>
<td>0100 0RXB 0011 0010 : mod bytereg r/m</td>
</tr>
<tr>
<td>memory64 to qwordregister</td>
<td>0100 1RXB 0011 0011 : mod qwordreg r/m</td>
</tr>
<tr>
<td>register to memory</td>
<td>0100 0RXB 0011 000w : mod reg r/m</td>
</tr>
<tr>
<td>byteregister to memory8</td>
<td>0100 0RXB 0011 0000 : mod bytereg r/m</td>
</tr>
<tr>
<td>qwordregister to memory8</td>
<td>0100 1RXB 0011 0001 : mod qwordreg r/m</td>
</tr>
<tr>
<td>immediate to register</td>
<td>0100 000B 1000 00sw : 11 110 reg : imm</td>
</tr>
<tr>
<td>immediate8 to byteregister</td>
<td>0100 000B 1000 0000 : 11 110 bytereg : imm8</td>
</tr>
<tr>
<td>immediate32 to qwordregister</td>
<td>0100 100B 1000 0001 : 11 110 qwordreg : imm32</td>
</tr>
<tr>
<td>immediate8 to qwordregister</td>
<td>0100 100B 1000 0011 : 11 110 qwordreg : imm8</td>
</tr>
<tr>
<td>immediate to AL, AX, or EAX</td>
<td>0100 000B 0011 010w : imm</td>
</tr>
<tr>
<td>immediate to RAX</td>
<td>0100 1000 0011 0101 : immediate data</td>
</tr>
<tr>
<td>immediate to memory</td>
<td>0100 00XB 1000 00sw : mod 110 r/m : imm</td>
</tr>
<tr>
<td>immediate8 to memory8</td>
<td>0100 00XB 1000 0000 : mod 110 r/m : imm8</td>
</tr>
<tr>
<td>immediate32 to memory64</td>
<td>0100 10XB 1000 0001 : mod 110 r/m : imm32</td>
</tr>
<tr>
<td>immediate8 to memory64</td>
<td>0100 10XB 1000 0011 : mod 110 r/m : imm8</td>
</tr>
</tbody>
</table>

### Prefix Bytes

<table>
<thead>
<tr>
<th>Prefix Bytes</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>address size</td>
<td>0111 0111</td>
</tr>
<tr>
<td>LOCK</td>
<td>1111 0000</td>
</tr>
<tr>
<td>operand size</td>
<td>0111 0110</td>
</tr>
<tr>
<td>CS segment override</td>
<td>0010 1110</td>
</tr>
<tr>
<td>DS segment override</td>
<td>0011 1110</td>
</tr>
<tr>
<td>ES segment override</td>
<td>0010 0110</td>
</tr>
<tr>
<td>FS segment override</td>
<td>0110 0100</td>
</tr>
<tr>
<td>GS segment override</td>
<td>0110 0101</td>
</tr>
<tr>
<td>SS segment override</td>
<td>0011 0110</td>
</tr>
</tbody>
</table>
INSTRUCTION FORMATS AND ENCODINGS

B.3 PENTIUM® PROCESSOR FAMILY INSTRUCTION FORMATS AND ENCODINGS

The following table shows formats and encodings introduced by the Pentium processor family.

Table B-16. Pentium Processor Family Instruction Formats and Encodings, Non-64-Bit Modes

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPXCHG8B – Compare and Exchange 8 Bytes</td>
<td>0000 1111 : 1100 0111 : mod 001 r/m</td>
</tr>
<tr>
<td>EDX:EAX with memory64</td>
<td>0000 1111 : 1100 0111 : mod 001 r/m</td>
</tr>
</tbody>
</table>

Table B-17. Pentium Processor Family Instruction Formats and Encodings, 64-Bit Mode

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPXCHG8B/CMPXCHG16B – Compare and Exchange Bytes</td>
<td>0000 1111 : 1100 0111 : mod 001 r/m</td>
</tr>
<tr>
<td>EDX:EAX with memory64</td>
<td>0000 1111 : 1100 0111 : mod 001 r/m</td>
</tr>
<tr>
<td>RDX:RAX with memory128</td>
<td>0100 10XB 0000 1111 : 1100 0111 : mod 001 r/m</td>
</tr>
</tbody>
</table>

B.4 64-BIT MODE INSTRUCTION ENCODINGS FOR SIMD INSTRUCTION EXTENSIONS

Non-64-bit mode instruction encodings for MMX Technology, SSE, SSE2, and SSE3 are covered by applying these rules to Table B-19 through Table B-31. Table B-34 lists special encodings (instructions that do not follow the rules below).

1. The REX instruction has no effect:
   - On immediates
   - If both operands are MMX registers
   - On MMX registers and XMM registers
   - If an MMX register is encoded in the reg field of the ModR/M byte

2. If a memory operand is encoded in the r/m field of the ModR/M byte, REX.X and REX.B may be used for encoding the memory operand.
3. If a general-purpose register is encoded in the r/m field of the ModR/M byte, REX.B may be used for register encoding and REX.W may be used to encode the 64-bit operand size.

4. If an XMM register operand is encoded in the reg field of the ModR/M byte, REX.R may be used for register encoding. If an XMM register operand is encoded in the r/m field of the ModR/M byte, REX.B may be used for register encoding.

B.5 MMX INSTRUCTION FORMATS AND ENCODINGS

MMX instructions, except the EMMS instruction, use a format similar to the 2-byte Intel Architecture integer format. Details of subfield encodings within these formats are presented below.

B.5.1 Granularity Field (gg)

The granularity field (gg) indicates the size of the packed operands that the instruction is operating on. When this field is used, it is located in bits 1 and 0 of the second opcode byte. Table B-18 shows the encoding of the gg field.

<table>
<thead>
<tr>
<th>gg</th>
<th>Granularity of Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Packed Bytes</td>
</tr>
<tr>
<td>01</td>
<td>Packed Words</td>
</tr>
<tr>
<td>10</td>
<td>Packed Doublewords</td>
</tr>
<tr>
<td>11</td>
<td>Quadword</td>
</tr>
</tbody>
</table>

B.5.2 MMX Technology and General-Purpose Register Fields (mmxreg and reg)

When MMX technology registers (mmxreg) are used as operands, they are encoded in the ModR/M byte in the reg field (bits 5, 4, and 3) and/or the R/M field (bits 2, 1, and 0).

If an MMX instruction operates on a general-purpose register (reg), the register is encoded in the R/M field of the ModR/M byte.

B.5.3 MMX Instruction Formats and Encodings Table

Table B-19 shows the formats and encodings of the integer instructions.
## INSTRUCTION FORMATS AND ENCODINGS

### Table B-19. MMX Instruction Formats and Encodings

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EMMS</strong> – Empty MMX technology state</td>
<td>0000 1111:01110111</td>
</tr>
<tr>
<td><strong>MOVD</strong> – Move doubleword</td>
<td></td>
</tr>
<tr>
<td>reg to mmxreg</td>
<td>0000 1111:0110 1110: mmxreg reg</td>
</tr>
<tr>
<td>reg from mmxreg</td>
<td>0000 1111:0111 1110: mmxreg reg</td>
</tr>
<tr>
<td>mem to mmxreg</td>
<td>0000 1111:0110 1110: mod mmxreg r/m</td>
</tr>
<tr>
<td>mem from mmxreg</td>
<td>0000 1111:0111 1110: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>MOVQ</strong> – Move quadword</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:0110 1111: mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mmxreg2 from mmxreg1</td>
<td>0000 1111:0111 1111: mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mem to mmxreg</td>
<td>0000 1111:0110 1111: mod mmxreg r/m</td>
</tr>
<tr>
<td>mem from mmxreg</td>
<td>0000 1111:0111 1111: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PACKSSDW1</strong> – Pack dword to word data (signed with saturation)</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:0110 1011: mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mem to mmxreg</td>
<td>0000 1111:0110 1011: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PACKSSWB1</strong> – Pack word to byte data (signed with saturation)</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:0110 0011: mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mem to mmxreg</td>
<td>0000 1111:0110 0011: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PACKUSWB1</strong> – Pack word to byte data (unsigned with saturation)</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:0110 0111: mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mem to mmxreg</td>
<td>0000 1111:0110 0111: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PADD</strong> – Add with wrap-around</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1111 11gg: mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mem to mmxreg</td>
<td>0000 1111:1111 11gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PADDS</strong> – Add signed with saturation</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1110 11gg: mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mem to mmxreg</td>
<td>0000 1111:1110 11gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PADDUS</strong> – Add unsigned with saturation</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1101 11gg: mmxreg1 mmxreg2</td>
</tr>
</tbody>
</table>
Table B-19. MMX Instruction Formats and Encodings (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:1110 11gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PAND - Bitwise And</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1101 1011: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:1101 1011: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PANDN - Bitwise AndNot</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1101 1111: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:1101 1111: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PCMPEQ - Packed compare for equality</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg1 with mmxreg2</td>
<td>0000 1111:0111 01gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mmxreg with memory</td>
<td>0000 1111:0111 01gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PCMPGT - Packed compare greater (signed)</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg1 with mmxreg2</td>
<td>0000 1111:0110 01gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mmxreg with memory</td>
<td>0000 1111:0110 01gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PMADDWD - Packed multiply add</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1111 0101: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:1111 0101: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PMULHUW - Packed multiplication, store high word (unsigned)</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1110 0100: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:1110 0100: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PMULHW - Packed multiplication, store high word</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1110 0101: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:1110 0101: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PMULLW - Packed multiplication, store low word</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1111 0101: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:1111 0101: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>POR - Bitwise Or</strong></td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:1110 1011: 11 mmxreg1 mmxreg2</td>
</tr>
</tbody>
</table>
### Table B-19. MMX Instruction Formats and Encodings (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:1110 1011: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PSLL</strong>(^2) – Packed shift left logical</td>
<td></td>
</tr>
<tr>
<td>mmxreg1 by mmxreg2</td>
<td>0000 1111:1111 00gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mmxreg by memory</td>
<td>0000 1111:1111 00gg: mod mmxreg r/m</td>
</tr>
<tr>
<td>mmxreg by immediate</td>
<td>0000 1111:0111 00gg: 11 110 mmxreg: imm8 data</td>
</tr>
<tr>
<td><strong>PSRA</strong>(^2) – Packed shift right arithmetic</td>
<td></td>
</tr>
<tr>
<td>mmxreg1 by mmxreg2</td>
<td>0000 1111:1111 00gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mmxreg by memory</td>
<td>0000 1111:1111 00gg: mod mmxreg r/m</td>
</tr>
<tr>
<td>mmxreg by immediate</td>
<td>0000 1111:0111 00gg: 11 100 mmxreg: imm8 data</td>
</tr>
<tr>
<td><strong>PSRL</strong>(^2) – Packed shift right logical</td>
<td></td>
</tr>
<tr>
<td>mmxreg1 by mmxreg2</td>
<td>0000 1111:1101 00gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>mmxreg by memory</td>
<td>0000 1111:1101 00gg: mod mmxreg r/m</td>
</tr>
<tr>
<td>mmxreg by immediate</td>
<td>0000 1111:0111 00gg: 11 010 mmxreg: imm8 data</td>
</tr>
<tr>
<td><strong>PSUB</strong> – Subtract with wrap-around</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 from mmxreg1</td>
<td>0000 1111:1111 10gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory from mmxreg</td>
<td>0000 1111:1111 10gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PSUBS</strong> – Subtract signed with saturation</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 from mmxreg1</td>
<td>0000 1111:1110 10gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory from mmxreg</td>
<td>0000 1111:1110 10gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PSUBUS</strong> – Subtract unsigned with saturation</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 from mmxreg1</td>
<td>0000 1111:1101 10gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory from mmxreg</td>
<td>0000 1111:1101 10gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PUNPCKH</strong> – Unpack high data to next larger type</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:0110 10gg: 11 mmxreg1 mmxreg2</td>
</tr>
<tr>
<td>memory to mmxreg</td>
<td>0000 1111:0110 10gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>PUNPCKL</strong> – Unpack low data to next larger type</td>
<td></td>
</tr>
<tr>
<td>mmxreg2 to mmxreg1</td>
<td>0000 1111:0110 00gg: 11 mmxreg1 mmxreg2</td>
</tr>
</tbody>
</table>
Table B-20 shows the formats and encodings for several instructions that relate to processor extended state management.

### Table B-20. Formats and Encodings of XSAVE/XRSTOR/XGETBV/XSETBV Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>XGETBV – Get Value of Extended Control Register</td>
<td>0000 1111:0000 0001: 1101 0000</td>
</tr>
<tr>
<td>XRSTOR – Restore Processor Extended States(^1)</td>
<td>0000 1111:1010 1110: mod(^1) 101 r/m</td>
</tr>
<tr>
<td>XSAVE – Save Processor Extended States(^2)</td>
<td>0000 1111:1010 1110: mod(^1) 100 r/m</td>
</tr>
<tr>
<td>XSETBV – Set Extended Control Register</td>
<td>0000 1111:0000 0001: 1101 0001</td>
</tr>
</tbody>
</table>

### B.6 PROCESSOR EXTENDED STATE INSTRUCTION FORMATS AND ENCODINGS

Table B-20 shows the formats and encodings for several instructions that relate to processor extended state management.

### Table B-20. Formats and Encodings of XSAVE/XRSTOR/XGETBV/XSETBV Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>XGETBV – Get Value of Extended Control Register</td>
<td>0000 1111:0000 0001: 1101 0000</td>
</tr>
<tr>
<td>XRSTOR – Restore Processor Extended States(^1)</td>
<td>0000 1111:1010 1110: mod(^1) 101 r/m</td>
</tr>
<tr>
<td>XSAVE – Save Processor Extended States(^2)</td>
<td>0000 1111:1010 1110: mod(^1) 100 r/m</td>
</tr>
<tr>
<td>XSETBV – Set Extended Control Register</td>
<td>0000 1111:0000 0001: 1101 0001</td>
</tr>
</tbody>
</table>

### B.7 P6 FAMILY INSTRUCTION FORMATS AND ENCODINGS

Table B-20 shows the formats and encodings for several instructions that were introduced into the IA-32 architecture in the P6 family processors.
The SSE instructions use the ModR/M format and are preceded by the 0FH prefix byte. In general, operations are not duplicated to provide two directions (that is, separate load and store variants).

The following three tables (Tables B-22, B-23, and B-24) show the formats and encodings for the SSE SIMD floating-point, SIMD integer, and cacheability and memory ordering instructions, respectively. Some SSE instructions require a mandatory prefix (66H, F2H, F3H) as part of the two-byte opcode. Mandatory prefixes are included in the tables.
<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDPS—Add Packed Single-Precision Floating-Point Values</td>
<td>0000 1111:0101 1000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 1000: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:11000111000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:11000111000: mod xmmreg r/m</td>
</tr>
<tr>
<td>ADDSS—Add Scalar Single-Precision Floating-Point Values</td>
<td>0000 1111:0101 1000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 1000: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:11000111000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:11000111000: mod xmmreg r/m</td>
</tr>
<tr>
<td>ANDNPS—Bitwise Logical AND NOT of Packed Single-Precision Floating-Point Values</td>
<td>0000 1111:0101 1000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 1000: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:11000111000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:11000111000: mod xmmreg r/m</td>
</tr>
<tr>
<td>ANDPS—Bitwise Logical AND of Packed Single-Precision Floating-Point Values</td>
<td>0000 1111:0101 1000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 1000: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:11000111000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:11000111000: mod xmmreg r/m</td>
</tr>
<tr>
<td>CMPPS—Compare Packed Single-Precision Floating-Point Values</td>
<td>0000 1111:1100 0010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0000 1111:1100 0010: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0000 1111:1100 0010: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td>CMPSS—Compare Scalar Single-Precision Floating-Point Values</td>
<td>1111 0011:0000 1111:1100 0010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>1111 0011:0000 1111:1100 0010: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>1111 0011:0000 1111:1100 0010: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td>COMISS—Compare Scalar Ordered Single-Precision Floating-Point Values and Set EFLAGS</td>
<td>0000 1111:0010 1111:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0010 1111: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0010 1111: mod xmmreg r/m</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>---------------------------------------------------------------------------------------</td>
<td>----------------------------------------------</td>
</tr>
<tr>
<td><strong>CVTPI2PS</strong>—Convert Packed Doubleword Integers to Packed Single-Precision Floating-Point Values</td>
<td></td>
</tr>
<tr>
<td>mmreg to xmmreg</td>
<td>0000 1111:0010 1010:11 xmmreg1 mmreg1</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0010 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>CVTPS2PI</strong>—Convert Packed Single-Precision Floating-Point Values to Packed Doubleword Integers</td>
<td></td>
</tr>
<tr>
<td>xmmreg to mmreg</td>
<td>0000 1111:0010 1101:11 mmreg1 xmmreg1</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0010 1101: mod mmreg r/m</td>
</tr>
<tr>
<td><strong>CVTSTI2SS</strong>—Convert Doubleword Integer to Scalar Single-Precision Floating-Point Value</td>
<td></td>
</tr>
<tr>
<td>r32 to xmmreg</td>
<td>1111 0011:0000 1111:00101010:11 xmmreg1 r32</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:00101010: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>CVTSS2SI</strong>—Convert Scalar Single-Precision Floating-Point Value to Doubleword Integer</td>
<td></td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>1111 0011:0000 1111:0010 1101:11 r32 xmmreg</td>
</tr>
<tr>
<td>mem to r32</td>
<td>1111 0011:0000 1111:0010 1101: mod r32 r/m</td>
</tr>
<tr>
<td><strong>CVTTPS2PI</strong>—Convert with Truncation Packed Single-Precision Floating-Point Values to Packed Doubleword Integers</td>
<td></td>
</tr>
<tr>
<td>xmmreg to mmreg</td>
<td>0000 1111:0010 1100:11 mmreg1 xmmreg1</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0010 1100: mod mmreg r/m</td>
</tr>
<tr>
<td><strong>CVTTSS2SI</strong>—Convert with Truncation Scalar Single-Precision Floating-Point Value to Doubleword Integer</td>
<td></td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>1111 0011:0000 1111:0010 1100:11 r32 xmmreg1</td>
</tr>
<tr>
<td>mem to r32</td>
<td>1111 0011:0000 1111:0010 1100: mod r32 r/m</td>
</tr>
<tr>
<td><strong>DIVPS</strong>—Divide Packed Single-Precision Floating-Point Values</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg</td>
<td>0000 1111:0101 1110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 1110: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>DIVSS</strong>—Divide Scalar Single-Precision Floating-Point Values</td>
<td></td>
</tr>
</tbody>
</table>

Table B-22. Formats and Encodings of SSE Floating-Point Instructions (Contd.)
### Table B-22. Formats and Encodings of SSE Floating-Point Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0101 1110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0101 1110: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>LDMXCSR—Load MXCSR Register State</strong></td>
<td></td>
</tr>
<tr>
<td>m32 to MXCSR</td>
<td>0000 1111:1010 1110:mod A 010 mem</td>
</tr>
<tr>
<td><strong>MAXPS—Return Maximum Packed Single-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 1111:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 1111: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MAXSS—Return Maximum Scalar Double-Precision Floating-Point Value</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0101 1111:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0101 1111: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MINPS—Return Minimum Packed Double-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 1101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 1101: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MINSS—Return Minimum Scalar Double-Precision Floating-Point Value</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0101 1101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0101 1101: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MOVAPS—Move Aligned Packed Single-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0010 1000:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>mem to xmmreg1</td>
<td>0000 1111:0010 1000: mod xmmreg r/m</td>
</tr>
<tr>
<td>xmmreg1 to xmmreg2</td>
<td>0000 1111:0010 1001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg1 to mem</td>
<td>0000 1111:0010 1001: mod xmmreg r/m</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
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<tr>
<td>---------------------------------------------------------------------------------------</td>
<td>-----------------------------------------------</td>
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<tr>
<td>MOVHLPS—Move Packed Single-Precision Floating-Point Values High to Low</td>
<td>0000 1111:0001 0010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVHPS—Move High Packed Single-Precision Floating-Point Values</td>
<td>0000 1111:0001 0110: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td></td>
</tr>
<tr>
<td>xmmreg to mem</td>
<td>0000 1111:0001 0111: mod xmmreg r/m</td>
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<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVLHPS—Move Packed Single-Precision Floating-Point Values Low to High</td>
<td>0000 1111:00010110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVLPS—Move Low Packed Single-Precision Floating-Point Values</td>
<td>0000 1111:0001 0010: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td></td>
</tr>
<tr>
<td>xmmreg to mem</td>
<td>0000 1111:0001 0011: mod xmmreg r/m</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVMSKPS—Extract Packed Single-Precision Floating-Point Sign Mask</td>
<td>0000 1111:0101 0000:11 r32 xmmreg</td>
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<tr>
<td>xmmreg to r32</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVSS—Move Scalar Single-Precision Floating-Point Values</td>
<td>1111 0011:0000 1111:0001 0000:11 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>xmmreg1</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg1</td>
<td>1111 0011:0000 1111:0001 0000: mod xmmreg r/m</td>
</tr>
<tr>
<td>xmmreg1 to xmmreg2</td>
<td>1111 0011:0000 1111:0001 0001:11 xmmreg1</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>xmmreg2</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg1</td>
<td>1111 0011:0000 1111:0001 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td>xmmreg1 to mem</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVUPS—Move Unaligned Packed Single-Precision Floating-Point Values</td>
<td>0000 1111:0001 0000:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg1</td>
<td>0000 1111:0001 0000: mod xmmreg r/m</td>
</tr>
<tr>
<td>xmmreg1 to xmmreg2</td>
<td>0000 1111:0001 0001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg1 to mem</td>
<td>0000 1111:0001 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------------------------------------------</td>
<td>-----------------------------------------------</td>
</tr>
<tr>
<td><strong>MULPS—Multiply Packed Single-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 1001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 1001:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MULSS—Multiply Scalar Single-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0101 1001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0101 1001:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>ORPS—Bitwise Logical OR of Single-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 0110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 0110:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>RCPSS—Compute Reciprocals of Scalar Single-Precision Floating-Point Value</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 0011:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 0011:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>RSQRTPS—Compute Reciprocals of Square Roots of Packed Single-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:01011011:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:01011011:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>RSQRTSS—Compute Reciprocals of Square Roots of Scalar Single-Precision Floating-Point Value</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0101 0010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0101 0010:mod xmmreg r/m</td>
</tr>
</tbody>
</table>
### Table B-22. Formats and Encodings of SSE Floating-Point Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SHUFPS—Shuffle Packed Single-Precision Floating-Point Values</strong></td>
<td>0000 1111:1100 0110:11 xmmreg1 xmmreg2: imm8</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0000 1111:1100 0110: mod xmmreg r/m:imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0000 1111:1100 0110: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>SQRTPS—Compute Square Roots of Packed Single-Precision Floating-Point Values</strong></td>
<td>0000 1111:0101 0001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>SQRTPS—Compute Square Root of Scalar Single-Precision Floating-Point Value</strong></td>
<td>1111 0011:0000 1111:0101 0001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0101 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0101 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>STMXCSR—Store MXCSR Register State</strong></td>
<td>0000 1111:1010 1110:modA 011 mem</td>
</tr>
<tr>
<td>MXCSR to mem</td>
<td>0000 1111:1010 1110:modA 011 mem</td>
</tr>
<tr>
<td><strong>SUBPS—Subtract Packed Single-Precision Floating-Point Values</strong></td>
<td>0000 1111:0101 1100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>SUBSS—Subtract Scalar Single-Precision Floating-Point Values</strong></td>
<td>1111 0011:0000 1111:0101 1100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0101 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0101 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>UCOMISS—Unordered Compare Scalar Ordered Single-Precision Floating-Point Values and Set EFLAGS</strong></td>
<td>0000 1111:0010 1110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0010 1110: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0010 1110: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>UNPCKHPS—Unpack and Interleave High Packed Single-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
</tbody>
</table>

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INSTRUCTION FORMATS AND ENCODINGS
<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0001 0101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0001 0101: mod xmmreg r/m</td>
</tr>
</tbody>
</table>

**UNPCKLPS—Unpack and Interleave Low Packed Single-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0001 0100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0001 0100: mod xmmreg r/m</td>
</tr>
</tbody>
</table>

**XORPS—Bitwise Logical XOR of Single-Precision Floating-Point Values**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0000 1111:0101 0111:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 0111: mod xmmreg r/m</td>
</tr>
</tbody>
</table>

### Table B-23. Formats and Encodings of SSE Integer Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PAVGB/PAVGw—Average Packed Integers</strong></td>
<td>0000 1111:1111:1110 0000:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1111:1110 0011:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:1111:1110 0000: mod mmreg r/m</td>
</tr>
<tr>
<td></td>
<td>0000 1111:1111:1110 0011: mod mmreg r/m</td>
</tr>
<tr>
<td><strong>PEXTRw—Extract Word</strong></td>
<td>0000 1111:1100 0101:11 r32 mmreg: imm8</td>
</tr>
<tr>
<td>mmreg to reg32, imm8</td>
<td>0000 1111:1100 0100:11 mmreg r32: imm8</td>
</tr>
<tr>
<td><strong>PINSRw—Insert Word</strong></td>
<td>0000 1111:1100 0100:11 mod mmreg r/m: imm8</td>
</tr>
<tr>
<td>reg32 to mmreg, imm8</td>
<td>0000 1111:1100 0100:11 mmreg r32: imm8</td>
</tr>
<tr>
<td>m16 to mmreg, imm8</td>
<td>0000 1111:1100 0100: mod mmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PMAXSw—Maximum of Packed Signed Word Integers</strong></td>
<td>0000 1111:1111:1110 1110:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1111:1110 1110: mod mmreg r/m</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:1111:1110 1110: mod mmreg r/m</td>
</tr>
<tr>
<td><strong>PMAXUB—Maximum of Packed Signed Byte Integers</strong></td>
<td>0000 1111:1111:1101 1110:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1111:1101 1110: mod mmreg r/m</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:1111:1101 1110: mod mmreg r/m</td>
</tr>
</tbody>
</table>
### Table B-23. Formats and Encodings of SSE Integer Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
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<tbody>
<tr>
<td><strong>PMINSW</strong>—Minimum of Packed Signed Word Integers</td>
<td></td>
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<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1110 1010:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:1110 1010: mod mmreg r/m</td>
</tr>
<tr>
<td><strong>PMINUB</strong>—Minimum of Packed Unsigned Byte Integers</td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1101 1010:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:1101 1010: mod mmreg r/m</td>
</tr>
<tr>
<td><strong>PMOVMSKB</strong>—Move Byte Mask To Integer</td>
<td></td>
</tr>
<tr>
<td>mmreg to reg32</td>
<td>0000 1111:1101 0111:11 r32 mmreg</td>
</tr>
<tr>
<td><strong>PMULHUW</strong>—Multiply Packed Unsigned Integers and Store High Result</td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1110 0100:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:1110 0100: mod mmreg r/m</td>
</tr>
<tr>
<td><strong>PSADBW</strong>—Compute Sum of Absolute Differences</td>
<td></td>
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<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1111 0110:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:1111 0110: mod mmreg r/m</td>
</tr>
<tr>
<td><strong>PSHUFW</strong>—Shuffle Packed Words</td>
<td></td>
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<tr>
<td>mmreg2 to mmreg1, imm8</td>
<td>0000 1111:0111 0000:11 mmreg1 mmreg2: imm8</td>
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<tr>
<td>mem to mmreg, imm8</td>
<td>0000 1111:0111 0000: mod mmreg r/m: imm8</td>
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### Table B-24. Format and Encoding of SSE Cacheability & Memory Ordering Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>MASKMOVQ</strong>—Store Selected Bytes of Quadword</td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1111 0111:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td><strong>MOVNTPS</strong>—Store Packed Single-Precision Floating-Point Values Using Non-Temporal Hint</td>
<td></td>
</tr>
<tr>
<td>xmmreg to mem</td>
<td>0000 1111:0010 1011: mod xmmreg r/m</td>
</tr>
</tbody>
</table>
INSTRUCTION FORMATS AND ENCODINGS

B.9 SSE2 INSTRUCTION FORMATS AND ENCODINGS

The SSE2 instructions use the ModR/M format and are preceded by the 0FH prefix byte. In general, operations are not duplicated to provide two directions (that is, separate load and store variants).

The following three tables show the formats and encodings for the SSE2 SIMD floating-point, SIMD integer, and cacheability instructions, respectively. Some SSE2 instructions require a mandatory prefix (66H, F2H, F3H) as part of the two-byte opcode. These prefixes are included in the tables.

**B.9.1 Granularity Field (gg)**

The granularity field (gg) indicates the size of the packed operands that the instruction is operating on. When this field is used, it is located in bits 1 and 0 of the second opcode byte. Table B-25 shows the encoding of this gg field.

<table>
<thead>
<tr>
<th>gg</th>
<th>Granularity of Data</th>
</tr>
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<tbody>
<tr>
<td>00</td>
<td>Packed Bytes</td>
</tr>
<tr>
<td>01</td>
<td>Packed Words</td>
</tr>
<tr>
<td>10</td>
<td>Packed Doublewords</td>
</tr>
<tr>
<td>11</td>
<td>Quadword</td>
</tr>
</tbody>
</table>

Table B-24. Format and Encoding of SSE Cacheability & Memory Ordering Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOVNTQ—Store Quadword Using Non-Temporal Hint</td>
<td>0000 1111:1110 0111: mod mmreg r/m</td>
</tr>
<tr>
<td>PREFETCHTO—Prefetch Temporal to All Cache Levels</td>
<td>0000 1111:0001 1000:modA 001 mem</td>
</tr>
<tr>
<td>PREFETCHT1—Prefetch Temporal to First Level Cache</td>
<td>0000 1111:0001 1000:modA 010 mem</td>
</tr>
<tr>
<td>PREFETCHT2—Prefetch Temporal to Second Level Cache</td>
<td>0000 1111:0001 1000:modA 011 mem</td>
</tr>
<tr>
<td>PREFETCHNTA—Prefetch Non-Temporal to All Cache Levels</td>
<td>0000 1111:0001 1000:modA 000 mem</td>
</tr>
<tr>
<td>SFENCE—Store Fence</td>
<td>0000 1111:1010 1110:11 111 000</td>
</tr>
</tbody>
</table>

Table B-25. Encoding of Granularity of Data Field (gg)
## Table B-26. Formats and Encodings of SSE2 Floating-Point Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDPD—Add Packed Double-Precision Floating-Point Values</td>
<td>0110 0110:0000 1111:0101 1000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 1000: mod xmmreg r/m</td>
</tr>
<tr>
<td>ADDSD—Add Scalar Double-Precision Floating-Point Values</td>
<td>1111 0010:0000 1111:0101 1000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0010:0000 1111:0101 1000: mod xmmreg r/m</td>
</tr>
<tr>
<td>ANDNPD—Bitwise Logical AND NOT of Packed Double-Precision Floating-Point Values</td>
<td>0110 0110:0000 1111:0101 0101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 0101: mod xmmreg r/m</td>
</tr>
<tr>
<td>ANDPD—Bitwise Logical AND of Packed Double-Precision Floating-Point Values</td>
<td>0110 0110:0000 1111:0101 0100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 0100: mod xmmreg r/m</td>
</tr>
<tr>
<td>CMPPD—Compare Packed Double-Precision Floating-Point Values</td>
<td>0110 0110:0000 1111:1100 0010:11 xmmreg1 xmmreg2: imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0110 0110:0000 1111:1100 0010: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td>CMPSD—Compare Scalar Double-Precision Floating-Point Values</td>
<td>1111 0010:0000 1111:1100 0010:11 xmmreg1 xmmreg2: imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>1111 0110:0000 1111:1100 0010: mod xmmreg r/m: imm8</td>
</tr>
</tbody>
</table>
### Instruction Formats and Encodings of SSE2 Floating-Point Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMISD—Compare Scalar Ordered Double-Precision Floating-Point Values and Set EFLAGS</td>
<td>0110 0110:0000 1111:0010 1111:11 xmmreg1 \ xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0010 1111:11 xmmreg1 \ xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0010 1111:11: mod xmmreg r/m</td>
</tr>
<tr>
<td>CVTPD2PI—Convert Packed Doubleword Integers to Packed Double-Precision Floating-Point Values</td>
<td>0110 0110:0000 1111:0010 1010:11 xmmreg1 \ xmmreg1</td>
</tr>
<tr>
<td>mmreg to xmmreg</td>
<td>0110 0110:0000 1111:0010 1010:11 xmmreg1 \ xmmreg1</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0010 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td>CVTSD2SI—Convert Scalar Double-Precision Floating-Point Value to Doubleword Integer</td>
<td>1111 0010:0000 1111:0010 1010:11 xmmreg r32</td>
</tr>
<tr>
<td>r32 to xmmreg1</td>
<td>1111 0010:0000 1111:0010 1010:11 xmmreg r32</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0010:0000 1111:0010 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td>CVTTPD2PI—Convert with Truncation Packed Double-Precision Floating-Point Values to Packed Doubleword Integers</td>
<td>1111 0010:0000 1111:0010 1101:11 r32 xmmreg</td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>1111 0010:0000 1111:0010 1101:11 r32 xmmreg</td>
</tr>
<tr>
<td>mem to r32</td>
<td>1111 0010:0000 1111:0010 1101: mod r32 r/m</td>
</tr>
<tr>
<td>CVTSI2SD—Convert Doubleword Integer to Scalar Double-Precision Floating-Point Value</td>
<td>0110 0110:0000 1111:0010 1111:0010 1111:11 xmmreg1</td>
</tr>
<tr>
<td>xmmreg to mmreg</td>
<td>0110 0110:0000 1111:0010 1111:0010 1111:11 xmmreg1</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0110 0110:0000 1111:0010 1111:0010 1111: mod xmmreg r/m</td>
</tr>
<tr>
<td>CVTPD2PI—Convert Packed Double-Precision Floating-Point Values to Packed Doubleword Integers</td>
<td>0110 0110:0000 1111:0010 1010:11 xmmreg1 \ xmmreg1</td>
</tr>
<tr>
<td>xmmreg to mmreg</td>
<td>0110 0110:0000 1111:0010 1010:11 xmmreg1 \ xmmreg1</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0110 0110:0000 1111:0010 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>CVTTSD2SI—Convert with Truncation Scalar Double-Precision Floating-Point Value to Doubleword Integer</td>
<td>1111 0010:0000 1111:0101 1010:11 r32 xmmreg</td>
</tr>
<tr>
<td>mem to r32</td>
<td>1111 0010:0000 1111:0100:11 r32</td>
</tr>
<tr>
<td>CVTPD2PS—Covert Packed Double-Precision Floating-Point Values to Packed Single-Precision Floating-Point Values</td>
<td>0110 0110:0000 1111:0101 1010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td>CVTPS2PD—Covert Packed Single-Precision Floating-Point Values to Packed Double-Precision Floating-Point Values</td>
<td>0000 1111:0101 1010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td>CVTSD2SS—Covert Scalar Double-Precision Floating-Point Value to Scalar Single-Precision Floating-Point Value</td>
<td>1111 0010:0000 1111:0101 1010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0010:0000 1111:0101 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td>CVTSS2SD—Covert Scalar Single-Precision Floating-Point Value to Scalar Double-Precision Floating-Point Value</td>
<td>1111 0011:0000 1111:0101 1010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0101 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>---------------------------------------------------------------------------------------</td>
<td>--------------------------------------------------------------------------</td>
</tr>
<tr>
<td>CVTPD2DQ—Convert Packed Double-Precision Floating-Point Values to Packed Doubleword Integers</td>
<td><code>xmmreg2</code> to <code>xmmreg1</code> 1111 0010:0000 1111:1110 0110:11 <code>xmmreg1</code> <code>xmmreg2</code></td>
</tr>
<tr>
<td></td>
<td><code>mem</code> to <code>xmmreg</code> 1111 0010:0000 1111:1110 0110:  mod <code>xmmreg</code> r/m</td>
</tr>
<tr>
<td>CVTTPD2DQ—Convert With Truncation Packed Double-Precision Floating-Point Values to Packed Doubleword Integers</td>
<td><code>xmmreg2</code> to <code>xmmreg1</code> 0110 0110:0000 1111:1110 0110:11 <code>xmmreg1</code> <code>xmmreg2</code></td>
</tr>
<tr>
<td></td>
<td><code>mem</code> to <code>xmmreg</code> 0110 0110:0000 1111:1110 0110:  mod <code>xmmreg</code> r/m</td>
</tr>
<tr>
<td>CVTDQ2PD—Convert Packed Doubleword Integers to Packed Single-Precision Floating-Point Values</td>
<td><code>xmmreg2</code> to <code>xmmreg1</code> 1111 0011:0000 1111:1110 0110:11 <code>xmmreg1</code> <code>xmmreg2</code></td>
</tr>
<tr>
<td></td>
<td><code>mem</code> to <code>xmmreg</code> 1111 0011:0000 1111:1110 0110:  mod <code>xmmreg</code> r/m</td>
</tr>
<tr>
<td>CVTPS2DQ—Convert Packed Single-Precision Floating-Point Values to Packed Doubleword Integers</td>
<td><code>xmmreg2</code> to <code>xmmreg1</code> 0110 0110:0000 1111:0101 1011:11 <code>xmmreg1</code> <code>xmmreg2</code></td>
</tr>
<tr>
<td></td>
<td><code>mem</code> to <code>xmmreg</code> 0110 0110:0000 1111:0101 1011:  mod <code>xmmreg</code> r/m</td>
</tr>
<tr>
<td>CVTTPS2DQ—Convert With Truncation Packed Single-Precision Floating-Point Values to Packed Doubleword Integers</td>
<td><code>xmmreg2</code> to <code>xmmreg1</code> 1111 0011:0000 1111:0101 1011:11 <code>xmmreg1</code> <code>xmmreg2</code></td>
</tr>
<tr>
<td></td>
<td><code>mem</code> to <code>xmmreg</code> 1111 0011:0000 1111:0101 1011:  mod <code>xmmreg</code> r/m</td>
</tr>
<tr>
<td>CVTDQ2PS—Convert Packed Doubleword Integers to Packed Double-Precision Floating-Point Values</td>
<td><code>xmmreg2</code> to <code>xmmreg1</code> 0000 1111:0101 1011:11 <code>xmmreg1</code> <code>xmmreg2</code></td>
</tr>
</tbody>
</table>

Table B-26. Formats and Encodings of SSE2 Floating-Point Instructions (Contd.)
### Table B-26. Formats and Encodings of SSE2 Floating-Point Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td>0000 1111:0101 1011: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>DIVPD—Divide Packed Double-Precision Floating-Point Values</strong></td>
<td>0110 0110:0000 1111:0101 1110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 1110: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>DIVSD—Divide Scalar Double-Precision Floating-Point Values</strong></td>
<td>1111 0010:0000 1111:0101 1110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0010:0000 1111:0101 1110: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MAXPD—Return Maximum Packed Double-Precision Floating-Point Values</strong></td>
<td>0110 0110:0000 1111:0101 1111:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 1111: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MAXSD—Return Maximum Scalar Double-Precision Floating-Point Value</strong></td>
<td>1111 0010:0000 1111:0101 1111:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0010:0000 1111:0101 1111: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MINPD—Return Minimum Packed Double-Precision Floating-Point Values</strong></td>
<td>0110 0110:0000 1111:0101 1101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 1101: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MINSD—Return Minimum Scalar Double-Precision Floating-Point Value</strong></td>
<td>1111 0010:0000 1111:0101 1101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0010:0000 1111:0101 1101: mod xmmreg r/m</td>
</tr>
</tbody>
</table>
**Table B-26. Formats and Encodings of SSE2 Floating-Point Instructions (Contd.)**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MOVAPD—Move Aligned Packed Double-Precision Floating-Point Values</strong></td>
<td>0110 0110:0000 1111:0010 1001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>xmmreg1 to xmmreg2</td>
<td>0110 0110:0000 1111:0010 1001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>xmmreg1 to mem</td>
<td>0110 0110:0000 1111:0010 1001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0010 1001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>mem to xmmreg1</td>
<td>0110 0110:0000 1111:0010 1001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td><strong>MOVHPD—Move High Packed Double-Precision Floating-Point Values</strong></td>
<td>0110 0110:0000 1111:0001 0111:1 mod xmmreg r/m</td>
</tr>
<tr>
<td>xmmreg to mem</td>
<td>0110 0110:0000 1111:0001 0111:1 mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0001 0111:1 mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MOVLPD—Move Low Packed Double-Precision Floating-Point Values</strong></td>
<td>0110 0110:0000 1111:0001 0011:1 mod xmmreg r/m</td>
</tr>
<tr>
<td>xmmreg to mem</td>
<td>0110 0110:0000 1111:0001 0011:1 mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0001 0011:1 mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MOVMSKPD—Extract Packed Double-Precision Floating-Point Sign Mask</strong></td>
<td>0110 0110:0000 1111:0101 0000:11 r32 xmmreg</td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>0110 0110:0000 1111:0101 0000:11 r32 xmmreg</td>
</tr>
<tr>
<td><strong>MOVSD—Move Scalar Double-Precision Floating-Point Values</strong></td>
<td>1111 0010:0000 1111:0001 0001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>xmmreg1 to xmmreg2</td>
<td>1111 0010:0000 1111:0001 0001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>xmmreg1 to mem</td>
<td>1111 0010:0000 1111:0001 0001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0010:0000 1111:0001 0001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td>mem to xmmreg1</td>
<td>1111 0010:0000 1111:0001 0001:11 xmmreg2 xmmreg1</td>
</tr>
<tr>
<td><strong>MOVUPD—Move Unaligned Packed Double-Precision Floating-Point Values</strong></td>
<td>0110 0110:0000 1111:0001 0011:1 mod xmmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0001 0011:1 mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg1</td>
<td>0110 0110:0000 1111:0001 0011:1 mod xmmreg r/m</td>
</tr>
</tbody>
</table>
### INSTRUCTION FORMATS AND ENCODINGS

**Table B-26. Formats and Encodings of SSE2 Floating-Point Instructions (Contd.)**

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>xmmreg1 to xmmreg2</code></td>
<td>0110 0110:0000 1111:0001 0000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td><code>xmmreg1 to mem</code></td>
<td>0110 0110:0000 1111:0001 0000: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MULPD—Multiply Packed Double-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2 to xmmreg1</code></td>
<td>0110 0110:0000 1111:0101 1001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td><code>mem to xmmreg</code></td>
<td>0110 0110:0000 1111:0101 1001: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>MULSD—Multiply Scalar Double-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2 to xmmreg1</code></td>
<td>1111 0010:00001111:01011001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td><code>mem to xmmreg</code></td>
<td>1111 0010:00001111:01011001: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>ORPD—Bitwise Logical OR of Double-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2 to xmmreg1</code></td>
<td>0110 0110:0000 1111:0101 0110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td><code>mem to xmmreg</code></td>
<td>0110 0110:0000 1111:0101 0110: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>SHUFPD—Shuffle Packed Double-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2 to xmmreg1, imm8</code></td>
<td>0110 0110:0000 1111:1100 0110:11 xmmreg1 xmmreg2 imm8</td>
</tr>
<tr>
<td><code>mem to xmmreg, imm8</code></td>
<td>0110 0110:0000 1111:1100 0110: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>SQRTPD—Compute Square Roots of Packed Double-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2 to xmmreg1</code></td>
<td>0110 0110:0000 1111:0101 0001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td><code>mem to xmmreg</code></td>
<td>0110 0110:0000 1111:0101 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>SQRTSD—Compute Square Root of Scalar Double-Precision Floating-Point Value</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2 to xmmreg1</code></td>
<td>1111 0010:0000 1111:0101 0001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0010:0000 1111:0101 10001: mod xmmreg r/m</td>
</tr>
<tr>
<td>SUBPD—Subtract Packed Double-Precision Floating-Point Values</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0101 1100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td>SUBSD—Subtract Scalar Double-Precision Floating-Point Values</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>1111 0010:0000 1111:0101 1100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>1111 0010:0000 1111:0101 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td>UCOMISD—Unordered Compare Scalar Ordered Double-Precision Floating-Point Values and Set EFLAGS</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0010 1110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0010 1110: mod xmmreg r/m</td>
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<tr>
<td>UNPCKHPD—Unpack and Interleave High Packed Double-Precision Floating-Point Values</td>
<td></td>
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<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0001 0100:11 xmmreg1 xmmreg2</td>
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<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0001 0100: mod xmmreg r/m</td>
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<tr>
<td>UNPCKLPD—Unpack and Interleave Low Packed Double-Precision Floating-Point Values</td>
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<td>xmmreg2 to xmmreg1</td>
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<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0000 1000: mod xmmreg r/m</td>
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<td>XORPD—Bitwise Logical OR of Double-Precision Floating-Point Values</td>
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<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0101 1011:11 xmmreg1 xmmreg2</td>
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### Table B-26. Formats and Encodings of SSE2 Floating-Point Instructions (Contd.)

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<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0101 0111: mod xmmreg r/m</td>
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### Table B-27. Formats and Encodings of SSE2 Integer Instructions

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<td><strong>MOVD—Move Doubleword</strong></td>
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<td>reg to xmmreg</td>
<td>0110 0110:0000 1111:0110 1110: 11 xmmreg reg</td>
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<tr>
<td>reg from xmmreg</td>
<td>0110 0110:0100 1111:0111 1110: 11 xmmreg reg</td>
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<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0110 1110: mod xmmreg r/m</td>
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<tr>
<td>mem from xmmreg</td>
<td>0110 0110:0000 1111:0111 1110: mod xmmreg r/m</td>
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<tr>
<td><strong>MOVDQA—Move Aligned Double Quadword</strong></td>
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<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0110 1111:11 xmmreg1 xmmreg2</td>
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<tr>
<td>xmmreg2 from xmmreg1</td>
<td>0110 0110:0000 1111:0111 1111:11 xmmreg1 xmmreg2</td>
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<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0110 1111: mod xmmreg r/m</td>
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<tr>
<td>mem from xmmreg</td>
<td>0110 0110:0000 1111:0111 1111: mod xmmreg r/m</td>
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<tr>
<td><strong>MOVDQU—Move Unaligned Double Quadword</strong></td>
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<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0110 1111:11 xmmreg1 xmmreg2</td>
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<tr>
<td>xmmreg2 from xmmreg1</td>
<td>1111 0011:0000 1111:0111 1111:11 xmmreg1 xmmreg2</td>
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<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0110 1111: mod xmmreg r/m</td>
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<tr>
<td>mem from xmmreg</td>
<td>1111 0011:0000 1111:0111 1111: mod xmmreg r/m</td>
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<tr>
<td><strong>MOVQ2DQ—Move Quadword from MMX to XMM Register</strong></td>
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<tr>
<td>mmreg to xmmreg</td>
<td>1111 0011:0000 1111:0000 0110:11 mmreg1 mmreg2</td>
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<tr>
<td><strong>MOVQ2Q—Move Quadword from XMM to MMX Register</strong></td>
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<tr>
<td>xmmreg to mmreg</td>
<td>1111 0010:0000 1111:1001 0110:11 mmreg1 mmreg2</td>
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<tr>
<td><strong>MOVQ—Move Quadword</strong></td>
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<td>xmmreg2 to xmmreg1</td>
<td>1111 0011:0000 1111:0111 1110: 11 xmmreg1 xmmreg2</td>
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<tr>
<td>xmmreg2 from xmmreg1</td>
<td>0110 0110:0000 1111:1001 0110: 11 xmmreg1 xmmreg2</td>
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<tr>
<td>mem to xmmreg</td>
<td>1111 0011:0000 1111:0111 1110: mod xmmreg r/m</td>
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### Table B-27. Formats and Encodings of SSE2 Integer Instructions (Contd.)

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<td>mem from xmmreg</td>
<td>0110 0110:0000 1111:1101 0110: mod xmmreg r/m</td>
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<tr>
<td><strong>PACKSSDW</strong>—Pack Dword To Word Data (signed with saturation)</td>
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<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0110 1011:11 xmmreg1 xmmreg2</td>
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<tr>
<td>memory to xmmreg</td>
<td>0110 0110:0000 1111:0110 1011: mod xmmreg r/m</td>
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<tr>
<td><strong>PACKSSWB</strong>—Pack Word To Byte Data (signed with saturation)</td>
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<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0110 0111:11 xmmreg1 xmmreg2</td>
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<tr>
<td>memory to xmmreg</td>
<td>0110 0110:0000 1111:0110 0111: mod xmmreg r/m</td>
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<tr>
<td><strong>PACKUSWB</strong>—Pack Word To Byte Data (unsigned with saturation)</td>
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<td>memory to xmmreg</td>
<td>0110 0110:0000 1111:0110 0111: mod xmmreg r/m</td>
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<tr>
<td><strong>PADDQ</strong>—Add Packed Quadword Integers</td>
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<td>0000 1111:1101 0100: mod mmreg r/m</td>
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<td>xmmreg2 to xmmreg1</td>
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<td>0110 0110:0000 1111:1101 0100: mod xmmreg r/m</td>
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<tr>
<td><strong>PADD</strong>—Add With Wrap-around</td>
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<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:1111 11gg:11 xmmreg1 xmmreg2</td>
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<tr>
<td>memory to xmmreg</td>
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<tr>
<td><strong>PADDSS</strong>—Add Signed With Saturation</td>
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<td><strong>PADDUS</strong>—Add Unsigned With Saturation</td>
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<td>PAND—Bitwise And</td>
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<td>xmmreg2</td>
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<td>PANDN—Bitwise AndNot</td>
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<td>memory to xmmreg</td>
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<td>PAVGB—Average Packed Integers</td>
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<td>xmmreg2</td>
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<tr>
<td>mem to xmmreg</td>
<td>01100110:0001111:1110000 mod xmmreg r/m</td>
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<td>PAVGW—Average Packed Integers</td>
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<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:1110 0011 mod xmmreg r/m</td>
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<td>PCMEQ—Packed Compare For Equality</td>
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<td>xmmreg1 with xmmreg2</td>
<td>0110 0110:0000 1111:0111 01gg: 11 xmmreg1</td>
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<tr>
<td></td>
<td>xmmreg2</td>
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<tr>
<td>xmmreg with memory</td>
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<td>PCMPGT—Packed Compare Greater (signed)</td>
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<td>xmmreg2</td>
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<tr>
<td>xmmreg with memory</td>
<td>0110 0110:0000 1111:0110 01gg: mod xmmreg r/m</td>
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<tr>
<td>PEXTRW—Extract Word</td>
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<td>xmmreg to reg32, imm8</td>
<td>0110 0110:0000 1111:1100 0101:11 r32 xmmreg:</td>
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<td>imm8</td>
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<tr>
<td>PINSRW—Insert Word</td>
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<td>reg32 to xmmreg, imm8</td>
<td>0110 0110:0000 1111:1100 0100:11 xmmreg r32:</td>
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<td>imm8</td>
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### INSTRUCTION FORMATS AND ENCODINGS

#### Table B-27. Formats and Encodings of SSE2 Integer Instructions (Contd.)

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<td>m16 to xmmreg, imm8</td>
<td>0110 0110:0000 1111:1100 0100: mod xmmreg r/m: imm8</td>
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<tr>
<td><strong>PMADDWD</strong>—Packed Multiply Add</td>
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<tr>
<td>memory to xmmreg</td>
<td>0110 0110:0000 1111:1111 0101: mod xmmreg r/m</td>
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<tr>
<td><strong>PMAXSW</strong>—Maximum of Packed Signed Word Integers</td>
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<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:1110 1110:11 1110: mod xmmreg r/m</td>
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<tr>
<td><strong>PMAXUB</strong>—Maximum of Packed Unsigned Byte Integers</td>
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<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:1101 1110:11 1110: mod xmmreg r/m</td>
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<td><strong>PMINSW</strong>—Minimum of Packed Signed Word Integers</td>
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<td>xmmreg2 to xmmreg1</td>
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<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:1110 1010:11 1110: mod xmmreg r/m</td>
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<tr>
<td><strong>PMINUB</strong>—Minimum of Packed Unsigned Byte Integers</td>
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<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:1101 1010:11 1110: mod xmmreg r/m</td>
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<tr>
<td><strong>PMOVMSKB</strong>—Move Byte Mask To Integer</td>
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<td>xmmreg to reg32</td>
<td>0110 0110:0000 1111:1101 0111:11 r32 xmmreg</td>
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<tr>
<td><strong>PMULHUW</strong>—Packed multiplication, store high word (unsigned)</td>
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<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:1110 0100: 11 xmmreg1 xmmreg2</td>
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<tr>
<td>memory to xmmreg</td>
<td>0110 0110:0000 1111:1110 0100: mod xmmreg r/m</td>
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### Table B-27. Formats and Encodings of SSE2 Integer Instructions (Contd.)

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<tr>
<td>memory to xmmreg</td>
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<tr>
<td><strong>PMULLW—Packed Multiplication, store low word</strong></td>
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<td>memory to xmmreg</td>
<td>0110 0110:0000 1111:1111 0101: mod xmmreg r/m</td>
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<td><strong>PMULUDQ—Multiply Packed Unsigned Doubleword Integers</strong></td>
<td>0000 1111:1111 0100:11 mmreg1 mmreg2</td>
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<td>mem to mmreg</td>
<td>0000 1111:1111 0100: mod mmreg r/m</td>
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<td>mem to xmmreg</td>
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<tr>
<td><strong>POR—Bitwise Or</strong></td>
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<td>memory to xmmreg</td>
<td>0110 0110:0000 1111:1111 1011: mod xmmreg r/m</td>
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<tr>
<td><strong>PSADBW—Compute Sum of Absolute Differences</strong></td>
<td>0110 0110:0000 1111:1111 0100:11 xmmreg1 xmmreg2</td>
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<td>xmmreg2 to xmmreg1</td>
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<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:1111 0100: mod xmmreg r/m</td>
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<tr>
<td><strong>PSHUFLW—Shuffle Packed Low Words</strong></td>
<td>1111 0010:0000 1111:0111 0000:11 xmmreg1 xmmreg2: imm8</td>
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<td>xmmreg2 to xmmreg1, imm8</td>
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<tr>
<td>mem to xmmreg, imm8</td>
<td>1111 0010:0000 1111:0111 0000:11 mod xmmreg r/m: imm8</td>
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<td>xmmreg2: imm8</td>
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<tr>
<td>mem to xmmreg, imm8</td>
<td>1111 0011:0000 1111:0111 0000: mod xmmreg r/m:</td>
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<td>imm8</td>
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<tr>
<td><strong>PSHUFD—Shuffle Packed Doublewords</strong></td>
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<td>xmmreg2: imm8</td>
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<tr>
<td>mem to xmmreg, imm8</td>
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<tr>
<td><strong>PSLLDQ—Shift Double Quadword Left Logical</strong></td>
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<td><strong>PSLL—Packed Shift Left Logical</strong></td>
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<td>xmmreg1 by xmmreg2</td>
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<td><strong>PSRA—Packed Shift Right Arithmetic</strong></td>
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<td><strong>PSRLDQ—Shift Double Quadword Right Logical</strong></td>
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</tr>
<tr>
<td><strong>PSUBQ—Subtract Packed Quadword Integers</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:1111 011:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:1111 1011: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:1111 1011:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:1111 1011: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PSUB—Subtract With Wrap-around</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 from xmmreg1</td>
<td>0110 0110:0000 1111:1110 10gg: 11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>memory from xmmreg</td>
<td>0110 0110:0000 1111:1111 10gg: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PSUBS—Subtract Signed With Saturation</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 from xmmreg1</td>
<td>0110 0110:0000 1111:1110 10gg: 11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>memory from xmmreg</td>
<td>0110 0110:0000 1111:1110 10gg: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PSUBUS—Subtract Unsigned With Saturation</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 from xmmreg1</td>
<td>0000 1111:1101 10gg: 11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>memory from xmmreg</td>
<td>0000 1111:1101 10gg: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PUNPCKH—Unpack High Data To Next Larger Type</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0110 10gg: 11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0110 10gg: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PUNPCKHQDQ—Unpack High Data</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0110 1101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0110 1101: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PUNPCKL—Unpack Low Data To Next Larger Type</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0110 00gg: 11 xmmreg1 xmmreg2</td>
</tr>
</tbody>
</table>
### Table B-27. Formats and Encodings of SSE2 Integer Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0110 00gg: mod xmmreg r/m</td>
</tr>
<tr>
<td>PUNPCKLQDQ—Unpack Low Data</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0110 1100:11 xmmreg1</td>
</tr>
<tr>
<td></td>
<td>xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0110 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td>PXOR—Bitwise Xor</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:1110 1111: 11 xmmreg1</td>
</tr>
<tr>
<td></td>
<td>xmmreg2</td>
</tr>
<tr>
<td>memory to xmmreg</td>
<td>0110 0110:0000 1111:1110 1111: mod xmmreg r/m</td>
</tr>
</tbody>
</table>

### Table B-28. Format and Encoding of SSE2 Cacheability Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>MASKMOVDQU—Store Selected Bytes of Double Quadword</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:1111 0111:11 xmmreg1</td>
</tr>
<tr>
<td></td>
<td>xmmreg2</td>
</tr>
<tr>
<td>CLFLUSH—Flush Cache Line</td>
<td></td>
</tr>
<tr>
<td>mem</td>
<td>0000 1111:1010 1110: mod 111 r/m</td>
</tr>
<tr>
<td>MOVNTPD—Store Packed Double-Precision Floating-Point Values Using Non-Temporal Hint</td>
<td></td>
</tr>
<tr>
<td>xmmreg to mem</td>
<td>0110 0110:0000 1111:0010 1011: mod xmmreg r/m</td>
</tr>
<tr>
<td>MOVNTDQ—Store Double Quadword Using Non-Temporal Hint</td>
<td></td>
</tr>
<tr>
<td>xmmreg to mem</td>
<td>0110 0110:0000 1111:1110 0111: mod xmmreg r/m</td>
</tr>
<tr>
<td>MOVNTI—Store Doubleword Using Non-Temporal Hint</td>
<td></td>
</tr>
<tr>
<td>reg to mem</td>
<td>0000 1111:1100 0011: mod reg r/m</td>
</tr>
<tr>
<td>PAUSE—Spin Loop Hint</td>
<td>1111 0011:1001 0000</td>
</tr>
<tr>
<td>LFENCE—Load Fence</td>
<td>0000 1111:1010 1110: 11 101 000</td>
</tr>
<tr>
<td>MFENCE—Memory Fence</td>
<td>0000 1111:1010 1110: 11 110 000</td>
</tr>
</tbody>
</table>
### B.10 SSE3 FORMATS AND ENCODINGS TABLE

The tables in this section provide SSE3 formats and encodings. Some SSE3 instructions require a mandatory prefix (66H, F2H, F3H) as part of the two-byte opcode. These prefixes are included in the tables.

When in IA-32e mode, use of the REX.R prefix permits instructions that use general purpose and XMM registers to access additional registers. Some instructions require the REX.W prefix to promote the instruction to 64-bit operation. Instructions that require the REX.W prefix are listed (with their opcodes) in Section B.13.

#### Table B-29. Formats and Encodings of SSE3 Floating-Point Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDSUBPD—Add /Sub packed DP FP numbers from XMM2/Mem to XMM1</td>
<td>01100110:00001111:11010000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>01100110:00001111:11010000: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td></td>
</tr>
<tr>
<td>ADDSUBPS—Add /Sub packed SP FP numbers from XMM2/Mem to XMM1</td>
<td>11110010:00001111:11010000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>11110010:00001111:11010000: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td></td>
</tr>
<tr>
<td>HADDPD—Add horizontally packed DP FP numbers XMM2/Mem to XMM1</td>
<td>01100110:00001111:01111100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>01100110:00001111:01111100: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td></td>
</tr>
<tr>
<td>HADDPD—Add horizontally packed SP FP numbers XMM2/Mem to XMM1</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td></td>
</tr>
<tr>
<td>HSUBPD—Sub horizontally packed DP FP numbers XMM2/Mem to XMM1</td>
<td>01100110:00001111:01111101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>01100110:00001111:01111101: mod xmmreg r/m</td>
</tr>
</tbody>
</table>
## Table B-29. Formats and Encodings of SSE3 Floating-Point Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td>01100110:00001111:011111101: mod xmmreg r/m</td>
</tr>
<tr>
<td>HSUBPS—Sub horizontally packed SP FP numbers XMM2/Mem to XMM1</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>11110010:00001111:01111101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>11110010:00001111:01111101: mod xmmreg r/m</td>
</tr>
</tbody>
</table>

## Table B-30. Formats and Encodings for SSE3 Event Management Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>MONITOR—Set up a linear address range to be monitored by hardware</td>
<td></td>
</tr>
<tr>
<td>eax, ecx, edx</td>
<td>0000 1111:0000 0001:11 001 000</td>
</tr>
<tr>
<td>MWAIT—Wait until write-back store performed within the range specified by the instruction MONITOR</td>
<td></td>
</tr>
<tr>
<td>eax, ecx</td>
<td>0000 1111:0000 0001:11 001 001</td>
</tr>
</tbody>
</table>

## Table B-31. Formats and Encodings for SSE3 Integer and Move Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>FISTTP—Store ST in int16 (chop) and pop</td>
<td></td>
</tr>
<tr>
<td>m16int</td>
<td>11011 111 : modA 001 r/m</td>
</tr>
<tr>
<td>FISTTP—Store ST in int32 (chop) and pop</td>
<td></td>
</tr>
<tr>
<td>m32int</td>
<td>11011 011 : modA 001 r/m</td>
</tr>
<tr>
<td>FISTTP—Store ST in int64 (chop) and pop</td>
<td></td>
</tr>
<tr>
<td>m64int</td>
<td>11011 101 : modA 001 r/m</td>
</tr>
<tr>
<td>LDDQU—Load unaligned integer 128-bit</td>
<td></td>
</tr>
<tr>
<td>xmm, m128</td>
<td>11110010:00001111:11110000: modA xmmreg r/m</td>
</tr>
<tr>
<td>MOVDDUP—Move 64 bits representing one DP data from XMM2/Mem to XMM1 and duplicate</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>11110010:00001111:00010101:11 xmmreg1 xmmreg2</td>
</tr>
</tbody>
</table>
B.11 SSSE3 FORMATS AND ENCODING TABLE

The tables in this section provide SSSE3 formats and encodings. Some SSSE3 instructions require a mandatory prefix (66H) as part of the three-byte opcode. These prefixes are included in the table below.

Table B-32. Formats and Encodings for SSSE3 Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>PABSB—Packed Absolute Value Bytes</td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000: 0001 1100:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000: 0001 1100: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000: 0001 1100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0001 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td>PABSD—Packed Absolute Value Double Words</td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000: 0001 1110:11 mmreg1 mmreg2</td>
</tr>
</tbody>
</table>
### Table B-32. Formats and Encodings for SSSE3 Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000: 0001 1110: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000: 0001 1110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0001 1110: mod xmmreg r/m</td>
</tr>
</tbody>
</table>

**PABSw—Packed Absolute Value Words**

| mmreg2 to mmreg1       | 0000 1111:0011 1000: 0001 1101:11 mmreg1 mmreg2 |
| mem to mmreg           | 0000 1111:0011 1000: 0001 1101: mod mmreg r/m |
| xmmreg2 to xmmreg1, imm8 | 0110 0110:0000 1111:0011 1000: 0001 1101:11 xmmreg1 xmmreg2: imm8 |
| mem to xmmreg, imm8    | 0110 0110:0000 1111:0011 1000: 0001 1101:11 mod xmmreg r/m: imm8 |

**PALIGNR—Packed Align Right**

| mmreg2 to mmreg1, imm8 | 0000 1111:0011 1000: 0000 0011:11 mmreg1 mmreg2: imm8 |
| mem to mmreg, imm8     | 0000 1111:0011 1000: 0000 0011: mod mmreg r/m: imm8 |
| xmmreg2 to xmmreg1, imm8 | 0110 0110:0000 1111:0011 1000: 0000 0011:11 xmmreg1 xmmreg2: imm8 |
| mem to xmmreg, imm8    | 0110 0110:0000 1111:0011 1000: 0000 0011:11 mod xmmreg r/m: imm8 |

**PHADDD—Packed Horizontal Add Double Words**

| mmreg2 to mmreg1       | 0000 1111:0011 1000: 0000 0010:11 mmreg1 mmreg2 |
| mem to mmreg           | 0000 1111:0011 1000: 0000 0010: mod mmreg r/m |
| xmmreg2 to xmmreg1     | 0110 0110:0000 1111:0011 1000: 0000 0010:11 xmmreg1 xmmreg2 |
| mem to xmmreg          | 0110 0110:0000 1111:0011 1000: 0000 0010: mod xmmreg r/m |

**PHADDSw—Packed Horizontal Add and Saturate**

| mmreg2 to mmreg1       | 0000 1111:0011 1000: 0000 0011:11 mmreg1 mmreg2 |
| mem to mmreg           | 0000 1111:0011 1000: 0000 0011: mod mmreg r/m |
| xmmreg2 to xmmreg1     | 0110 0110:0000 1111:0011 1000: 0000 0011:11 xmmreg1 xmmreg2 |
### Table B-32. Formats and Encodings for SSSE3 Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0011: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PHADDw—Packed Horizontal Add Words</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000: 0000 0011:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000: 0000 0001: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0001:11 mmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PHSUBD—Packed Horizontal Subtract Double Words</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000: 0000 0110:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000: 0000 0110: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0110:11 mmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0110: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PHSUBBSw—Packed Horizontal Subtract and Saturate</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000: 0000 0111:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000: 0000 0111: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0111:11 mmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0111: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PHSUBW—Packed Horizontal Subtract Words</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000: 0000 0101:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000: 0000 0101: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0101:11 mmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0000 0101: mod xmmreg r/m</td>
</tr>
</tbody>
</table>
### Table B-32. Formats and Encodings for SSSE3 Instructions (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PMADDUBSw—Multiply and Add Packed Signed and Unsigned Bytes</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000:0000 0100:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000:0000 0100:10: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0000 0100:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0000 0100:10: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PMULHRSw—Packed Multiply High with Round and Scale</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000:0000 1011:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000:0000 1011:10: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0000 1011:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0000 1011:10: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PSHUFB—Packed Shuffle Bytes</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000:0000 0000:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000:0000 0000:00: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0000 0000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0000 0000:00: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PSIGNB—Packed Sign Bytes</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000:0000 1000:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000:0000 1000:10: mod mmreg r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0000 1000:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0000 1000:10: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PSIGND—Packed Sign Double Words</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg2 to mmreg1</td>
<td>0000 1111:0011 1000:0000 1010:11 mmreg1 mmreg2</td>
</tr>
<tr>
<td>mem to mmreg</td>
<td>0000 1111:0011 1000:0000 1010:10: mod mmreg r/m</td>
</tr>
</tbody>
</table>
B.12 AESNI AND PCLMULQDQ INSTRUCTION FORMATS AND ENCODINGS

Table B-33 shows the formats and encodings for AESNI and PCLMULQDQ instructions.

Table B-33. Formats and Encodings of AESNI and PCLMULQDQ Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>AESDEC—Perform One Round of an AES Decryption Flow</td>
<td>0110 0110:0000 1111:0011 1000:1101 1110:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:1100:11 mod xmmreg r/m</td>
</tr>
<tr>
<td>AESDECLAST—Perform Last Round of an AES Decryption Flow</td>
<td>0110 0110:0000 1111:0011 1000:1101 1111:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:1101:11 mod xmmreg r/m</td>
</tr>
<tr>
<td>AESENCE—Perform One Round of an AES Encryption Flow</td>
<td>0110 0110:0000 1111:0011 1000:1101 1100:11 xmmreg1 xmmreg2</td>
</tr>
</tbody>
</table>
INSTRUCTION FORMATS AND ENCODINGS

Table B-33. Formats and Encodings of AESNI and PCLMULQDQ Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:1101 1100: mod xmmreg r/m</td>
</tr>
<tr>
<td>AESENCLAST—Perform Last Round of an AES Encryption Flow</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:1101 1101:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:1101 1101:1101: mod xmmreg r/m</td>
</tr>
<tr>
<td>AESIMC—Perform the AES InvMixColumn Transformation</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:1101 1011:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:1101 1011: mod xmmreg r/m</td>
</tr>
<tr>
<td>AESKEYGENASSIST—AES Round Key Generation Assist</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0110 0110:0000 1111:0011 1001:1101 1111:11 xmmreg1 xmmreg2: imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1001:1101 1111: mod xmmreg r/m; imm8</td>
</tr>
<tr>
<td>PCLMULQDQ—Carry-Less Multiplication Quadword</td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0110 0110:0000 1111:0011 1000:0100 0100:11 xmmreg1 xmmreg2: imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1000:0100 0100: mod xmmreg r/m; imm8</td>
</tr>
</tbody>
</table>

B.13 SPECIAL ENCODINGS FOR 64-BIT MODE

The following Pentium, P6, MMX, SSE, SSE2, SSE3 instructions are promoted to 64-bit operation in IA-32e mode by using REX.W. However, these entries are special cases that do not follow the general rules (specified in Section B.4).
### Table B-34. Special Case Instructions Promoted Using REX.W

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CMOVcc—Conditional Move</strong></td>
<td></td>
</tr>
<tr>
<td>register2 to register1</td>
<td>0100 0R0B 0000 1111:0100 tttn : 11 reg1</td>
</tr>
<tr>
<td></td>
<td>reg2</td>
</tr>
<tr>
<td>qwordregister2 to qwordregister1</td>
<td>0100 1R0B 0000 1111:0100 tttn : 11</td>
</tr>
<tr>
<td></td>
<td>qwordreg1 qwordreg2</td>
</tr>
<tr>
<td>memory to register</td>
<td>0100 0RXB 0000 1111 : 0100 tttn : mod reg</td>
</tr>
<tr>
<td></td>
<td>r/m</td>
</tr>
<tr>
<td>memory64 to qwordregister</td>
<td>0100 1RXB 0000 1111 : 0100 tttn : mod qwordreg r/m</td>
</tr>
<tr>
<td><strong>CVTSD2SI—Convert Scalar Double-Precision Floating-Point Value to Doubleword Integer</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>0100 0R0B 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101:11 r32 xmmreg</td>
</tr>
<tr>
<td>xmmreg to r64</td>
<td>0100 1R0B 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101:11 r64 xmmreg</td>
</tr>
<tr>
<td>mem64 to r32</td>
<td>0100 0RXB 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101:mod r32 r/m</td>
</tr>
<tr>
<td>mem64 to r64</td>
<td>0100 1RXB 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101:mod r64 r/m</td>
</tr>
<tr>
<td><strong>CVTSI2SS—Convert Doubleword Integer to Scalar Single-Precision Floating-Point Value</strong></td>
<td></td>
</tr>
<tr>
<td>r32 to xmmreg1</td>
<td>0100 0R0B 1111 0011:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1010:11 xmmreg r32</td>
</tr>
<tr>
<td>r64 to xmmreg1</td>
<td>0100 1R0B 1111 0011:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1010:11 xmmreg r64</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0100 0RXB 1111 0011:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1010:mod xmmreg r/m</td>
</tr>
<tr>
<td>mem64 to xmmreg</td>
<td>0100 1RXB 1111 0011:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1010:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>CVTSI2SD—Convert Doubleword Integer to Scalar Double-Precision Floating-Point Value</strong></td>
<td></td>
</tr>
<tr>
<td>r32 to xmmreg1</td>
<td>0100 0R0B 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1010:11 xmmreg r32</td>
</tr>
<tr>
<td>r64 to xmmreg1</td>
<td>0100 1R0B 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1010:11 xmmreg r64</td>
</tr>
</tbody>
</table>
### Table B-34. Special Case Instructions Promoted Using REX.W (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td>0100 0RXB 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>010: mod xmmreg r/m</td>
</tr>
<tr>
<td>mem64 to xmmreg</td>
<td>0100 1RXB 1111 0010:0000</td>
</tr>
<tr>
<td></td>
<td>1111:0010 1010: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>CVTSS2SI—Convert Scalar Single-Precision Floating-Point Value to Doubleword Integer</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>0100 0R0B 1111 0011:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101:11 r32 xmmreg</td>
</tr>
<tr>
<td>xmmreg to r64</td>
<td>0100 1R0B 1111 0011:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101:11 r64 xmmreg</td>
</tr>
<tr>
<td>mem to r32</td>
<td>0100 0RXB 11110011:00001111:00101101:</td>
</tr>
<tr>
<td></td>
<td>mod r32 r/m</td>
</tr>
<tr>
<td>mem32 to r64</td>
<td>0100 1RXB 1111 0011:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101: mod r64 r/m</td>
</tr>
<tr>
<td><strong>CVTTS2SI—Convert with Truncation Scalar Single-Precision Floating-Point Value to Doubleword Integer</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>0100 0R0B 11110010:00001111:0011:0010</td>
</tr>
<tr>
<td></td>
<td>1100:11 r32 xmmreg</td>
</tr>
<tr>
<td>xmmreg to r64</td>
<td>0100 1R0B 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101: mod r32 r/m</td>
</tr>
<tr>
<td>mem64 to r32</td>
<td>0100 0RXB 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101: mod r64 r/m</td>
</tr>
<tr>
<td><strong>CVTTSD2SI—Convert with Truncation Scalar Double-Precision Floating-Point Value to Doubleword Integer</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>0100 0R0B 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1101:11 r32 xmmreg</td>
</tr>
<tr>
<td>xmmreg to r64</td>
<td>0100 1R0B 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1100:11 r64 xmmreg</td>
</tr>
<tr>
<td>mem64 to r32</td>
<td>0100 0RXB 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1100: mod r32 r/m</td>
</tr>
<tr>
<td>mem64 to r64</td>
<td>0100 1RXB 1111 0010:0000 1111:0010</td>
</tr>
<tr>
<td></td>
<td>1100: mod r64 r/m</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>mem32 to r64</td>
<td>0100 1RXB 1111 0011:0000 1111:0010 1100: mod r64 r/m</td>
</tr>
<tr>
<td><strong>MOVD/MOVQ—Move doubleword</strong></td>
<td></td>
</tr>
<tr>
<td>reg to mmxreg</td>
<td>0100 0R0B 0000 1111:0110 1110:11 mmxreg reg</td>
</tr>
<tr>
<td>qwordreg to mmxreg</td>
<td>0100 1R0B 0000 1111:0110 1110:11 mmxreg qwordreg</td>
</tr>
<tr>
<td>reg from mmxreg</td>
<td>0100 0R0B 0000 1111:0111 1110:11 mmxreg reg</td>
</tr>
<tr>
<td>qwordreg from mmxreg</td>
<td>0100 1R0B 0000 1111:0111 1110:11 mmxreg qwordreg</td>
</tr>
<tr>
<td>mem to mmxreg</td>
<td>0100 ORXB 0000 1111:0110 1110: mod mmxreg r/m</td>
</tr>
<tr>
<td>mem64 to mmxreg</td>
<td>0100 1RXB 0000 1111:0110 1110: mod mmxreg r/m</td>
</tr>
<tr>
<td>mem from mmxreg</td>
<td>0100 ORXB 0000 1111:0111 1110: mod mmxreg r/m</td>
</tr>
<tr>
<td>mem64 from mmxreg</td>
<td>0100 1RXB 0000 1111:0111 1110: mod mmxreg r/m</td>
</tr>
<tr>
<td>mmxreg with memory</td>
<td>0100 ORXB 0000 1111:0110 01gg: mod mmxreg r/m</td>
</tr>
<tr>
<td><strong>MOVMSKPS—Extract Packed Single-Precision Floating-Point Sign Mask</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg to r32</td>
<td>0100 0R0B 0000 1111:0101 0000:11 r32 xmmreg</td>
</tr>
<tr>
<td>xmmreg to r64</td>
<td>0100 1R0B 00001111:01010000:11 r64 xmmreg</td>
</tr>
<tr>
<td><strong>PEXTRw—Extract Word</strong></td>
<td></td>
</tr>
<tr>
<td>mmreg to reg32, imm8</td>
<td>0100 0R0B 0000 1111:1100 0101:11 r32 mmreg: imm8</td>
</tr>
<tr>
<td>mmreg to reg64, imm8</td>
<td>0100 1R0B 0000 1111:1100 0101:11 r64 mmreg: imm8</td>
</tr>
<tr>
<td>xmmreg to reg32, imm8</td>
<td>0100 0R0B 0110 0110 0000 1111:1100 0101:11 r32 xmmreg: imm8</td>
</tr>
<tr>
<td>xmmreg to reg64, imm8</td>
<td>0100 1R0B 0110 0110 0000 1111:1100 0101:11 r64 xmmreg: imm8</td>
</tr>
</tbody>
</table>
### Table B-34. Special Case Instructions Promoted Using REX.W (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>PINSRW—Insert Word</td>
<td></td>
</tr>
<tr>
<td>reg32 to mmreg, imm8</td>
<td>0100 0ROB 0000 1111:1100 0100:11 mmreg r32: imm8</td>
</tr>
<tr>
<td>reg64 to mmreg, imm8</td>
<td>0100 1ROB 0000 1111:1100 0100:11 mmreg r64: imm8</td>
</tr>
<tr>
<td>m16 to mmreg, imm8</td>
<td>0100 0ROB 0000 1111:1100 0100 mod mmreg r/m: imm8</td>
</tr>
<tr>
<td>m16 to mmreg, imm8</td>
<td>0100 1RXB 0000 1111:11000100 mod mmreg r/m: imm8</td>
</tr>
<tr>
<td>reg32 to xmmreg, imm8</td>
<td>0100 0RXB 0110 0110 0000 1111:1100 0100:11 xmmreg r32: imm8</td>
</tr>
<tr>
<td>reg64 to xmmreg, imm8</td>
<td>0100 0RXB 0110 0110 0000 1111:1100 0100:11 xmmreg r64: imm8</td>
</tr>
<tr>
<td>m16 to xmmreg, imm8</td>
<td>0100 0RXB 0110 0110 0000 1111:1100 0100 mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td>m16 to xmmreg, imm8</td>
<td>0100 1RXB 0110 0110 0000 1111:1100 0100 mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td>PMOVMSKB—Move Byte Mask To Integer</td>
<td></td>
</tr>
<tr>
<td>mmreg to reg32</td>
<td>0100 0RXB 0000 1111:1101 0111:11 r32 mmreg</td>
</tr>
<tr>
<td>mmreg to reg64</td>
<td>0100 1ROB 0000 1111:1101 0111:11 r64 mmreg</td>
</tr>
<tr>
<td>xmmreg to reg32</td>
<td>0100 0RXB 0110 0110 0000 1111:1101 0111:11 r32 xmmreg</td>
</tr>
<tr>
<td>xmmreg to reg64</td>
<td>0110 0110 0000 1111:1101 0111:11 r64 xmmreg</td>
</tr>
</tbody>
</table>

### B.14 SSE4.1 FORMATS AND ENCODING TABLE

The tables in this section provide SSE4.1 formats and encodings. Some SSE4.1 instructions require a mandatory prefix (66H, F2H, F3H) as part of the three-byte opcode. These prefixes are included in the tables.

In 64-bit mode, some instructions requires REX.W, the byte sequence of REX.W prefix in the opcode sequence is shown.
## Table B-35. Encodings of SSE4.1 instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLENDPD — Blend Packed Double-Precision Floats</td>
<td>xmmreg2 to xmmreg1</td>
</tr>
<tr>
<td></td>
<td>mem to xmmreg</td>
</tr>
<tr>
<td>BLENDPS — Blend Packed Single-Precision Floats</td>
<td>xmmreg2 to xmmreg1</td>
</tr>
<tr>
<td></td>
<td>mem to xmmreg</td>
</tr>
<tr>
<td>BLENDVPD — Variable Blend Packed Double-Precision Floats</td>
<td>xmmreg2 to xmmreg1 &lt;xmm0&gt;</td>
</tr>
<tr>
<td></td>
<td>mem to xmmreg &lt;xmm0&gt;</td>
</tr>
<tr>
<td>BLENDVPS — Variable Blend Packed Single-Precision Floats</td>
<td>xmmreg2 to xmmreg1 &lt;xmm0&gt;</td>
</tr>
<tr>
<td></td>
<td>mem to xmmreg &lt;xmm0&gt;</td>
</tr>
<tr>
<td>DPPD — Packed Double-Precision Dot Products</td>
<td>xmmreg2 to xmmreg1, imm8</td>
</tr>
<tr>
<td></td>
<td>mem to xmmreg, imm8</td>
</tr>
<tr>
<td>DPPS — Packed Single-Precision Dot Products</td>
<td>xmmreg2 to xmmreg1, imm8</td>
</tr>
<tr>
<td></td>
<td>mem to xmmreg, imm8</td>
</tr>
</tbody>
</table>
### INSTRUCTION FORMATS AND ENCODINGS

Table B-35. Encodings of SSE4.1 instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EXTRACTPS — Extract From Packed Single-Precision Floats</strong></td>
<td></td>
</tr>
<tr>
<td>reg from xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0001 0111:11</td>
</tr>
<tr>
<td>mem from xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0001 0111:mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>INSERTPS — Insert Into Packed Single-Precision Floats</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0010 0001:11</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0010 0001:mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>MOVNTDQA — Load Double Quadword Non-temporal Aligned</strong></td>
<td></td>
</tr>
<tr>
<td>m128 to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0010 1010:11 r/m xmmreg2</td>
</tr>
<tr>
<td><strong>MPSADBW — Multiple Packed Sums of Absolute Difference</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0010 0010:11</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0010 0010:mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PACKUSDW — Pack with Unsigned Saturation</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0010 1011:11</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0010 1011:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PBLENDVB — Variable Blend Packed Bytes</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1 &lt;xmm0&gt;</td>
<td>0110 0110:0000 1111:0011 1000:0001 0000:11</td>
</tr>
<tr>
<td>mem to xmmreg &lt;xmm0&gt;</td>
<td>0110 0110:0000 1111:0011 1000:0001 0000:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PBLENDW — Blend Packed Words</strong></td>
<td></td>
</tr>
</tbody>
</table>
### Table B-35. Encodings of SSE4.1 instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0001 1110:11 xmmreg1 xmmreg2: imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0000 1110: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PCMPEQQ — Compare Packed Qword Data of Equal</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0010 1001:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0010 1001: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PEXTRB — Extract Byte</strong></td>
<td></td>
</tr>
<tr>
<td>reg from xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0001 0100:11 xmmreg reg: imm8</td>
</tr>
<tr>
<td>xmmreg to mem, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0001 0100: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PEXTRD — Extract DWord</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg to mem, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0001 0110: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PEXTRQ — Extract QWord</strong></td>
<td></td>
</tr>
<tr>
<td>r64 from xmmreg, imm8</td>
<td>0110 0110:REX.W:0000 1111:0011 1010:0001 0110:11 xmmreg reg: imm8</td>
</tr>
<tr>
<td>m64 from xmmreg, imm8</td>
<td>0110 0110:REX.W:0000 1111:0011 1010:0001 0110: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PEXTRW — Extract Word</strong></td>
<td></td>
</tr>
<tr>
<td>mem from xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0001 0101: mod xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PHMINPOSUW — Packed Horizontal Word Minimum</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0100 0001:11 xmmreg1 xmmreg2</td>
</tr>
</tbody>
</table>
### Table B-35. Encodings of SSE4.1 instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0100 0001: mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PINSRB — Extract Byte</strong></td>
<td></td>
</tr>
<tr>
<td>reg to xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0010 0000:11&lt;br&gt; xmmreg reg: imm8</td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0010 0000: mod&lt;br&gt; xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PINSRD — Extract DWord</strong></td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0010 0010: mod&lt;br&gt; xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PINSRQ — Extract QWord</strong></td>
<td></td>
</tr>
<tr>
<td>r64 to xmmreg, imm8</td>
<td>0110 0110:REX.W:0000 1111:0011 1010:0010 0010:11&lt;br&gt; xmmreg reg: imm8</td>
</tr>
<tr>
<td>m64 to xmmreg, imm8</td>
<td>0110 0110:REX.W:0000 1111:0011 1010:0010 0010: mod&lt;br&gt; xmmreg r/m: imm8</td>
</tr>
<tr>
<td><strong>PMAXSB — Maximum of Packed Signed Byte Integers</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0011 1100:11&lt;br&gt; xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0011 1100: mod&lt;br&gt; xmmreg r/m</td>
</tr>
<tr>
<td><strong>PMAXSD — Maximum of Packed Signed Dword Integers</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0011 1101:11&lt;br&gt; xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0011 1101: mod&lt;br&gt; xmmreg r/m</td>
</tr>
<tr>
<td><strong>PMAXUD — Maximum of Packed Unsigned Dword Integers</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>0110 0110:0000 1111:0011 1000:0011 1111:11&lt;br&gt; xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0011 1111: mod&lt;br&gt; xmmreg r/m</td>
</tr>
</tbody>
</table>
### Table B-35. Encodings of SSE4.1 instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PMAXUW — Maximum of Packed Unsigned Word Integers</strong></td>
<td><strong>xmmreg2 to xmmreg1</strong> 0110 0110:0000 1111:0011 1000:0011 1110:11   *</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg1 xmmreg2</strong></td>
</tr>
<tr>
<td></td>
<td><strong>mem to xmmreg</strong> 0110 0110:0000 1111:0011 1000:0011 1110: mod</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg r/m</strong></td>
</tr>
<tr>
<td><strong>PMINSB — Minimum of Packed Signed Byte Integers</strong></td>
<td><strong>xmmreg2 to xmmreg1</strong> 0110 0110:0000 1111:0011 1000:0011 1000:11   *</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg1 xmmreg2</strong></td>
</tr>
<tr>
<td></td>
<td><strong>mem to xmmreg</strong> 0110 0110:0000 1111:0011 1000:0011 1000: mod</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg r/m</strong></td>
</tr>
<tr>
<td><strong>PMINSD — Minimum of Packed Signed Dword Integers</strong></td>
<td><strong>xmmreg2 to xmmreg1</strong> 0110 0110:0000 1111:0011 1000:0011 1001:11   *</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg1 xmmreg2</strong></td>
</tr>
<tr>
<td></td>
<td><strong>mem to xmmreg</strong> 0110 0110:0000 1111:0011 1000:0011 1001: mod</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg r/m</strong></td>
</tr>
<tr>
<td><strong>PMINUD — Minimum of Packed Unsigned Dword Integers</strong></td>
<td><strong>xmmreg2 to xmmreg1</strong> 0110 0110:0000 1111:0011 1000:0011 1011:11   *</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg1 xmmreg2</strong></td>
</tr>
<tr>
<td></td>
<td><strong>mem to xmmreg</strong> 0110 0110:0000 1111:0011 1000:0011 1011: mod</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg r/m</strong></td>
</tr>
<tr>
<td><strong>PMINUW — Minimum of Packed Unsigned Word Integers</strong></td>
<td><strong>xmmreg2 to xmmreg1</strong> 0110 0110:0000 1111:0011 1000:0011 1010:11   *</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg1 xmmreg2</strong></td>
</tr>
<tr>
<td></td>
<td><strong>mem to xmmreg</strong> 0110 0110:0000 1111:0011 1000:0011 1010: mod</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg r/m</strong></td>
</tr>
<tr>
<td><strong>PMOVUSXBD — Packed Move Sign Extend - Byte to Dword</strong></td>
<td><strong>xmmreg2 to xmmreg1</strong> 0110 0110:0000 1111:0011 1000:0010 0001:11   *</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg1 xmmreg2</strong></td>
</tr>
<tr>
<td></td>
<td><strong>mem to xmmreg</strong> 0110 0110:0000 1111:0011 1000:0010 0001: mod</td>
</tr>
<tr>
<td></td>
<td><strong>xmmreg r/m</strong></td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>-----------------------</td>
<td>----------</td>
</tr>
<tr>
<td><strong>PMOVSXBQ — Packed Move Sign Extend - Byte to Qword</strong></td>
<td>0110 0110:0000 1111:0011 1000:0010 0010:11 xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000:0010 0010: mod xmmreg r/m</td>
</tr>
</tbody>
</table>

| **PMOVSXBW — Packed Move Sign Extend - Byte to Word** | 0110 0110:0000 1111:0011 1000:0010 0000:11 xmmreg1 xmmreg2 |
| xmmreg2 to xmmreg1 | |
| mem to xmmreg | 0110 0110:0000 1111:0011 1000:0010 0000: mod xmmreg r/m |

| **PMOVSXWD — Packed Move Sign Extend - Word to Dword** | 0110 0110:0000 1111:0011 1000:0010 0011:11 xmmreg1 xmmreg2 |
| xmmreg2 to xmmreg1 | |
| mem to xmmreg | 0110 0110:0000 1111:0011 1000:0010 0011: mod xmmreg r/m |

| **PMOVSXWQ — Packed Move Sign Extend - Word to Qword** | 0110 0110:0000 1111:0011 1000:0010 0100:11 xmmreg1 xmmreg2 |
| xmmreg2 to xmmreg1 | |
| mem to xmmreg | 0110 0110:0000 1111:0011 1000:0010 0100: mod xmmreg r/m |

<p>| <strong>PMOVZXBD — Packed Move Zero Extend - Byte to Dword</strong> | 0110 0110:0000 1111:0011 1000:0011 0001:11 xmmreg1 xmmreg2 |
| xmmreg2 to xmmreg1 | |
| mem to xmmreg | 0110 0110:0000 1111:0011 1000:0011 0001: mod xmmreg r/m |</p>
<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOVZXBQ — Packed Move Zero Extend - Byte to Qword</td>
<td>0110 0110:0000 1111:0011 1000: 0011 0010:11</td>
</tr>
<tr>
<td></td>
<td>xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mailed to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0011 0010: mod</td>
</tr>
<tr>
<td></td>
<td>xmmreg r/m</td>
</tr>
<tr>
<td>PMOVZXBW — Packed Move Zero Extend - Byte to Word</td>
<td>0110 0110:0000 1111:0011 1000: 0011 0000:11</td>
</tr>
<tr>
<td></td>
<td>xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mailed to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0011 0000: mod</td>
</tr>
<tr>
<td></td>
<td>xmmreg r/m</td>
</tr>
<tr>
<td></td>
<td>xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mailed to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0011 0011: mod</td>
</tr>
<tr>
<td></td>
<td>xmmreg r/m</td>
</tr>
<tr>
<td>PMOVZXWQ — Packed Move Zero Extend - Word to Qword</td>
<td>0110 0110:0000 1111:0011 1000: 0011 0011:11</td>
</tr>
<tr>
<td></td>
<td>xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mailed to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0011 0011: mod</td>
</tr>
<tr>
<td></td>
<td>xmmreg r/m</td>
</tr>
<tr>
<td>PMULDQ — Multiply Packed Signed Dword Integers</td>
<td>0110 0110:0000 1111:0011 1000: 0010 1000:11</td>
</tr>
<tr>
<td></td>
<td>xmmreg1 xmmreg2</td>
</tr>
<tr>
<td>mailed to xmmreg</td>
<td>0110 0110:0000 1111:0011 1000: 0010 1000: mod</td>
</tr>
<tr>
<td></td>
<td>xmmreg r/m</td>
</tr>
</tbody>
</table>
### INSTRUCTION FORMATS AND ENCODINGS

#### Table B-35. Encodings of SSE4.1 instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PMULLD</strong> — Multiply Packed Signed Dword Integers, Store low Result</td>
<td></td>
</tr>
</tbody>
</table>
| xmmreg2 to xmmreg1 | 0110 0110:0000 1111:0011 1000:0100 0000:11  
xmmreg1 xmmreg2 | |  
| mem to xmmreg | 0110 0110:0000 1111:0011 1000:0100 0000: mod  
xmmreg r/m | |  
| **PTEST** — Logical Compare | |  
| xmmreg2 to xmmreg1 | 0110 0110:0000 1111:0011 1000:0001 0111:11  
xmmreg1 xmmreg2 | |  
| mem to xmmreg | 0110 0110:0000 1111:0011 1000:0001 0111: mod  
xmmreg r/m | |  
| **ROUNDPD** — Round Packed Double-Precision Values | |  
| xmmreg2 to xmmreg1, imm8 | 0110 0110:0000 1111:0011 1010:0000 1001:11  
xmmreg1 xmmreg2: imm8 | |  
| mem to xmmreg, imm8 | 0110 0110:0000 1111:0011 1010:0000 1001: mod  
xmmreg r/m: imm8 | |  
| **ROUNDPSS** — Round Packed Single-Precision Values | |  
| xmmreg2 to xmmreg1, imm8 | 0110 0110:0000 1111:0011 1010:0000 1000:11  
xmmreg1 xmmreg2: imm8 | |  
| mem to xmmreg, imm8 | 0110 0110:0000 1111:0011 1010:0000 1000: mod  
xmmreg r/m: imm8 | |  
| **ROUNDSDD** — Round Scalar Double-Precision Value | |  
| xmmreg2 to xmmreg1, imm8 | 0110 0110:0000 1111:0011 1010:0000 1011:11  
xmmreg1 xmmreg2: imm8 | |  
| mem to xmmreg, imm8 | 0110 0110:0000 1111:0011 1010:0000 1011: mod  
xmmreg r/m: imm8 | |  
| **ROUNDSSS** — Round Scalar Single-Precision Value | |  
| xmmreg2 to xmmreg1, imm8 | 0110 0110:0000 1111:0011 1010:0000 1010:11  
xmmreg1 xmmreg2: imm8 | |  
| mem to xmmreg, imm8 | 0110 0110:0000 1111:0011 1010:0000 1010: mod  
xmmreg r/m: imm8 | |  

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The tables in this section provide SSE4.2 formats and encodings. Some SSE4.2 instructions require a mandatory prefix (66H, F2H, F3H) as part of the three-byte opcode. These prefixes are included in the tables. In 64-bit mode, some instructions requires REX.W, the byte sequence of REX.W prefix in the opcode sequence is shown.

### Table B-36. Encodings of SSE4.2 instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CRC32 — Accumulate CRC32</strong></td>
<td></td>
</tr>
<tr>
<td>reg2 to reg1</td>
<td>1111 0010:0000 1111:0011 1000: 1111 000w :11 reg1 reg2</td>
</tr>
<tr>
<td>mem to reg</td>
<td>1111 0010:0000 1111:0011 1000: 1111 000w : mod reg r/m</td>
</tr>
<tr>
<td>bytereg2 to reg1</td>
<td>1111 0010:0100 WR0B:0000 1111:0011 1000: 1111 0000 :11 reg1 bytereg2</td>
</tr>
<tr>
<td>m8 to reg</td>
<td>1111 0010:0100 WR0B:0000 1111:0011 1000: mod reg r/m</td>
</tr>
<tr>
<td>qwreg2 to qwreg1</td>
<td>1111 0010:0100 1R0B:0000 1111:0011 1000:11 qwreg1 qwreg2</td>
</tr>
<tr>
<td>mem64 to qwreg</td>
<td>1111 0010:0100 1R0B:0000 1111:0011 1000: mod qwreg r/m</td>
</tr>
<tr>
<td><strong>PCMPESTRI— Packed Compare Explicit-Length Strings To Index</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0110 0001:11 xmmreg1 xmmreg2:imm8</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1010:0110 0001:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PCMPESTRM— Packed Compare Explicit-Length Strings To Mask</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0110 0000:11 xmmreg1 xmmreg2:imm8</td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1010:0110 0000:mod xmmreg r/m</td>
</tr>
<tr>
<td><strong>PCMPISTRI— Packed Compare Implicit-Length String To Index</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1, imm8</td>
<td>0110 0110:0000 1111:0011 1010:0110 0011:11 xmmreg1 xmmreg2:imm8</td>
</tr>
</tbody>
</table>
INSTRUCTION FORMATS AND ENCODINGS

Table B-36.  Encodings of SSE4.2 instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1010:0110 0011:mod xmmreg r/m</td>
</tr>
</tbody>
</table>

PCMPISTRM— Packed Compare Implicit-Length Strings To Mask

<table>
<thead>
<tr>
<th>xmmreg2 to xmmreg1, imm8</th>
<th>0110 0110:0000 1111:0011 1010:0110 0010:11</th>
</tr>
</thead>
<tbody>
<tr>
<td>xmmreg1 xmmreg2: imm8</td>
<td></td>
</tr>
<tr>
<td>mem to xmmreg</td>
<td>0110 0110:0000 1111:0011 1010:0110 0010:mod xmmreg r/m</td>
</tr>
</tbody>
</table>

PCMPGTQ— Packed Compare Greater Than

<table>
<thead>
<tr>
<th>xmmreg to xmmreg</th>
<th>0110 0110:0000 1111:0011 1000:0011 0111:11</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to xmmreg</td>
<td></td>
</tr>
</tbody>
</table>

POPCNT— Return Number of Bits Set to 1

<table>
<thead>
<tr>
<th>reg2 to reg1</th>
<th>1111 0011:0000 1111:1011 1000:11 reg1 reg2</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to reg1</td>
<td>1111 0011:0000 1111:1011 1000:mod reg1 r/m</td>
</tr>
<tr>
<td>qwreg2 to qwreg1</td>
<td>1111 0011:0000 1111:1011 1000:0010:010B:1R0B:0000 1111:1011 1000:11</td>
</tr>
<tr>
<td>mem64 to qwreg1</td>
<td>1111 0011:0010 1R0B:0000 1111:1011 1000:mod reg1 r/m</td>
</tr>
</tbody>
</table>

B.16  AVX FORMATS AND ENCODING TABLE

The tables in this section provide AVX formats and encodings. A mixed form of bit/hex/symbolic forms are used to express the various bytes:

The C4/C5 and opcode bytes are expressed in hex notation; the first and second payload byte of VEX, the modR/M byte is expressed in combination of bit/symbolic form. The first payload byte of C4 is expressed as combination of bits and hex form, with the hex value preceded by an underscore. The VEX bit field to encode upper register 8-15 uses 1’s complement form, each of those bit field is expressed as lower case notation rxb, instead of RXB.

The hybrid bit-nibble-byte form is depicted below:
### Table B-37. Encodings of AVX instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VBLENDPD — Blend Packed Double-Precision Floats</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 with xmmreg3 into xmmreg1</td>
<td>C4: rxb0_3: w xmmreg2 001:0D:11 xmmreg1 xmmreg3: imm</td>
</tr>
<tr>
<td>xmmreg2 with mem to xmmreg1</td>
<td>C4: rxb0_3: w xmmreg2 001:0D:mod xmmreg1 r/m: imm</td>
</tr>
<tr>
<td>ymmreg2 with ymmreg3 into ymmreg1</td>
<td>C4: rxb0_3: w ymmreg2 101:0D:11 ymmreg1 ymmreg3: imm</td>
</tr>
<tr>
<td>ymmreg2 with mem to ymmreg1</td>
<td>C4: rxb0_3: w ymmreg2 101:0D:mod ymmreg1 r/m: imm</td>
</tr>
<tr>
<td><strong>VBLENDPS — Blend Packed Single-Precision Floats</strong></td>
<td></td>
</tr>
<tr>
<td>xmmreg2 with xmmreg3 into xmmreg1</td>
<td>C4: rxb0_3: w xmmreg2 001:0C:11 xmmreg1 xmmreg3: imm</td>
</tr>
<tr>
<td>xmmreg2 with mem to xmmreg1</td>
<td>C4: rxb0_3: w xmmreg2 001:0C:mod xmmreg1 r/m: imm</td>
</tr>
<tr>
<td>ymmreg2 with ymmreg3 into ymmreg1</td>
<td>C4: rxb0_3: w ymmreg2 101:0C:11 ymmreg1 ymmreg3: imm</td>
</tr>
<tr>
<td>ymmreg2 with mem to ymmreg1</td>
<td>C4: rxb0_3: w ymmreg2 101:0C:mod ymmreg1 r/m: imm</td>
</tr>
<tr>
<td><strong>VBLENDVPD — Variable Blend Packed Double-Precision Floats</strong></td>
<td></td>
</tr>
</tbody>
</table>

---

**Figure B-2. Hybrid Notation of VEX-Encoded Key Instruction Bytes**
### INSTRUCTION FORMATS AND ENCODINGS

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>xmmreg2 with xmmreg3 into xmmreg1 using xmmreg4 as mask</code></td>
<td>C4: rxb0_3: 0 xmmreg2 001:4B:11 xmmreg1 xmmreg3: xmmreg4</td>
</tr>
<tr>
<td><code>xmmreg2 with mem to xmmreg1 using xmmreg4 as mask</code></td>
<td>C4: rxb0_3: 0 xmmreg2 001:4B:mod xmmreg1 r/m: xmmreg4</td>
</tr>
<tr>
<td><code>ymmmreg2 with ymmreg3 into ymmreg1 using ymmreg4 as mask</code></td>
<td>C4: rxb0_3: 0 ymmreg2 101:4B:11 ymmreg1 ymmreg3: ymmreg4</td>
</tr>
<tr>
<td><code>ymmmreg2 with mem to ymmreg1 using ymmreg4 as mask</code></td>
<td>C4: rxb0_3: 0 ymmreg2 101:4B:mod ymmreg1 r/m: ymmreg4</td>
</tr>
<tr>
<td><strong>VBLENDVPS — Variable Blend Packed Single-Precision Floats</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2 with xmmreg3 into xmmreg1 using xmmreg4 as mask</code></td>
<td>C4: rxb0_3: 0 xmmreg2 001:4A:11 xmmreg1 xmmreg3: xmmreg4</td>
</tr>
<tr>
<td><code>xmmreg2 with mem to xmmreg1 using xmmreg4 as mask</code></td>
<td>C4: rxb0_3: 0 xmmreg2 001:4A:mod xmmreg1 r/m: xmmreg4</td>
</tr>
<tr>
<td><code>ymmmreg2 with ymmreg3 into ymmreg1 using ymmreg4 as mask</code></td>
<td>C4: rxb0_3: 0 ymmreg2 101:4A:11 ymmreg1 ymmreg3: ymmreg4</td>
</tr>
<tr>
<td><code>ymmmreg2 with mem to ymmreg1 using ymmreg4 as mask</code></td>
<td>C4: rxb0_3: 0 ymmreg2 101:4A:mod ymmreg1 r/m: ymmreg4</td>
</tr>
<tr>
<td><strong>VDPPD — Packed Double-Precision Dot Products</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2 with xmmreg3 into xmmreg1</code></td>
<td>C4: rxb0_3: w xmmreg2 001:41:11 xmmreg1 xmmreg3: imm</td>
</tr>
<tr>
<td><code>xmmreg2 with mem to xmmreg1</code></td>
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<td>xmmreg2 with xmmreg1, imm8</td>
<td>C4: rxb0_3: w_F 001:60:11 xmmreg1 xmmreg2: imm</td>
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<td>C4: rxb0_3: w_F 001:60:mod xmmreg1 r/m: imm</td>
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<td>mem with xmmreg1, imm8</td>
<td>C4: rxb0_3: w_F 001:63:mod xmmreg1 r/m: imm</td>
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<td><strong>VAEDECLAST — Perform Last Round of an AES Decryption Flow</strong></td>
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<td>xmmreg2 with xmmreg3 to xmmreg1</td>
<td>C4: rxb0_2: w xmmreg2 001:DF:11 xmmreg1 xmmreg3</td>
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<td>xmmreg2 with mem to xmmreg1</td>
<td>C4: rxb0_2: w xmmreg2 001:DF:mod xmmreg1 r/m</td>
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<tr>
<td>xmmreg2 with mem to xmmreg1</td>
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<td><strong>VAESENCLAST — Perform Last Round of an AES Encryption Flow</strong></td>
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<td>mem to xmmreg, imm8</td>
<td>C4: rxb0_3: w_F 001:DF:mod xmmreg1 r/m: imm</td>
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<td><strong>VPABSB — Packed Absolute Value</strong></td>
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<td>xmmreg2 to xmmreg1</td>
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<td>mem to xmmreg1</td>
<td>C4: rxb0_2: w_F 001:1C:mod xmmreg1 r/m</td>
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<td><strong>VPABSD — Packed Absolute Value</strong></td>
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<td>xmmreg2 to xmmreg1</td>
<td>C4: rxb0_2: w_F 001:1E:11 xmmreg1 xmmreg2</td>
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<tr>
<td>mem to xmmreg1</td>
<td>C4: rxb0_2: w_F 001:1E:mod xmmreg1 r/m</td>
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<td>**VPSHUFB — Packed Shuffle Bytes</td>
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<td>**VPSIGNB — Packed SIGN</td>
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<td>C4: rb0_2: w xmmreg2 001:0B:11 xmmreg1 xmmreg3</td>
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<td>C4: rb0_2: w xmmreg2 001:0B:mod xmmreg1 r/m</td>
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<td>C4: rb0_2: w xmmreg2 001:09:mod xmmreg1 r/m</td>
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<td>**VADDSUBPD — Packed Double-FP Add/Sub-</td>
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<td>xmmreg2 with xmmreg3 to xmmreg1</td>
<td>C4: rb0_1: w xmmreg2 001:D0:11 xmmreg1 xmmreg3</td>
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<td>C4: rb0_1: w xmmreg2 001:D0:mod xmmreg1 r/m</td>
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<td>xmmreg1</td>
<td>C5: r xmmreglo2 001:D0:11 xmmreg1 xmmreglo3</td>
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<td>xmmreglo2 with mem to xmmreg1</td>
<td>C5: r xmmreglo2 001:D0:mod xmmreg1 r/m</td>
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<td>**VADDSUBPS — Packed Single-FP Add/Sub-</td>
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<td>(C5: r_{\text{xmmreglo2}} 011:00:11 \text{xmmreg1} \text{xmmreglo3})</td>
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<td>xmmreglo2 with mem to xmmreg1</td>
<td>(C5: r_{\text{xmmreglo2}} 011:00:mod \text{xmmreg1} r/m)</td>
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<td>ymmreg2 with ymmreg3 to ymmreg1</td>
<td>(C4: rxb0_1: w \text{ ymmreg2} 111:00:11 \text{ ymmreg1} \text{ ymmreg3})</td>
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<td>ymmreg2 with mem to ymmreg1</td>
<td>(C4: rxb0_1: w \text{ ymmreg2} 111:00:mod \text{ ymmreg1} r/m)</td>
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<td>ymmreglo2 with ymmreglo3 to ymmreg1</td>
<td>(C5: r_{\text{ymmreglo2}} 111:00:11 \text{ ymmreg1} \text{ ymmreglo3})</td>
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<tr>
<td>ymmreglo2 with mem to ymmreg1</td>
<td>(C5: r_{\text{ymmreglo2}} 111:00:mod \text{ ymmreg1} r/m)</td>
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**VHADDPD — Packed Double-FP Horizontal Add**

| xmmreglo2 with xmmreg3 to xmmreg1 | \(C4: rxb0_1: w \text{ xmmreg2} 001:7C:11 \text{ xmmreg1} \text{ xmmreg3}\) |
| xmmreglo2 with mem to xmmreg1 | \(C4: rxb0_1: w \text{ xmmreg2} 001:7C:mod \text{ xmmreg1} r/m\) |
| xmmreglo2 with xmmreglo3 to xmmreg1 | \(C5: r_{\text{xmmreglo2}} 001:7C:11 \text{ xmmreg1} \text{ xmmreglo3}\) |
| xmmreglo2 with mem to xmmreg1 | \(C5: r_{\text{xmmreglo2}} 001:7C:mod \text{ xmmreg1} r/m\) |
| ymmreg2 with ymmreg3 to ymmreg1 | \(C4: rxb0_1: w \text{ ymmreg2} 101:7C:11 \text{ ymmreg1} \text{ ymmreg3}\) |
| ymmreg2 with mem to ymmreg1 | \(C4: rxb0_1: w \text{ ymmreg2} 101:7C:mod \text{ ymmreg1} r/m\) |
| ymmreglo2 with ymmreglo3 to ymmreg1 | \(C5: r_{\text{ymmreglo2}} 101:7C:11 \text{ ymmreg1} \text{ ymmreglo3}\) |
| ymmreglo2 with mem to ymmreg1 | \(C5: r_{\text{ymmreglo2}} 101:7C:mod \text{ ymmreg1} r/m\) |

**VHaddirps — Packed Single-FP Horizontal Add**

| xmmreglo2 with xmmreg3 to xmmreg1 | \(C4: rxb0_1: w \text{ xmmreg2} 011:7C:11 \text{ xmmreg1} \text{ xmmreg3}\) |
| xmmreglo2 with mem to xmmreg1 | \(C4: rxb0_1: w \text{ xmmreg2} 011:7C:mod \text{ xmmreg1} r/m\) |
| xmmreglo2 with xmmreglo3 to xmmreg1 | \(C5: r_{\text{xmmreglo2}} 011:7C:11 \text{ xmmreg1} \text{ xmmreglo3}\) |
| xmmreglo2 with mem to xmmreg1 | \(C5: r_{\text{xmmreglo2}} 011:7C:mod \text{ xmmreg1} r/m\) |
| ymmreg2 with ymmreg3 to ymmreg1 | \(C4: rxb0_1: w \text{ ymmreg2} 111:7C:11 \text{ ymmreg1} \text{ ymmreg3}\) |
| ymmreg2 with mem to ymmreg1 | \(C4: rxb0_1: w \text{ ymmreg2} 111:7C:mod \text{ ymmreg1} r/m\) |
| ymmreglo2 with ymmreglo3 to ymmreg1 | \(C5: r_{\text{ymmreglo2}} 111:7C:11 \text{ ymmreg1} \text{ ymmreglo3}\) |
| ymmreglo2 with mem to ymmreg1 | \(C5: r_{\text{ymmreglo2}} 111:7C:mod \text{ ymmreg1} r/m\) |

**VHSUBPD — Packed Double-FP Horizontal Subtract**
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<td>C4: rxb0_1: w xmmreg2 001:7D:11 xmmreg1 xmmreg3</td>
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<tr>
<td>xmmreg2 with mem to xmmreg1</td>
<td>C4: rxb0_1: w xmmreg2 001:7D:mod xmmreg1 r/m</td>
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<td>xmmreglo2 with xmmreglo3 to xmmreg1</td>
<td>C5: r_xmmreglo2 001:7D:11 xmmreg1 xmmreglo3</td>
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<tr>
<td>xmmreglo2 with mem to xmmreg1</td>
<td>C5: r_xmmreglo2 001:7D:mod xmmreg1 r/m</td>
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<tr>
<td>ymmreg2 with mem to ymmreg1</td>
<td>C4: rxb0_1: w ymmreg2 101:7D:mod ymmreg1 r/m</td>
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<td>ymmreglo2 with ymmreglo3 to ymmreg1</td>
<td>C5: r_ymmreglo2 101:7D:11 ymmreg1 ymmreglo3</td>
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<tr>
<td>ymmreglo2 with mem to ymmreg1</td>
<td>C5: r_ymmreglo2 101:7D:mod ymmreg1 r/m</td>
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<td><strong>VHSUBPS — Packed Single-FP Horizontal Subtract</strong></td>
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<td>C4: rxb0_1: w ymmreg2 111:7D:11 ymmreg1 ymmreg3</td>
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<td>ymmreg2 with mem to ymmreg1</td>
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<td>ymmreglo2 with mem to ymmreg1</td>
<td>C5: r_ymmreglo2 111:7D:mod ymmreg1 r/m</td>
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<td><strong>VLDDQU — Load Unaligned Integer 128 Bits</strong></td>
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<td>mem to xmmreg1</td>
<td>C4: rxb0_1: w_F 011:F0:mod xmmreg1 r/m</td>
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<tr>
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<td>C5: r_F 011:F0:mod xmmreg1 r/m</td>
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<tr>
<td>mem to ymmreg1</td>
<td>C4: rxb0_1: w_F 111:F0:mod ymmreg1 r/m</td>
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<tr>
<td>mem to ymmreg1</td>
<td>C5: r_F 111:F0:mod ymmreg1 r/m</td>
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<td><strong>VMOVDDUP — Move One Double-FP and Duplicate</strong></td>
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## INSTRUCTION FORMATS AND ENCODINGS

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<td>C5: r_F 011:12:mod xmmreg1 r/m</td>
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<tr>
<td>ymmreg2 to ymmreg1</td>
<td>C4: rxb0_1: w_F 111:12:11 ymmreg1 ymmreg2</td>
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<td>C5: r_F 111:12:11 ymmreg1 ymmreglo</td>
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<td>mem to ymmreg1</td>
<td>C5: r_F 111:12:mod ymmreg1 r/m</td>
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**VMOVHLPS — Move Packed Single-Precision Floating-Point Values High to Low**

- xmmreg2 and xmmreg3 to xmmreg1: C4: rxb0_1: w xmmreg2 000:12:11 xmmreg1 xmmreg3
- xmmreglo2 and xmmreglo3 to xmmreg1: C5: r_xxmmreglo2 000:12:11 xmmreg1 xmmreglo3

**VMOVSHDUP — Move Packed Single-FP High and Duplicate**

- xmmreg2 to xmmreg1: C4: rxb0_1: w_F 010:16:11 xmmreg1 xmmreg2
- mem to xmmreg1: C4: rxb0_1: w_F 010:16:mod xmmreg1 r/m
- xmmreglo to xmmreg1: C5: r_F 010:16:11 xmmreg1 xmmreglo
- mem to xmmreg1: C5: r_F 010:16:mod xmmreg1 r/m
- ymmreg2 to ymmreg1: C4: rxb0_1: w_F 110:16:11 ymmreg1 ymmreg2
- mem to ymmreg1: C4: rxb0_1: w_F 110:16:mod ymmreg1 r/m
- ymmreglo to ymmreg1: C5: r_F 110:16:11 ymmreg1 ymmreglo
- mem to ymmreg1: C5: r_F 110:16:mod ymmreg1 r/m

**VMOVSLDUP — Move Packed Single-FP Low and Duplicate**

- xmmreg2 to xmmreg1: C4: rxb0_1: w_F 010:12:11 xmmreg1 xmmreg2
- mem to xmmreg1: C4: rxb0_1: w_F 010:12:mod xmmreg1 r/m
- xmmreglo to xmmreg1: C5: r_F 010:12:11 xmmreg1 xmmreglo
- mem to xmmreg1: C5: r_F 010:12:mod xmmreg1 r/m
- ymmreg2 to ymmreg1: C4: rxb0_1: w_F 110:12:11 ymmreg1 ymmreg2
- mem to ymmreg1: C4: rxb0_1: w_F 110:12:mod ymmreg1 r/m
- ymmreglo to ymmreg1: C5: r_F 110:12:11 ymmreg1 ymmreglo
- mem to ymmreg1: C5: r_F 110:12:mod ymmreg1 r/m

**VADDPPD — Add Packed Double-Precision Floating-Point Values**
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<td>xmmreg2 with xmmreg3 to xmmreg1</td>
<td>C4: rxb0_1: w xmmreg2 001:58:11 xmmreg1 xmmreg3</td>
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<td>xmmreg2 with mem to xmmreg1</td>
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<td>C5: r_yymmreglo2 101:58:11 ymmreg1 ymmreglo3</td>
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<td>C5: r_yymmreglo2 101:58:mod ymmreg1 r/m</td>
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<td>VADDSD — Add Scalar Double-Precision Floating-Point Values</td>
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**VCMPPD — Compare Packed Double-Precision Floating-Point Values**

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<td><code>ymmreglo2 with mem to ymmreg1</code></td>
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**VCMPSD — Compare Scalar Double-Precision Floating-Point Values**

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**VCOMISD — Compare Scalar Ordered Double-Precision Floating-Point Values and Set EFLAGS**

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<td>C5: r_F 001:2F:mod xmmreg1 r/m</td>
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<td>VCVTDQ2PD— Convert Packed Dword Integers to Packed Double-Precision FP Values</td>
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VCVTPD2PS— Convert Packed Double-Precision FP Values to Packed Single-Precision FP Values

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VCVTPS2DQ— Convert Packed Single-Precision FP Values to Packed Dword Integers

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VCVTPS2PD— Convert Packed Single-Precision FP Values to Packed Double-Precision FP Values

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**VCVTSI2SD— Convert Scalar Double-Precision FP Value to Integer**

| mem to reg32           | C4: rxb0_1: 0_F 011:2D:11 reg ymmreg1 |
| xmmreglo to reg32      | C4: r_F 011:2D:11 reg ymmreglo |
| mem to reg32           | C5: r_F 011:2D:mod reg ymmreglo |
| ymmreg1 to reg64       | C4: rxb0_1: 1_F 111:2D:11 reg ymmreg1 |
| mem to reg64           | C4: rxb0_1: 1_F 111:2D:mod reg ymmreg1 |

**VCVTSI2SS — Convert Scalar Double-Precision FP Value to Scalar Single-Precision FP Value**

| xmmreg2 with xmmreg3 to xmmreg1 | C4: rxb0_1: w xmmreg2 011:5A:11 xmmreg1 xmmreg3 |
| xmmreg2 with mem to xmmreg1    | C4: rxb0_1: w xmmreg2 011:5A:mod xmmreg1 r/m |
| xmmreglo2 with xmmreglo3 to xmmreg1 | C5: r_xmmreglo2 011:5A:11 xmmreg1 xmmreglo3 |
| xmmreglo2 with mem to xmmreg1 | C5: r_xmmreglo2 011:5A:mod xmmreg1 r/m |

**VCVTSS2SD — Convert Scalar Single-Precision FP Value to Scalar Double-Precision FP Value**

| xmmreg2 with xmmreg3 to xmmreg1 | C4: rxb0_1: w xmmreg2 010:5A:11 xmmreg1 xmmreg3 |
| xmmreg2 with mem to xmmreg1    | C4: rxb0_1: w xmmreg2 010:5A:mod xmmreg1 r/m |
| xmmreglo2 with xmmreglo3 to xmmreg1 | C5: r_xmmreglo2 010:5A:11 xmmreg1 xmmreglo3 |
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### VMINPD — Return Minimum Packed Double-Precision Floating-Point Values

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### VMINSND — Return Minimum Scalar Double-Precision Floating-Point Value

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### VMOVAPD — Move Aligned Packed Double-Precision Floating-Point Values

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**VMOVDBQ — Move Unaligned Double Quadword**

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<td>C4: rxb0_1: w xmmreg1 001:16:11 xmmreg2 r/m</td>
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<td>C5: r_xmmreg1 001:16:11 xmmreglo2 r/m</td>
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<td>xmmreg1 to mem</td>
<td>C4: rxb0_1: w_F 001:17:mod r/m xmmreg1</td>
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<td>xmmreglo to mem</td>
<td>C5: r_F 001:17:mod r/m xmmreglo</td>
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<td><strong>VMOVLPD</strong> — Move Low Packed Double-Precision Floating-Point Value</td>
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<td>xmmreg1 and mem to xmmreg2</td>
<td>C4: rxb0_1: w xmmreg1 001:12:11 xmmreg2 r/m</td>
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<td>C5: r_xmmreg1 001:12:11 xmmreglo2 r/m</td>
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<td>C4: rxb0_1: w_F 001:13:mod r/m xmmreg1</td>
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<td>xmmreglo to mem</td>
<td>C5: r_F 001:13:mod r/m xmmreglo</td>
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<td><strong>VMOVMSKPD</strong> — Extract Packed Double-Precision Floating-Point Sign Mask</td>
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<td>xmmreg2 to reg</td>
<td>C4: rxb0_1: w_F 001:50:11 reg xmmreg1</td>
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<td>xmmreglo to reg</td>
<td>C5: r_F 001:50:11 reg xmmreglo</td>
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<td>C4: rxb0_1: w_F 101:50:11 reg ymmreg1</td>
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<td>ymmreglo to reg</td>
<td>C5: r_F 101:50:11 reg ymmreglo</td>
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<td><strong>VMOVNTDQ</strong> — Store Double Quadword Using Non-Temporal Hint</td>
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<td>xmmreg1 to mem</td>
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<td>xmmreglo to mem</td>
<td>C5: r_F 001:E7:11 r/m xmmreglo</td>
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<td>C4: rxb0_1: w_F 101:E7:11 r/m ymmreg1</td>
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<td>C5: r_F 101:E7:11 r/m ymmreglo</td>
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<td><strong>VMOVNTPD</strong> — Store Packed Double-Precision Floating-Point Values Using Non-Temporal Hint</td>
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<td>xmmreg1 to mem</td>
<td>C4: rxb0_1: w_F 001:2B:11 r/m xmmreg1</td>
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<td>xmmreglo to mem</td>
<td>C5: r_F 001:2B:11 r/m xmmreglo</td>
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<td>ymmreg1 to mem</td>
<td>C4: rxb0_1: w_F 101:2B:11r/m ymmreg1</td>
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<td>ymmreglo to mem</td>
<td>C5: r_F 101:2B:11r/m ymmreglo</td>
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<td><strong>VMOVSD</strong> — Move Scalar Double-Precision Floating-Point Value</td>
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<td>C4: rxb0_1: w xmmreg2 011:10:11 xmmreg1 xmmreg3</td>
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<td>mem to xmmreg1</td>
<td>C4: rxb0_1: w_F 011:10:mod xmmreg1 r/m</td>
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<td>xmmreglo to mem</td>
<td>C5: r_F 011:11:mod r/m xmmreglo</td>
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**VMOVUPD — Move Unaligned Packed Double-Precision Floating-Point Values**

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<td>C5: r_F 001:10:mod xmmreg1 r/m</td>
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<td>ymmreg2 to ymmreg1</td>
<td>C4: rxb0_1: w_F 101:10:11 ymmreg1 ymmreg2</td>
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<td>mem to ymmreg1</td>
<td>C4: rxb0_1: w_F 101:10:mod ymmreg1 r/m</td>
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<td>C4: rxb0_1: w_F 001:11:mod r/m xmmreg1</td>
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**VMULPD — Multiply Packed Double-Precision Floating-Point Values**

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<td>xmmreg2 with mem to xmmreg1</td>
<td>C4: rxb0_1: w xmmreg2 001:59:mod xmmreg1 r/m</td>
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<td>xmmreglo2 with xmmreglo3 to xmmreg1</td>
<td>CS: r_xmmreglo2 001:59:11 xmmreg1 xmmreglo3</td>
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<td>xmmreglo2 with mem to xmmreg1</td>
<td>CS: r_xmmreglo2 001:59:mod xmmreg1 r/m</td>
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<td>ymmreg2 with ymmreg3 to ymmreg1</td>
<td>C4: rxb0_1: w ymmreg2 101:59:11 ymmreg1 ymmreg3</td>
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<td>ymmreg2 with mem to ymmreg1</td>
<td>C4: rxb0_1: w ymmreg2 101:59:mod ymmreg1 r/m</td>
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<td>C5: r_ymmreglo2 101:59:11 ymmreg1 ymmreglo3</td>
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<td>ymmreglo2 with mem to ymmreg1</td>
<td>C5: r_ymmreglo2 101:59:mod ymmreg1 r/m</td>
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<td><strong>VMULSD — Multiply Scalar Double-Precision Floating-Point Values</strong></td>
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<td>C4: rxb0_1: w xmmreg2 011:59:11 xmmreg1 xmmreg3</td>
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<td><strong>VORPD — Bitwise Logical OR of Double-Precision Floating-Point Values</strong></td>
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<td><strong>VPACKSSWB — Pack with Signed Saturation</strong></td>
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<td>C5: r_xmmreglo2 001:63:11 xmmreg1 xmmreglo3</td>
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<td><strong>VPACKUSWB— Pack with Unsigned Saturation</strong></td>
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<td><strong>VPADDB — Add Packed Integers</strong></td>
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<td><strong>VPADDD — Add Packed Integers</strong></td>
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<td>VPADDQ — Add Packed Quadword Integers</td>
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<td>VPADDSB — Add Packed Signed Integers with Signed Saturation</td>
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<td>VPADDUSB — Add Packed Unsigned Integers with Unsigned Saturation</td>
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<td><strong>VPAVGw — Average Packed Integers</strong></td>
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<td>C4: rxb0_1: w xmmreg2 001:E3:11 xmmreg1 xmmreg3</td>
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<td><strong>VPCMPEQW — Compare Packed Data for Equal</strong></td>
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<td>C4: rxb0_1: w xmmreg2 001:75:11 xmmreg1 xmmreg3</td>
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<td>C4: rxb0_1: w xmmreg2 001:76:11 xmmreg1 xmmreg3</td>
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<td><strong>VPCMPGTB — Compare Packed Signed Integers for Greater Than</strong></td>
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### INSTRUCTION FORMATS AND ENCODINGS

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#### VPextract Word

- `xmmreg1 to reg using imm`  
  
  C4: rxb0_1: 0_F 001:C5:11 reg xmmreg1: imm  

- `xmmreg1 to reg using imm`  
  
  C5: r_F 001:C5:11 reg xmmreg1: imm

#### VPinsRW — Insert Word

- `xmmreg2 with reg to xmmreg1`  
  
  C4: rxb0_1: w xmmreg2 001:F5:11 xmmreg1 xmmreg3  

- `xmmreg2 with mem to xmmreg1`  
  
  C4: rxb0_1: w xmmreg2 001:F5:mod xmmreg1 r/m  

- `xmmreglo2 with xmmreglo3 to xmmreg1`  
  
  C5: r_xmmreglo2 001:F5:11 xmmreg1 xmmreglo3  

- `xmmreglo2 with mem to xmmreg1`  
  
  C5: r_xmmreglo2 001:F5:mod xmmreg1 r/m

#### VPMADDWD — Multiply and Add Packed Integers

- `xmmreg2 with xmmreg3 to xmmreg1`  
  
  C4: rxb0_1: w xmmreg2 001:EE:11 xmmreg1 xmmreg3  

- `xmmreg2 with mem to xmmreg1`  
  
  C4: rxb0_1: w xmmreg2 001:EE:mod xmmreg1 r/m  

- `xmmreglo2 with xmmreglo3 to xmmreg1`  
  
  C5: r_xmmreglo2 001:EE:11 xmmreg1 xmmreglo3  

- `xmmreglo2 with mem to xmmreg1`  
  
  C5: r_xmmreglo2 001:EE:mod xmmreg1 r/m

#### VPMAXSW — Maximum of Packed Signed Word Integers

- `xmmreg2 with xmmreg3 to xmmreg1`  
  
  C4: rxb0_1: w xmmreg2 001:DE:11 xmmreg1 xmmreg3  

- `xmmreg2 with mem to xmmreg1`  
  
  C4: rxb0_1: w xmmreg2 001:DE:mod xmmreg1 r/m  

- `xmmreglo2 with xmmreglo3 to xmmreg1`  
  
  C5: r_xmmreglo2 001:DE:11 xmmreg1 xmmreglo3  

- `xmmreglo2 with mem to xmmreg1`  
  
  C5: r_xmmreglo2 001:DE:mod xmmreg1 r/m

#### VPMINSW — Minimum of Packed Signed Word Integers

- `xmmreg2 with xmmreg3 to xmmreg1`  
  
  C4: rxb0_1: w xmmreg2 001:E9:11 xmmreg1 xmmreg3  

- `xmmreg2 with mem to xmmreg1`  
  
  C4: rxb0_1: w xmmreg2 001:E9:mod xmmreg1 r/m  

- `xmmreglo2 with xmmreglo3 to xmmreg1`  
  
  C5: r_xmmreglo2 001:E9:11 xmmreg1 xmmreglo3  

- `xmmreglo2 with mem to xmmreg1`  
  
  C5: r_xmmreglo2 001:E9:mod xmmreg1 r/m
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<td>xmmreg1 to reg</td>
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### VPMULUDQ — Multiply Packed Unsigned Doubleword Integers

| xmmreg2 with xmmreg3 to xmmreg1 | C4: rxb0_1: w xmmreg2 001:F4:11 xmmreg1 xmmreg3 |
| xmmreg2 with mem to xmmreg1 | C4: rxb0_1: w xmmreg2 001:F4:mod xmmreg1 r/m |
| xmmreglo2 with xmmreglo3 to xmmreg1 | C5: r_xmmreglo2 001:F4:11 xmmreg1 xmmreglo3 |
| xmmreglo2 with mem to xmmreg1 | C5: r_xmmreglo2 001:F4:mod xmmreg1 r/m |

### VPOR — Bitwise Logical OR

| xmmreg2 with xmmreg3 to xmmreg1 | C4: rxb0_1: w xmmreg2 001:EB:11 xmmreg1 xmmreg3 |
| xmmreg2 with mem to xmmreg1 | C4: rxb0_1: w xmmreg2 001:EB:mod xmmreg1 r/m |
| xmmreglo2 with xmmreglo3 to xmmreg1 | C5: r_xmmreglo2 001:EB:11 xmmreg1 xmmreglo3 |
| xmmreglo2 with mem to xmmreg1 | C5: r_xmmreglo2 001:EB:mod xmmreg1 r/m |

### VPSADBW — Compute Sum of Absolute Differences

| xmmreg2 with xmmreg3 to xmmreg1 | C4: rxb0_1: w xmmreg2 001:F6:11 xmmreg1 xmmreg3 |
| xmmreg2 with mem to xmmreg1 | C4: rxb0_1: w xmmreg2 001:F6:mod xmmreg1 r/m |
| xmmreglo2 with xmmreglo3 to xmmreg1 | C5: r_xmmreglo2 001:F6:11 xmmreg1 xmmreglo3 |
| xmmreglo2 with mem to xmmreg1 | C5: r_xmmreglo2 001:F6:mod xmmreg1 r/m |

### VPSHUFWD — Shuffle Packed Doublewords

| xmmreg2 to xmmreg1 using imm | C4: rxb0_1: w_F 001:70:11 xmmreg1 xmmreg2:imm |
| mem to xmmreg1 using imm | C4: rxb0_1: w_F 001:70:mod xmmreg1 r/m:imm |
| xmmreglo to xmmreg1 using imm | C5: r_F 001:70:11 xmmreg1 xmmreglo:imm |
| mem to xmmreg1 using imm | C5: r_F 001:70:mod xmmreg1 r/m:imm |

### VPSHUFW — Shuffle Packed High Words

<p>| xmmreg2 to xmmreg1 using imm | C4: rxb0_1: w_F 010:70:11 xmmreg1 xmmreg2:imm |
| mem to xmmreg1 using imm | C4: rxb0_1: w_F 010:70:mod xmmreg1 r/m:imm |
| xmmreglo to xmmreg1 using imm | C5: r_F 010:70:11 xmmreg1 xmmreglo:imm |</p>
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<td><strong>VPSHUFLW — Shuffle Packed Low Words</strong></td>
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<td>mem to xmmreg1 using imm</td>
<td>C4: rxb0_1: w_F 011:70:mod xmmreg1 r/m: imm</td>
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<td>xmmreglo to xmmreg1 using imm</td>
<td>C5: r_F 011:70:11 xmmreg1 xmmreglo: imm</td>
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<tr>
<td>mem to xmmreg1 using imm</td>
<td>C5: r_F 011:70:mod xmmreg1 r/m: imm</td>
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<td><strong>VPSLLDQ — Shift Double Quadword Left Logical</strong></td>
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<td>xmmreg2 to xmmreg1 using imm</td>
<td>C4: rxb0_1: w_F 001:73:11 xmmreg1 xmmreg2: imm</td>
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<td>C5: r_xmmreglo2 001:F1:mod xmmreg1 r/m</td>
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<td>xmmreglo to xmmreg1 using imm11</td>
<td>C4: rxb0_1: w_F 001:71:11 xmmreg1 xmmreglo2: imm</td>
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<td>xmmreglo to xmmreg1 using imm8</td>
<td>C5: r_F 001:71:11 xmmreg1 xmmreglo: imm</td>
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**VPSRAW — Shift Packed Data Right Arithmetic**

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**VPSRAD — Shift Packed Data Right Arithmetic**

<table>
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<td>C4: rxb0_1: w xmmreg2 001:E2:11 xmmreg1 xmmreglo3</td>
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<td>C5: r_xmmreglo2 001:E2:11 xmmreg1 xmmreglo3</td>
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<td>xmmreglo2 to xmmreg1 using imm8</td>
<td>C4: rxb0_1: w_F 001:72:11 xmmreg1 xmmreglo2: imm</td>
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<td>xmmreglo to xmmreg1 using imm8</td>
<td>C5: r_F 001:72:11 xmmreg1 xmmreglo: imm</td>
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**VPSRLDQ — Shift Double Quadword Right Logical**

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<td>xmmreglo2 to xmmreg1 using imm8</td>
<td>C4: rxb0_1: w_F 001:73:11 xmmreg1 xmmreglo2: imm</td>
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<td>C5: r_F 001:73:11 xmmreg1 xmmreglo: imm</td>
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**VPSRLW — Shift Packed Data Right Logical**

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<td>C5: r_xmmreglo2 001:D1:11 xmmreg1 xmmreglo3</td>
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<td>C5: r_xmmreglo2 001:D1:mod xmmreg1 r/m</td>
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<td>xmmreg2 to xmmreg1 using imm8</td>
<td>C4: rxb0_1: w_F 001:71:11 xmmreg1 xmmreg2: imm</td>
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<td>xmmreglo to xmmreg1 using imm8</td>
<td>C5: r_F 001:71:11 xmmreg1 xmmreglo: imm</td>
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<td><strong>VPSRLD — Shift Packed Data Right Logical</strong></td>
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#### VPSUBQ — Subtract Packed Quadword Integers

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<td>C5: r xmmreglo2 001:FB:mod xmmreg1 r/m</td>
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#### VPSUBSB — Subtract Packed Signed Integers with Signed Saturation

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#### VPSUBSW — Subtract Packed Signed Integers with Signed Saturation

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#### VPSUBUSB — Subtract Packed Unsigned Integers with Unsigned Saturation

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<td>C5: r xmmreglo2 001:D8:11 xmmreg1 xmmreglo3</td>
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<tr>
<td>xmmreglo2 with mem to xmmreg1</td>
<td>C5: r xmmreglo2 001:D8:mod xmmreg1 r/m</td>
</tr>
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<td>C4: rxb0_1: w xmmreg2 001:D9:11 xmmreg1 xmmreg3</td>
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<td>C5: r_xmmreglo2 001:D9:mod xmmreg1 r/m</td>
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<td><strong>VPUNPCKHBW — Unpack High Data</strong></td>
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<tr>
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<td>C4: rxb0_1: w xmmreg2 001:68:11 xmmreg1 xmmreg3</td>
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<td>xmmreg2 with xmmreg3 to xmmreg1</td>
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<td><strong>VPUNPCKLBD — Unpack Low Data</strong></td>
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<td>C4: rxb0_1: w_F 001:51:mod xmmreg1 r/m</td>
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<tr>
<td>xmmreglo to xmmreg1</td>
<td>C5: r_F 001:51:11 xmmreg1 xmmreglo</td>
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<td>C5: r_F 001:51:mod xmmreg1 r/m</td>
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<td>C4: rxb0_1: w_F 101:51:11 ymmreg1 ymmreg2</td>
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<td>C4: rxb0_1: w xmmreg2 011:51:11 xmmreg1 xmmreg3</td>
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<td>C5: r_xmmreglo2 011:51:11 xmmreg1 xmmreglo3</td>
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<td>VSUBPD — Subtract Packed Double-Precision Floating-Point Values</td>
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<td>xmmreg2 with xmmreg3 to xmmreg1</td>
<td>C4: rb0_1: w xmmreg2 001:5C:11 xmmreg1 xmmreg3</td>
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<td>C5: _r_ymmreglo2 101:5C:mod ymmreg1 r/m</td>
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</table>

**VSUBSD — Subtract Scalar Double-Precision Floating-Point Values**

| xmmreg2 with xmmreg3 to xmmreg1 | C4: rb0_1: w xmmreg2 011:5C:11 xmmreg1 xmmreg3 |
| xmmreg2 with mem to xmmreg1 | C4: rb0_1: w xmmreg2 011:5C:mod xmmreg1 r/m |
| xmmreglo2 with xmmreglo3 to xmmreg1 | C5: _r_xmmreglo2 011:5C:11 xmmreg1 xmmreglo3 |
| xmmreglo2 with mem to xmmreg1 | C5: _r_xmmreglo2 011:5C:mod xmmreg1 r/m |

**VUCOMISD — Unordered Compare Scalar Double-Precision Floating-Point Values and Set EFLAGS**

| xmmreg2 with xmmreg1, set EFLAGS | C4: rb0_1: w_F xmmreg1 001:2E:11 xmmreg2 |
| mem with xmmreg1, set EFLAGS | C4: rb0_1: w_F xmmreg1 001:2E:mod r/m |
| xmmreglo with xmmreg1, set EFLAGS | C5: r_F xmmreg1 001:2E:11 xmmreglo |
| mem with xmmreg1, set EFLAGS | C5: r_F xmmreg1 001:2E:mod r/m |

**VUNPCKHPD — Unpack and Interleave High Packed Double-Precision Floating-Point Values**

<p>| xmmreg2 with xmmreg3 to xmmreg1 | C4: rb0_1: w xmmreg2 001:15:11 xmmreg1 xmmreg3 |
| xmmreg2 with mem to xmmreg1 | C4: rb0_1: w xmmreg2 001:15:mod xmmreg1 r/m |
| xmmreglo2 with xmmreglo3 to xmmreg1 | C5: _r_xmmreglo2 001:15:11 xmmreg1 xmmreglo3 |
| xmmreglo2 with mem to xmmreg1 | C5: _r_xmmreglo2 001:15:mod xmmreg1 r/m |
| ymmreg2 with ymmreg3 to ymmreg1 | C4: rb0_1: w ymmreg2 101:15:11 ymmreg1 ymmreg3 |
| ymmreg2 with mem to ymmreg1 | C4: rb0_1: w ymmreg2 101:15:mod ymmreg1 r/m |</p>
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<td>C4: rxb0_1: w xmmreg2 001:14:11 xmmreg1 xmmreg3</td>
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### VXORPD — Bitwise Logical XOR for Double-Precision Floating-Point Values

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### VADDS — Add Packed Single-Precision Floating-Point Values

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<td>C4: rbbo_1: 0 xmmreg2 010:2A:11 xmmreg1 reg</td>
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<td><strong>VCVTSI2SS</strong> — Convert Dword Integer to Scalar Single-Precision FP Value</td>
<td>C4: rbbo_1: 0 xmmreg2 010:2A:mod xmmreg1 r/m</td>
</tr>
<tr>
<td><strong>VCVTSI2SS</strong> — Convert Dword Integer to Scalar Single-Precision FP Value</td>
<td>C4: rbbo_1: 1 xmmreg2 010:2A:11 xmmreg1 reg</td>
</tr>
</tbody>
</table>
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<table>
<thead>
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<tbody>
<tr>
<td>xmmreg2 with mem to xmmreg1</td>
<td>C4: rxb0_1: 1 xmmreg2 010:2A:mod xmmreg1 r/m</td>
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#### VCVTSS2SI — Convert Scalar Single-Precision FP Value to Dword Integer

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<tr>
<td>xmmreg1 to reg</td>
<td>C4: rxb0_1: 0_F 010:2D:11 reg xmmreg1</td>
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<tr>
<td>mem to reg</td>
<td>C4: rxb0_1: 0_F 010:2D:mod reg r/m</td>
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<td>xmmreglo to reg</td>
<td>C5: r_F 010:2D:11 reg xmmreglo</td>
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<td>mem to reg</td>
<td>C5: r_F 010:2D:mod reg r/m</td>
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<td>xmmreg1 to reg</td>
<td>C4: rxb0_1: 1_F 010:2D:11 reg xmmreg1</td>
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<tr>
<td>mem to reg</td>
<td>C4: rxb0_1: 1_F 010:2D:mod reg r/m</td>
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#### VCVTTSS2SI — Convert with Truncation Scalar Single-Precision FP Value to Dword Integer

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<td>C4: rxb0_1: 0_F 010:2C:11 reg xmmreg1</td>
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<tr>
<td>mem to reg</td>
<td>C4: rxb0_1: 0_F 010:2C:mod reg r/m</td>
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<tr>
<td>xmmreglo to reg</td>
<td>C5: r_F 010:2C:11 reg xmmreglo</td>
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<td>C5: r_F 010:2C:mod reg r/m</td>
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<td>C4: rxb0_1: 1_F 010:2C:11 reg xmmreg1</td>
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<tr>
<td>mem to reg</td>
<td>C4: rxb0_1: 1_F 010:2C:mod reg r/m</td>
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#### VDIVPS — Divide Packed Single-Precision Floating-Point Values

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<td>C4: rxb0_1: w xmmreg2 000:5E:11 xmmreg1 xmmreg3</td>
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<tr>
<td>xmmreg2 with mem to xmmreg1</td>
<td>C4: rxb0_1: w xmmreg2 000:5E:mod xmmreg1 r/m</td>
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<tr>
<td>xmmreglo2 with xmmreglo3 to xmmreg1</td>
<td>C5: r_xmmreglo2 000:5E:11 xmmreg1 xmmreglo3</td>
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<tr>
<td>xmmreglo2 with mem to xmmreg1</td>
<td>C5: r_xmmreglo2 000:5E:mod xmmreg1 r/m</td>
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<tr>
<td>ymmreg2 with ymmreg3 to ymmreg1</td>
<td>C4: rxb0_1: w ymmreg2 100:5E:11 ymmreg1 ymmreg3</td>
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<tr>
<td>ymmreg2 with mem to ymmreg1</td>
<td>C4: rxb0_1: w ymmreg2 100:5E:mod ymmreg1 r/m</td>
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<tr>
<td>ymmreglo2 with ymmreglo3 to ymmreg1</td>
<td>C5: r_ymmreglo2 100:5E:11 ymmreg1 ymmreglo3</td>
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<tr>
<td>ymmreglo2 with mem to ymmreg1</td>
<td>C5: r_ymmreglo2 100:5E:mod ymmreg1 r/m</td>
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#### VDIVSS — Divide Scalar Single-Precision Floating-Point Values

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<td>C5: r_xmmreglo2 010:5E:mod xmmreg1 r/m</td>
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<td><strong>VLDMXCSR — Load MXCSR Register</strong></td>
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<td>mem to MXCSR reg</td>
<td>C4: rxb0_1: w_F 000:AEmod 011 r/m</td>
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<td>C5: r_F 000:AEmod 011 r/m</td>
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<td><strong>VMAXPS — Return Maximum Packed Single-Precision Floating-Point Values</strong></td>
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<td>C5: r_xmmreglo2 010:5F:mod xmmreg1 r/m</td>
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<td><strong>VMINPS — Return Minimum Packed Single-Precision Floating-Point Values</strong></td>
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<td>C4: rxb0_1: w xmmreg2 000:5D:11 xmmreg1 xmmreg3</td>
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<td>C5: r_xmmreglo2 000:5D:11 xmmreg1 xmmreglo3</td>
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<td>C4: rxb0_1: w ymmreg2 100:5D:11 ymmreg1 ymmreg3</td>
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<td>ymmreg2 with mem to ymmreg1</td>
<td>C4: rxb0_1: w ymmreg2 100:5D:mod ymmreg1 r/m</td>
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<td>ymmreglo2 with ymmreglo3 to ymmreg1</td>
<td>C5: r_ymmreglo2 100:5D:11 ymmreg1 ymmreglo3</td>
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<tr>
<td>ymmreglo2 with mem to ymmreg1</td>
<td>C5: r_ymmreglo2 100:5D:mod ymmreg1 r/m</td>
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### VMINSS — Return Minimum Scalar Single-Precision Floating-Point Value

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<td>C4: rxb0_1: w xmmreg2 010:5D:mod xmmreg1 r/m</td>
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<td>xmmreglo2 with xmmreglo3 to xmmreg1</td>
<td>C5: r_xmmreglo2 010:5D:11 xmmreg1 xmmreglo3</td>
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<tr>
<td>xmmreglo2 with mem to xmmreg1</td>
<td>C5: r_xmmreglo2 010:5D:mod xmmreg1 r/m</td>
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### VMOVAPS— Move Aligned Packed Single-Precision Floating-Point Values

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<td>xmmreg2 to xmmreg1</td>
<td>C4: rxb0_1: w_F 000:28:11 xmmreg1 xmmreg2</td>
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<tr>
<td>mem to xmmreg1</td>
<td>C4: rxb0_1: w_F 000:28:mod xmmreg1 r/m</td>
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<tr>
<td>xmmreglo to xmmreg1</td>
<td>C5: r_F 000:28:11 xmmreg1 xmmreglo</td>
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<tr>
<td>mem to xmmreg1</td>
<td>C5: r_F 000:28:mod xmmreg1 r/m</td>
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<td>xmmreg1 to xmmreg2</td>
<td>C4: rxb0_1: w_F 000:29:11 xmmreg2 xmmreg1</td>
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<tr>
<td>xmmreg1 to mem</td>
<td>C4: rxb0_1: w_F 000:29:mod r/m xmmreg1</td>
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<tr>
<td>xmmreg1 to xmmreglo</td>
<td>C5: r_F 000:29:11 xmmreglo xmmreg1</td>
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<tr>
<td>mem to xmmreg1</td>
<td>C5: r_F 000:29:mod r/m xmmreg1</td>
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<tr>
<td>ymmreg2 to ymmreg1</td>
<td>C4: rxb0_1: w_F 100:28:11 ymmreg1 ymmreg2</td>
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<tr>
<td>mem to ymmreg1</td>
<td>C4: rxb0_1: w_F 100:28:mod ymmreg1 r/m</td>
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<td>ymmreglo to ymmreg1</td>
<td>C5: r_F 100:28:11 ymmreg1 ymmreglo</td>
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<td>C5: r_F 100:28:mod ymmreg1 r/m</td>
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<td>C4: rxb0_1: w_F 100:29:11 ymmreg2 ymmreg1</td>
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<td>C4: rxb0_1: w_F 100:29:mod r/m ymmreg1</td>
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<td>ymmreg1 to xmmreglo</td>
<td>C5: r_F 100:29:11 xmmreglo ymmreg1</td>
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<td>ymmreg1 to mem</td>
<td>C5: r_F 100:29:mod r/m ymmreg1</td>
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<tr>
<td><strong>VMOVHPS — Move High Packed Single-Precision Floating-Point Values</strong></td>
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<tr>
<td>xmmreg1 with mem to xmmreg2</td>
<td>C4: rxb0_1: w xmmreg1 000:16:mod xmmreg2 r/m</td>
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<tr>
<td>xmmreg1 with mem to xmmreglo2</td>
<td>C5: r_xmmreg1 000:16:mod xmmreglo2 r/m</td>
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<tr>
<td>xmmreg1 to mem</td>
<td>C4: rxb0_1: w_F 000:17:mod r/m xmmreg1</td>
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<td>xmmreglo to mem</td>
<td>C5: r_F 000:17:mod r/m xmmreglo</td>
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<td><strong>VMOVLHPS — Move Packed Single-Precision Floating-Point Values Low to High</strong></td>
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<td>C5: r_xmmreglo2 000:16:11 xmmreg1 xmmreglo3</td>
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<td>C5: r_xmmreg1 000:12:mod xmmreglo2 r/m</td>
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<td>xmmreg1 to mem</td>
<td>C4: rxb0_1: w_F 000:13:mod r/m xmmreg1</td>
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<td>xmmreglo to mem</td>
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<td><strong>VMOVMSKPS — Extract Packed Single-Precision Floating-Point Sign Mask</strong></td>
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<td>C4: rxb0_1: w_F 000:50:11 reg xmmreg2</td>
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<td>xmmreglo to reg</td>
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<td>ymmreglo to reg</td>
<td>C5: r_F 100:50:11 reg ymmreglo</td>
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<td><strong>VMOVNTPS — Store Packed Single-Precision Floating-Point Values Using Non-Temporal Hint</strong></td>
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<td>C5: r_F 100:2B:mod r/m ymmreglo</td>
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<td>C4: rxb0_1: w_F 010:10:mod xmmreg1 r/m</td>
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<td>C4: rxb0_1: w_F 010:11:mod r/m xmmreg1</td>
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<td>C5: r_xmmreglo2 010:11:11 xmmreg1 xmmreglo3</td>
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<td>C4: rb0_1: w ymmreg2 100:59:11 ymmreg1 ymmreg3</td>
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<td><strong>VRCPPS — Compute Reciprocals of Packed Single-Precision Floating-Point Values</strong></td>
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<td>C5: r_xmmreglo2 010:52:mod xmmreg1 r/m</td>
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<td>VSHUFPS — Shuffle Packed Single-Precision Floating-Point Values</td>
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<td>xmmreg2 with xmmreg3 to xmmreg1, imm8</td>
<td>C4: rxb0_1: w xmmreg2 000:C6:11 xmmreg1 xmmreg3: imm</td>
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<td>C5: r_ymmmreglo2 100:C6:mod ymmreg1 r/m: imm</td>
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**VSQRTPS — Compute Square Roots of Packed Single-Precision Floating-Point Values**

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**VSQRTSS — Compute Square Root of Scalar Single-Precision Floating-Point Value**

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<tr>
<td><strong>VSTMXCSR — Store MXCSR Register State</strong></td>
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<td>MXCSR to mem</td>
<td>C4: rxb0_1: w_F , 000:AE, mod , 011 , r/m</td>
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<td>MXCSR to mem</td>
<td>C5: r_F , 000:AE, mod , 011 , r/m</td>
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<td>C4: rxb0_1: w , xmmreg2 , 000:5C:11 , xmmreg1 , xmmreg3</td>
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<td>C4: rxb0_1: w , xmmreg2 , 000:5C:mod , xmmreg1 , r/m</td>
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<td>C4: rxb0_1: w , ymmreg2 , 100:5C:11 , ymmreg1 , ymmreg3</td>
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<td>C5: r_ymmreglo2 , 100:5C:11 , ymmreg1 , ymmreglo3</td>
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<td>mem with xmmreg1</td>
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<td>xmmreg2 with xmmreg3 to xmmreg1</td>
<td>C4: rxb0_1: w , xmmreg2 , 000:15:11 , xmmreg1 , xmmreg3</td>
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<td><code>xmmreg2 with xmmreg3 to xmmreg1</code></td>
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<td><code>VBROADCAST — Load with Broadcast</code></td>
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<td><code>mem to xmmreg1</code></td>
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<td>C4: <code>rxbo_2</code>: 0_F 101:1A:mod <code>ymmreg1</code> r/m</td>
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<td><code>VEXTRACTF128 — Extract Packed Floating-Point Values</code></td>
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<td><code>ymmreg2 to xmmreg1, imm8</code></td>
<td>C4: <code>rxbo_3</code>: 0_F 001:19:11 <code>xmmreg1</code> <code>ymmreg2</code>: imm</td>
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<td><code>ymmreg2 to mem, imm8</code></td>
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<td><code>VININSERTF128 — Insert Packed Floating-Point Values</code></td>
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<td><code>xmmreg3</code> and merge with <code>ymmreg2</code> to <code>ymmreg1</code>, imm8</td>
<td>C4: <code>rbx0_3: 0 ymmreg2101:18:11 ymmreg1xmmreg3: imm</code></td>
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<td>mem and merge with <code>ymmreg2</code> to <code>ymmreg1</code>, imm8</td>
<td>C4: <code>rbx0_3: 0 ymmreg2101:18:mod ymmreg1 r/m: imm</code></td>
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<td><code>xmmreg2</code> with <code>xmmreg3</code> to <code>xmmreg1</code></td>
<td>C4: <code>rbx0_2: 0 xmmreg2 001:0D:11 xmmreg1 xmmreg3</code></td>
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<td>C4: <code>rbx0_2: 0 xmmreg2 001:0D:mod xmmreg1 r/m</code></td>
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<td>C4: <code>rbx0_2: 0 ymmreg2 101:0D:11 ymmreg1 ymmreg3</code></td>
</tr>
<tr>
<td><code>ymmreg2</code> with mem to <code>ymmreg1</code></td>
<td>C4: <code>rbx0_2: 0 ymmreg2 101:0D:mod ymmreg1 r/m</code></td>
</tr>
<tr>
<td><code>xmmreg2</code> to <code>xmmreg1</code>, imm</td>
<td>C4: <code>rbx0_3: 0_F 001:05:11 xmmreg1 xmmreg2: imm</code></td>
</tr>
<tr>
<td>mem to <code>xmmreg1</code>, imm</td>
<td>C4: <code>rbx0_3: 0_F 001:05:mod xmmreg1 r/m: imm</code></td>
</tr>
<tr>
<td><code>ymmreg2</code> to <code>ymmreg1</code>, imm</td>
<td>C4: <code>rbx0_3: 0_F 101:05:11 ymmreg1 ymmreg2: imm</code></td>
</tr>
<tr>
<td>mem to <code>ymmreg1</code>, imm</td>
<td>C4: <code>rbx0_3: 0_F 101:05:mod ymmreg1 r/m: imm</code></td>
</tr>
<tr>
<td><strong>VPERMILPS — Permute Single-Precision Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2</code> with <code>xmmreg3</code> to <code>xmmreg1</code></td>
<td>C4: <code>rbx0_2: 0 xmmreg2 001:0C:11 xmmreg1 xmmreg3</code></td>
</tr>
<tr>
<td><code>xmmreg2</code> with mem to <code>xmmreg1</code></td>
<td>C4: <code>rbx0_2: 0 xmmreg2 001:0C:mod xmmreg1 r/m</code></td>
</tr>
<tr>
<td><code>xmmreg2</code> to <code>xmmreg1</code>, imm</td>
<td>C4: <code>rbx0_3: 0_F 001:04:11 xmmreg1 xmmreg2: imm</code></td>
</tr>
<tr>
<td>mem to <code>xmmreg1</code>, imm</td>
<td>C4: <code>rbx0_3: 0_F 001:04:mod xmmreg1 r/m: imm</code></td>
</tr>
<tr>
<td><code>ymmreg2</code> with <code>ymmreg3</code> to <code>ymmreg1</code></td>
<td>C4: <code>rbx0_2: 0 ymmreg2 101:0C:11 ymmreg1 ymmreg3</code></td>
</tr>
<tr>
<td><code>ymmreg2</code> with mem to <code>ymmreg1</code></td>
<td>C4: <code>rbx0_2: 0 ymmreg2 101:0C:mod ymmreg1 r/m</code></td>
</tr>
<tr>
<td><code>ymmreg2</code> to <code>ymmreg1</code>, imm</td>
<td>C4: <code>rbx0_3: 0_F 101:04:11 ymmreg1 ymmreg2: imm</code></td>
</tr>
<tr>
<td>mem to <code>ymmreg1</code>, imm</td>
<td>C4: <code>rbx0_3: 0_F 101:04:mod ymmreg1 r/m: imm</code></td>
</tr>
<tr>
<td><strong>VPERM2F128 — Permute Floating-Point Values</strong></td>
<td></td>
</tr>
<tr>
<td><code>ymmreg2</code> with <code>ymmreg3</code> to <code>ymmreg1</code></td>
<td>C4: <code>rbx0_3: 0 ymmreg2 101:06:11 ymmreg1 ymmreg3: imm</code></td>
</tr>
<tr>
<td><code>ymmreg2</code> with mem to <code>ymmreg1</code></td>
<td>C4: <code>rbx0_3: 0 ymmreg2 101:06:mod ymmreg1 r/m: imm</code></td>
</tr>
<tr>
<td><strong>VTESTPD/VTESTPS — Packed Bit Test</strong></td>
<td></td>
</tr>
<tr>
<td><code>xmmreg2</code> to <code>xmmreg1</code></td>
<td>C4: <code>rbx0_2: 0_F 001:0E:11 xmmreg2 xmmreg1</code></td>
</tr>
<tr>
<td>mem to <code>xmmreg1</code></td>
<td>C4: <code>rbx0_2: 0_F 001:0E:mod xmmreg2 r/m</code></td>
</tr>
<tr>
<td><code>ymmreg2</code> to <code>ymmreg1</code></td>
<td>C4: <code>rbx0_2: 0_F 101:0E:11 ymmreg2 ymmreg1</code></td>
</tr>
</tbody>
</table>
### INSTRUCTION FORMATS AND ENCODINGS

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>mem to ymmreg1</td>
<td>C4: rb0_2: 0_F 101:0E:mod ymmreg2 r/m</td>
</tr>
<tr>
<td>xmmreg2 to xmmreg1</td>
<td>C4: rb0_2: 0_F 001:0F:11 xmmreg1 xmmreg2: imm</td>
</tr>
<tr>
<td>mem to xmmreg1</td>
<td>C4: rb0_2: 0_F 001:0F:mod xmmreg1 r/m: imm</td>
</tr>
<tr>
<td>ymmreg2 to ymmreg1</td>
<td>C4: rb0_2: 0_F 101:0F:11 ymmreg1 ymmreg2: imm</td>
</tr>
<tr>
<td>mem to ymmreg1</td>
<td>C4: rb0_2: 0_F 101:0F:mod ymmreg1 r/m: imm</td>
</tr>
</tbody>
</table>

**NOTES:**
1. The term “lo” refers to the lower eight registers, 0-7
B.17 FLOATING-POINT INSTRUCTION FORMATS AND ENCODINGS

Table B-35 shows the five different formats used for floating-point instructions. In all cases, instructions are at least two bytes long and begin with the bit pattern 11011.

Table B-38. General Floating-Point Instruction Formats

<table>
<thead>
<tr>
<th>Instruction</th>
<th>First Byte</th>
<th>Second Byte</th>
<th>Optional Fields</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>11011</td>
<td>OPA 1</td>
<td>mod 1 OPB r/m</td>
</tr>
<tr>
<td>2</td>
<td>11011</td>
<td>MF OPA mod</td>
<td>OPB r/m s-i-b disp</td>
</tr>
<tr>
<td>3</td>
<td>11011</td>
<td>d P OPA 1 1</td>
<td>OPB R ST(i)</td>
</tr>
<tr>
<td>4</td>
<td>11011</td>
<td>0 0 1 1</td>
<td>1 1 OP</td>
</tr>
<tr>
<td>5</td>
<td>11011</td>
<td>0 1 1 1</td>
<td>1 1 OP</td>
</tr>
</tbody>
</table>

MF = Memory Format
00 = 32-bit real
01 = 32-bit integer
10 = 64-bit real
11 = 16-bit integer
P = Pop
0 = Do not pop stack
1 = Pop stack after operation
d = Destination
0 = Destination is ST(0)
1 = Destination is ST(i)

The Mod and R/M fields of the ModR/M byte have the same interpretation as the corresponding fields of the integer instructions. The SIB byte and disp (displacement) are optionally present in instructions that have Mod and R/M fields. Their presence depends on the values of Mod and R/M, as for integer instructions.

Table B-36 shows the formats and encodings of the floating-point instructions.

Table B-39. Floating-Point Instruction Formats and Encodings

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2XM1 - Compute 2^{ST(0)} - 1</td>
<td>11011 001 : 1111 0000</td>
</tr>
<tr>
<td>FABS - Absolute Value</td>
<td>11011 001 : 1110 0001</td>
</tr>
<tr>
<td>FADD - Add</td>
<td></td>
</tr>
</tbody>
</table>
### Table B-39. Floating-Point Instruction Formats and Encodings (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) ← ST(0) + 32-bit memory</td>
<td>11011 000 : mod 000 r/m</td>
</tr>
<tr>
<td>ST(0) ← ST(0) + 64-bit memory</td>
<td>11011 100 : mod 000 r/m</td>
</tr>
<tr>
<td>ST(d) ← ST(0) + ST(i)</td>
<td>11011 d00 : 11 000 ST(i)</td>
</tr>
<tr>
<td>FADDP – Add and Pop</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(0) + ST(i)</td>
<td>11011 110 : 11 000 ST(i)</td>
</tr>
<tr>
<td>FBLD – Load Binary Coded Decimal</td>
<td>11011 111 : mod 100 r/m</td>
</tr>
<tr>
<td>FBSTP – Store Binary Coded Decimal and Pop</td>
<td>11011 111 : mod 110 r/m</td>
</tr>
<tr>
<td>FCHS – Change Sign</td>
<td>11011 001 : 1110 0000</td>
</tr>
<tr>
<td>FCLEX – Clear Exceptions</td>
<td>11011 011 : 1110 0010</td>
</tr>
<tr>
<td>FCOM – Compare Real</td>
<td></td>
</tr>
<tr>
<td>32-bit memory</td>
<td>11011 000 : mod 010 r/m</td>
</tr>
<tr>
<td>64-bit memory</td>
<td>11011 100 : mod 010 r/m</td>
</tr>
<tr>
<td>ST(i)</td>
<td>11011 000 : 11 010 ST(i)</td>
</tr>
<tr>
<td>FCOMP – Compare Real and Pop</td>
<td></td>
</tr>
<tr>
<td>32-bit memory</td>
<td>11011 000 : mod 011 r/m</td>
</tr>
<tr>
<td>64-bit memory</td>
<td>11011 100 : mod 011 r/m</td>
</tr>
<tr>
<td>ST(i)</td>
<td>11011 000 : 11 011 ST(i)</td>
</tr>
<tr>
<td>FCOMPP – Compare Real and Pop Twice</td>
<td>11011 110 : 11 011 001</td>
</tr>
<tr>
<td>FCOMIP – Compare Real, Set EFLAGS, and Pop</td>
<td>11011 111 : 1110 110 ST(i)</td>
</tr>
<tr>
<td>FCOS – Cosine of ST(0)</td>
<td>11011 001 : 1111 1111</td>
</tr>
<tr>
<td>FDECSTP – Decrement Stack-Top Pointer</td>
<td>11011 001 : 1111 0110</td>
</tr>
<tr>
<td>FDIV – Divide</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(0) ÷ 32-bit memory</td>
<td>11011 000 : mod 110 r/m</td>
</tr>
<tr>
<td>ST(0) ← ST(0) ÷ 64-bit memory</td>
<td>11011 100 : mod 110 r/m</td>
</tr>
<tr>
<td>ST(d) ← ST(0) ÷ ST(i)</td>
<td>11011 d00 : 1111 R ST(i)</td>
</tr>
<tr>
<td>FDIVP – Divide and Pop</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(0) ÷ ST(i)</td>
<td>11011 110 : 1111 1 ST(i)</td>
</tr>
<tr>
<td>FDIVR – Reverse Divide</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← 32-bit memory ÷ ST(0)</td>
<td>11011 000 : mod 111 r/m</td>
</tr>
<tr>
<td>ST(0) ← 64-bit memory ÷ ST(0)</td>
<td>11011 100 : mod 111 r/m</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>ST(d) ← ST(i) ÷ ST(0)</td>
<td>11011 d00 : 1111 R ST(i)</td>
</tr>
<tr>
<td>FDIVRP - Reverse Divide and Pop</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(i) ÷ ST(0)</td>
<td>11011 110 : 1111 0 ST(i)</td>
</tr>
<tr>
<td>FFREE - Free ST(i) Register</td>
<td>11011 101 : 1100 0 ST(i)</td>
</tr>
<tr>
<td>FIADD - Add Integer</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(0) + 16-bit memory</td>
<td>11011 110 : mod 000 r/m</td>
</tr>
<tr>
<td>ST(0) ← ST(0) + 32-bit memory</td>
<td>11011 010 : mod 000 r/m</td>
</tr>
<tr>
<td>FICOM - Compare Integer</td>
<td></td>
</tr>
<tr>
<td>16-bit memory</td>
<td>11011 110 : mod 010 r/m</td>
</tr>
<tr>
<td>32-bit memory</td>
<td>11011 010 : mod 010 r/m</td>
</tr>
<tr>
<td>FICOMP - Compare Integer and Pop</td>
<td></td>
</tr>
<tr>
<td>16-bit memory</td>
<td>11011 110 : mod 011 r/m</td>
</tr>
<tr>
<td>32-bit memory</td>
<td>11011 010 : mod 011 r/m</td>
</tr>
<tr>
<td>FIDIV</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(0) ÷ 16-bit memory</td>
<td>11011 110 : mod 110 r/m</td>
</tr>
<tr>
<td>ST(0) ← ST(0) ÷ 32-bit memory</td>
<td>11011 010 : mod 110 r/m</td>
</tr>
<tr>
<td>FIDIVR</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← 16-bit memory ÷ ST(0)</td>
<td>11011 110 : mod 111 r/m</td>
</tr>
<tr>
<td>ST(0) ← 32-bit memory ÷ ST(0)</td>
<td>11011 010 : mod 111 r/m</td>
</tr>
<tr>
<td>FILD - Load Integer</td>
<td></td>
</tr>
<tr>
<td>16-bit memory</td>
<td>11011 111 : mod 000 r/m</td>
</tr>
<tr>
<td>32-bit memory</td>
<td>11011 011 : mod 000 r/m</td>
</tr>
<tr>
<td>64-bit memory</td>
<td>11011 111 : mod 101 r/m</td>
</tr>
<tr>
<td>FIMUL</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(0) × 16-bit memory</td>
<td>11011 110 : mod 001 r/m</td>
</tr>
<tr>
<td>ST(0) ← ST(0) × 32-bit memory</td>
<td>11011 010 : mod 001 r/m</td>
</tr>
<tr>
<td>FINCSTP - Increment Stack Pointer</td>
<td>11011 001 : 1111 0111</td>
</tr>
<tr>
<td>FINIT - Initialize Floating-Point Unit</td>
<td></td>
</tr>
<tr>
<td>FIST - Store Integer</td>
<td></td>
</tr>
<tr>
<td>16-bit memory</td>
<td>11011 111 : mod 010 r/m</td>
</tr>
</tbody>
</table>
## Table B-39. Floating-Point Instruction Formats and Encodings (Contd.)

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>32-bit memory</td>
<td>11011 011 : mod 010 r/m</td>
</tr>
<tr>
<td><strong>FISTP</strong> - Store Integer and Pop</td>
<td></td>
</tr>
<tr>
<td>16-bit memory</td>
<td>11011 111 : mod 011 r/m</td>
</tr>
<tr>
<td>32-bit memory</td>
<td>11011 011 : mod 011 r/m</td>
</tr>
<tr>
<td>64-bit memory</td>
<td>11011 111 : mod 111 r/m</td>
</tr>
<tr>
<td><strong>FISUB</strong></td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(0) - 16-bit memory</td>
<td>11011 110 : mod 100 r/m</td>
</tr>
<tr>
<td>ST(0) ← ST(0) - 32-bit memory</td>
<td>11011 010 : mod 100 r/m</td>
</tr>
<tr>
<td><strong>FISUBR</strong></td>
<td></td>
</tr>
<tr>
<td>ST(0) ← 16-bit memory – ST(0)</td>
<td>11011 110 : mod 101 r/m</td>
</tr>
<tr>
<td>ST(0) ← 32-bit memory – ST(0)</td>
<td>11011 010 : mod 101 r/m</td>
</tr>
<tr>
<td><strong>FLD</strong> - Load Real</td>
<td></td>
</tr>
<tr>
<td>32-bit memory</td>
<td>11011 001 : mod 000 r/m</td>
</tr>
<tr>
<td>64-bit memory</td>
<td>11011 101 : mod 000 r/m</td>
</tr>
<tr>
<td>80-bit memory</td>
<td>11011 011 : mod 010 r/m</td>
</tr>
<tr>
<td>ST(i)</td>
<td>11011 001 : 11 000 ST(i)</td>
</tr>
<tr>
<td><strong>FLD1</strong> - Load +1.0 into ST(0)</td>
<td>11011 001 : 1110 1000</td>
</tr>
<tr>
<td><strong>FLDCW</strong> - Load Control Word</td>
<td>11011 001 : mod 101 r/m</td>
</tr>
<tr>
<td><strong>FLDENV</strong> - Load FPU Environment</td>
<td>11011 001 : mod 100 r/m</td>
</tr>
<tr>
<td><strong>FLDL2E</strong> - Load log₂(ε) into ST(0)</td>
<td>11011 001 : 1110 1010</td>
</tr>
<tr>
<td><strong>FLDL2T</strong> - Load log₁₀(10) into ST(0)</td>
<td>11011 001 : 1110 1001</td>
</tr>
<tr>
<td><strong>FLDLG2</strong> - Load log₁₀(2) into ST(0)</td>
<td>11011 001 : 1110 1100</td>
</tr>
<tr>
<td><strong>FLDLN2</strong> - Load logₑ(2) into ST(0)</td>
<td>11011 001 : 1110 1101</td>
</tr>
<tr>
<td><strong>FLDPI</strong> - Load π into ST(0)</td>
<td>11011 001 : 1110 1011</td>
</tr>
<tr>
<td><strong>FLDZ</strong> - Load +0.0 into ST(0)</td>
<td>11011 001 : 1110 1110</td>
</tr>
<tr>
<td><strong>FMUL</strong> - Multiply</td>
<td></td>
</tr>
<tr>
<td>ST(0) ← ST(0) × 32-bit memory</td>
<td>11011 000 : mod 001 r/m</td>
</tr>
<tr>
<td>ST(0) ← ST(0) × 64-bit memory</td>
<td>11011 100 : mod 001 r/m</td>
</tr>
<tr>
<td>ST(d) ← ST(0) × ST(i)</td>
<td>11011 d00 : 1100 1 ST(i)</td>
</tr>
<tr>
<td><strong>FMULP</strong> - Multiply</td>
<td></td>
</tr>
<tr>
<td>ST(i) ← ST(0) × ST(i)</td>
<td>11011 110 : 1100 1 ST(i)</td>
</tr>
<tr>
<td>Instruction and Format</td>
<td>Encoding</td>
</tr>
<tr>
<td>------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>FNOP – No Operation</td>
<td>11011 001 : 1101 0000</td>
</tr>
<tr>
<td>FPATAN – Partial Arctangent</td>
<td>11011 001 : 1111 0011</td>
</tr>
<tr>
<td>FPREM – Partial Remainder</td>
<td>11011 001 : 1111 1000</td>
</tr>
<tr>
<td>FPREM1 – Partial Remainder (IEEE)</td>
<td>11011 001 : 1111 0101</td>
</tr>
<tr>
<td>FPTAN – Partial Tangent</td>
<td>11011 001 : 1111 0010</td>
</tr>
<tr>
<td>FRNDINT – Round to Integer</td>
<td>11011 001 : 1111 1100</td>
</tr>
<tr>
<td>FRSTOR – Restore FPU State</td>
<td>11011 101 : mod 100 r/m</td>
</tr>
<tr>
<td>FSAVE – Store FPU State</td>
<td>11011 101 : mod 110 r/m</td>
</tr>
<tr>
<td>FSUBP – Subtract and Pop</td>
<td>11011 110 : 1110 1 ST(i)</td>
</tr>
<tr>
<td>FSQRT – Square Root</td>
<td>11011 101 : mod 110 r/m</td>
</tr>
<tr>
<td>FRNDINT – Round to Integer</td>
<td>11011 001 : 1111 1100</td>
</tr>
<tr>
<td>FRSTOR – Restore FPU State</td>
<td>11011 101 : mod 100 r/m</td>
</tr>
<tr>
<td>FSAVE – Store FPU State</td>
<td>11011 101 : mod 110 r/m</td>
</tr>
<tr>
<td>FSUBP – Subtract and Pop</td>
<td>11011 110 : 1110 1 ST(i)</td>
</tr>
</tbody>
</table>

Table B-39. Floating-Point Instruction Formats and Encodings (Contd.)
<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSUBR – Reverse Subtract</td>
<td>ST(0) ← 32-bit memory – ST(0) 11011 000 : mod 101 r/m</td>
</tr>
<tr>
<td></td>
<td>ST(0) ← 64-bit memory – ST(0) 11011 100 : mod 101 r/m</td>
</tr>
<tr>
<td></td>
<td>ST(d) ← ST(i) – ST(0) 11011 d00 : 1110 R ST(i)</td>
</tr>
<tr>
<td>FSUBRP – Reverse Subtract and Pop</td>
<td>ST(i) ← ST(i) – ST(0) 11011 110 : 1110 0 ST(i)</td>
</tr>
<tr>
<td>FTST – Test</td>
<td>11011 001 : 1110 0100</td>
</tr>
<tr>
<td>FUCOM – Unordered Compare Real</td>
<td>11011 101 : 1110 0 ST(i)</td>
</tr>
<tr>
<td>FUCOMP – Unordered Compare Real and Pop</td>
<td>11011 101 : 1110 1 ST(i)</td>
</tr>
<tr>
<td>FUCOMPP – Unordered Compare Real and Pop Twice</td>
<td>11011 010 : 1110 1001</td>
</tr>
<tr>
<td>FUCOMI – Unordered Compare Real and Set EFLAGS</td>
<td>11011 011 : 11 101 ST(i)</td>
</tr>
<tr>
<td>FUCOMIP – Unordered Compare Real, Set EFLAGS, and Pop</td>
<td>11011 111 : 11 101 ST(i)</td>
</tr>
<tr>
<td>FXAM – Examine</td>
<td>11011 001 : 1110 0101</td>
</tr>
<tr>
<td>FXCH – Exchange ST(0) and ST(i)</td>
<td>11011 001 : 1100 1 ST(i)</td>
</tr>
<tr>
<td>FXTRACT – Extract Exponent and Significand</td>
<td>11011 001 : 1111 0100</td>
</tr>
<tr>
<td>FYL2X – ST(1) × log2(ST(0))</td>
<td>11011 001 : 1111 0001</td>
</tr>
<tr>
<td>FYL2XP1 – ST(1) × log2(ST(0) + 1.0)</td>
<td>11011 001 : 1111 1001</td>
</tr>
<tr>
<td>FWAIT – Wait until FPU Ready</td>
<td>1001 1011</td>
</tr>
</tbody>
</table>
## B.18 VMX INSTRUCTIONS

Table B-40 describes virtual-machine extensions (VMX).

### Table B-40. Encodings for VMX Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INVEPT</strong>—Invalidate Cached EPT Mappings</td>
<td>01100110 00001111 00111000 10000000: mod reg r/m</td>
</tr>
<tr>
<td><strong>INVVPID</strong>—Invalidate Cached VPID Mappings</td>
<td>01100110 00001111 00111000 10000001: mod reg r/m</td>
</tr>
<tr>
<td><strong>VMCALL</strong>—Call to VM Monitor</td>
<td>00001111 00000001 11000001</td>
</tr>
<tr>
<td><strong>VMCLEAR</strong>—Clear Virtual-Machine Control Structure</td>
<td>01100110 00001111 11000111: mod 110 r/m</td>
</tr>
<tr>
<td><strong>VMFUNC</strong>—Invoke VM Function</td>
<td>00001111 00000001 11010100</td>
</tr>
<tr>
<td><strong>VMLAUNCH</strong>—Launch Virtual Machine</td>
<td>00001111 00000001 11000110</td>
</tr>
<tr>
<td><strong>VMPTRLD</strong>—Load Pointer to Virtual-Machine Control Structure</td>
<td>00001111 11000111: mod 110 r/m</td>
</tr>
<tr>
<td><strong>VMPTRST</strong>—Store Pointer to Virtual-Machine Control Structure</td>
<td>00001111 11000111: mod 110 r/m</td>
</tr>
<tr>
<td><strong>VMREAD</strong>—Read Field from Virtual-Machine Control Structure</td>
<td>00001111 11000111: mod 111 r/m</td>
</tr>
</tbody>
</table>
### Table B-40. Encodings for VMX Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>r32 (VMCS_fieldn) to r32</td>
<td>00001111 01111000: 11 reg2 reg1</td>
</tr>
<tr>
<td>r32 (VMCS_fieldn) to mem32</td>
<td>00001111 01111000: mod r32 r/m</td>
</tr>
<tr>
<td>r64 (VMCS_fieldn) to r64</td>
<td>00001111 01111000: 11 reg2 reg1</td>
</tr>
<tr>
<td>r64 (VMCS_fieldn) to mem64</td>
<td>00001111 01111000: mod r64 r/m</td>
</tr>
<tr>
<td><strong>VMWRITE—Write Field to Virtual-Machine Control Structure</strong></td>
<td></td>
</tr>
<tr>
<td>r32 to r32 (VMCS_fieldn)</td>
<td>00001111 01111001: 11 reg1 reg2</td>
</tr>
<tr>
<td>mem32 to r32 (VMCS_fieldn)</td>
<td>00001111 01111001: mod r32 r/m</td>
</tr>
<tr>
<td>r64 to r64 (VMCS_fieldn)</td>
<td>00001111 01111001: 11 reg1 reg2</td>
</tr>
<tr>
<td>mem64 to r64 (VMCS_fieldn)</td>
<td>00001111 01111001: mod r64 r/m</td>
</tr>
<tr>
<td><strong>VMXOFF—Leave VMX Operation</strong></td>
<td></td>
</tr>
<tr>
<td>Leave VMX.</td>
<td>00001111 00000001 11000100</td>
</tr>
<tr>
<td><strong>VMXON—Enter VMX Operation</strong></td>
<td></td>
</tr>
<tr>
<td>Enter VMX.</td>
<td>11110011 00000111 11000111: mod 110 r/m</td>
</tr>
</tbody>
</table>
B.19 SMX INSTRUCTIONS

Table B-38 describes Safer Mode extensions (VMX). GETSEC leaf functions are selected by a valid value in EAX on input.

Table B-41. Encodings for SMX Instructions

<table>
<thead>
<tr>
<th>Instruction and Format</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>GETSEC—GETSEC leaf functions are selected by the value in EAX on input</td>
<td></td>
</tr>
<tr>
<td>GETSEC[CAPABILITIES].</td>
<td>00001111 00110111 (EAX= 0)</td>
</tr>
<tr>
<td>GETSEC[ENTERACCS].</td>
<td>00001111 00110111 (EAX= 2)</td>
</tr>
<tr>
<td>GETSEC[EXITAC].</td>
<td>00001111 00110111 (EAX= 3)</td>
</tr>
<tr>
<td>GETSEC[SENTER].</td>
<td>00001111 00110111 (EAX= 4)</td>
</tr>
<tr>
<td>GETSEC[SEXIT].</td>
<td>00001111 00110111 (EAX= 5)</td>
</tr>
<tr>
<td>GETSEC[PARAMETERS].</td>
<td>00001111 00110111 (EAX= 6)</td>
</tr>
<tr>
<td>GETSEC[SMCTRL].</td>
<td>00001111 00110111 (EAX= 7)</td>
</tr>
<tr>
<td>GETSEC[WAKEUP].</td>
<td>00001111 00110111 (EAX= 8)</td>
</tr>
</tbody>
</table>
INSTRUCTION FORMATS AND ENCODINGS
The two tables in this appendix itemize the Intel C/C++ compiler intrinsics and functional equivalents for the Intel MMX technology, SSE, SSE2, SSE3, and SSSE3 instructions.

There may be additional intrinsics that do not have an instruction equivalent. It is strongly recommended that the reader reference the compiler documentation for the complete list of supported intrinsics. Please refer to [http://www.intel.com/support/performancetools/](http://www.intel.com/support/performancetools/).

Table C-1 presents simple intrinsics and Table C-2 presents composite intrinsics. Some intrinsics are "composites" because they require more than one instruction to implement them.

Intel C/C++ Compiler intrinsic names reflect the following naming conventions:

```
_mm_<intrin_op>_<suffix>
```

where:

- `<intrin_op>` Indicates the intrinsics basic operation; for example, add for addition and sub for subtraction
- `<suffix>` Denotes the type of data operated on by the instruction. The first one or two letters of each suffix denotes whether the data is packed (p), extended packed (ep), or scalar (s).

The remaining letters denote the type:

- `s` single-precision floating point
- `d` double-precision floating point
- `i128` signed 128-bit integer
- `i64` signed 64-bit integer
- `u64` unsigned 64-bit integer
- `i32` signed 32-bit integer
- `u32` unsigned 32-bit integer
- `i16` signed 16-bit integer
- `u16` unsigned 16-bit integer
- `i8` signed 8-bit integer
- `u8` unsigned 8-bit integer

The variable `r` is generally used for the intrinsic's return value. A number appended to a variable name indicates the element of a packed object. For example, `r0` is the lowest word of `r`. 
The packed values are represented in right-to-left order, with the lowest value being used for scalar operations. Consider the following example operation:

```c
double a[2] = {1.0, 2.0};
__m128d t = _mm_load_pd(a);
```

The result is the same as either of the following:

```c
__m128d t = _mm_set_pd(2.0, 1.0);
__m128d t = _mm_setr_pd(1.0, 2.0);
```

In other words, the XMM register that holds the value t will look as follows:

```
<table>
<thead>
<tr>
<th></th>
<th>2.0</th>
<th>1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>64</td>
<td>127</td>
</tr>
</tbody>
</table>
```

The "scalar" element is 1.0. Due to the nature of the instruction, some intrinsics require their arguments to be immediates (constant integer literals).

To use an intrinsic in your code, insert a line with the following syntax:

```c
data_type intrinsic_name(parameters)
```

Where:

- `data_type` is the return data type, which can be either void, int, __m64, __m128, __m128d, or __m128i. Only the _mm_empty intrinsic returns void.
- `intrinsic_name` is the name of the intrinsic, which behaves like a function that you can use in your C/C++ code instead of in-lining the actual instruction.
- `parameters` represents the parameters required by each intrinsic.

### C.1 SIMPLE INTRINSICS

**NOTE**

For detailed descriptions of the intrinsics in Table C-1, see the corresponding mnemonic in Chapter 3 in the "Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A", or Chapter 4, “Instruction Set Reference, M-Z” in the "Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B".
### Table C-1. Simple Intrinsics

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Intrinsic</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDPD</td>
<td>__m128d _mm_add_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>ADDPS</td>
<td>__m128 _mm_add_ps(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>ADDSD</td>
<td>__m128d _mm_add_sd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>ADDSS</td>
<td>__m128 _mm_add_ss(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>ADDSUBPD</td>
<td>__m128d _mm_addsub_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>ADDSUBPS</td>
<td>__m128 _mm_addsub_ps(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>AESDEC</td>
<td>__m128i _mm_aesdec (__m128i, __m128i)</td>
</tr>
<tr>
<td>AESDECLAST</td>
<td>__m128i _mm_aesenclast (__m128i, __m128i)</td>
</tr>
<tr>
<td>AESENC</td>
<td>__m128i _mm_aesenc (__m128i, __m128i)</td>
</tr>
<tr>
<td>AESENCLAST</td>
<td>__m128i _mm_aesenclast (__m128i, __m128i)</td>
</tr>
<tr>
<td>AESIMC</td>
<td>__m128i _mm_aesimc (__m128i)</td>
</tr>
<tr>
<td>AESKEYGENASSIST</td>
<td>__m128i _mm_aesimc (__m128i, const int)</td>
</tr>
<tr>
<td>ANDNPD</td>
<td>__m128d _mm_andnot_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>ANDNPS</td>
<td>__m128 _mm_andnot_ps(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>ANDPD</td>
<td>__m128d _mm_and_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>ANDPS</td>
<td>__m128 _mm_and_ps(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>BLENDPD</td>
<td>__m128d _mm_blend_pd(__m128d v1, __m128d v2, const int mask)</td>
</tr>
<tr>
<td>BLENDPS</td>
<td>__m128d _mm_blend_ps(__m128 v1, __m128 v2, const int mask)</td>
</tr>
<tr>
<td>BLENDVDPD</td>
<td>__m128d _mm_blendv_pd(__m128d v1, __m128d v2, __m128d v3)</td>
</tr>
<tr>
<td>BLENDVPS</td>
<td>__m128d _mm_blendv_ps(__m128 v1, __m128 v2, __m128 v3)</td>
</tr>
<tr>
<td>CLFLUSH</td>
<td>void _mm_clflush(void const *p)</td>
</tr>
<tr>
<td>CMPPD</td>
<td>__m128d _mm_cmpeq_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmpgt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmple_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmpgt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmple_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmpeq_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmplt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmpgt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmplt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmple_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmplt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmpgt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmpgt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmplt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmplt_pd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>CMPPS</td>
<td>__m128d _mm_cmpeq_ps(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmpgt_ps(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmple_ps(__m128d a, __m128d b)</td>
</tr>
<tr>
<td></td>
<td>__m128d _mm_cmplt_ps(__m128d a, __m128d b)</td>
</tr>
</tbody>
</table>
### Table C-1. Simple Intrinsics (Contd.)

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Intrinsic</th>
</tr>
</thead>
<tbody>
<tr>
<td>__m128 _mm_cmple_ps(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpgt_ps(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpge_ps(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpneq_ps(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmplt_ps(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpgt_ps(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpge_ps(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpneq_ps(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmplt_sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmple_sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpgt_sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpge_sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpneq_sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmplt:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmple:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpgt:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpge:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpneq:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmplt:sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmple:sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpgt:sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpge:sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpneq:sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmplt:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmple:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpgt:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpge:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>__m128 _mm_cmpneq:ss(__m128 a, __m128 b)</td>
<td></td>
</tr>
<tr>
<td>int _mm_comieq_sd(__m128d a, __m128d b)</td>
<td></td>
</tr>
</tbody>
</table>

C-4 Vol. 2C
<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Intrinsic</th>
</tr>
</thead>
<tbody>
<tr>
<td>_mm_comilt_sd</td>
<td>int _mm_comilt_sd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>_mm_comile_sd</td>
<td>int _mm_comile_sd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>_mm_comigt_sd</td>
<td>int _mm_comigt_sd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>_mm_comige_sd</td>
<td>int _mm_comige_sd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>_mm_comineq_sd</td>
<td>int _mm_comineq_sd(__m128d a, __m128d b)</td>
</tr>
<tr>
<td>_mm_comieq_ss</td>
<td>int _mm_comieq_ss(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>_mm_comilt_ss</td>
<td>int _mm_comilt_ss(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>_mm_comile_ss</td>
<td>int _mm_comile_ss(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>_mm_comigt_ss</td>
<td>int _mm_comigt_ss(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>_mm_comige_ss</td>
<td>int _mm_comige_ss(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>_mm_comineq_ss</td>
<td>int _mm_comineq_ss(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>COMISS</td>
<td></td>
</tr>
<tr>
<td>_mm_crc32</td>
<td>unsigned int _mm_crc32_u8(unsigned int crc, unsigned char data)</td>
</tr>
<tr>
<td>_mm_crc32_u16</td>
<td>unsigned int _mm_crc32_u16(unsigned int crc, unsigned short data)</td>
</tr>
<tr>
<td>_mm_crc32_u64</td>
<td>unsigned int _mm_crc32_u64(unsigned int crc, unsigned int data)</td>
</tr>
<tr>
<td>CVTDQ2PD</td>
<td>__m128d_mm_cvtpd_epi32(__m128i a)</td>
</tr>
<tr>
<td>CVTDQ2PS</td>
<td>__m128_mm_cvtpd_epi32(__m128i a)</td>
</tr>
<tr>
<td>CVTPD2DQ</td>
<td>__m128i_mm_cvtpd_epi32(__m128d a)</td>
</tr>
<tr>
<td>CVTPD2PI</td>
<td>__m64_mm_cvtpd_epi32(__m128d a)</td>
</tr>
<tr>
<td>CVTPD2PS</td>
<td>__m128_mm_cvtpd_epi32(__m128d a)</td>
</tr>
<tr>
<td>CVTP2PD</td>
<td>__m128d_mm_cvtpd_epi32(__m64 a)</td>
</tr>
<tr>
<td>CVTP2PS</td>
<td>__m128d_mm_cvtpd_epi32(__m128d a, __m64 b)</td>
</tr>
<tr>
<td>CVTPS2DQ</td>
<td>__m128i_mm_cvtpd_epi32(__m128 a)</td>
</tr>
<tr>
<td>CVTPS2PD</td>
<td>__m128d_mm_cvtpd_epi32(__m128 a)</td>
</tr>
<tr>
<td>CVTS2PI</td>
<td>__m64_mm_cvtpd_epi32(__m128 a)</td>
</tr>
<tr>
<td>CVTS2SI</td>
<td>__m128d_mm_cvtsd_epi32(__m128 a)</td>
</tr>
<tr>
<td>CVTS2SS</td>
<td>__m128d_mm_cvtsd_epi32(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>CVTS2SD</td>
<td>__m128d_mm_cvtsd_epi32(__m128 a, __m128 d)</td>
</tr>
<tr>
<td>CVTS2SS</td>
<td>__m128d_mm_cvtsd_epi32(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>CVTS2SD</td>
<td>__m128d_mm_cvtsd_epi32(__m128 a, __m128 d)</td>
</tr>
<tr>
<td>CVTS2SI</td>
<td>__m128d_mm_cvtsd_epi32(__m128 a)</td>
</tr>
<tr>
<td>CVTS2SS</td>
<td>__m128d_mm_cvtsd_epi32(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>CVTS2SD</td>
<td>__m128d_mm_cvtsd_epi32(__m128 a, __m128 d)</td>
</tr>
<tr>
<td>CVTPD2DQ</td>
<td>__m128i_mm_cvtpd_epi32(__m128 d a)</td>
</tr>
</tbody>
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Table C-1. Simple Intrinsics (Contd.)
<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Intrinsic</th>
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<tbody>
<tr>
<td>CVTTPD2PI</td>
<td>__m64 __mm_cvttp_pi32(__m128d a)</td>
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<td>CVTTPS2DQ</td>
<td>__m128i __mm_cvttps_epi32(__m128 a)</td>
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<tr>
<td>CVTTPS2PI</td>
<td>__m64 __mm_cvttp_ps2pi(__m128 a)</td>
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<tr>
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<td>__m64 __mm_cvttps_pi32(__m128 a)</td>
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<td>CVTTSD2SI</td>
<td>int __mm_cvttsd_si32(__m128d a)</td>
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<tr>
<td>CVTTSS2SI</td>
<td>int __mm_cvttss_si32(__m128 a)</td>
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<td>__m64 __mm_cvtsi32_si64(int i)</td>
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<td>int __mm_cvtsi64_si32(__m64 m)</td>
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<td>DIVPD</td>
<td>__m128d __mm_div_pd(__m128d a, __m128d b)</td>
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<tr>
<td>DIVPS</td>
<td>__m128 __mm_div_ps(__m128 a, __m128 b)</td>
</tr>
<tr>
<td>DIVSD</td>
<td>__m128d __mm_div_sd(__m128d a, __m128d b)</td>
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<tr>
<td>DIVSS</td>
<td>__m128 __mm_div_ss(__m128 a, __m128 b)</td>
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<td>DPPD</td>
<td>__m128d __mm_dp_pd(__m128d a, __m128d b, const int mask)</td>
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<tr>
<td>DPPS</td>
<td>__m128 __mm_dp_ps(__m128 a, __m128 b, const int mask)</td>
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<tr>
<td>EMMS</td>
<td>int __mm_empty()</td>
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<tr>
<td>EXTRACTPS</td>
<td>int __mm_extract_ps(__m128 src, const int ndx)</td>
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<td>HADDPD</td>
<td>__m128d __mm_hadd_pd(__m128d a, __m128d b)</td>
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<td>__m128 __mm_hadd_ps(__m128 a, __m128 b)</td>
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<td>HSUBPD</td>
<td>__m128d __mm_hsub_pd(__m128d a, __m128d b)</td>
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<td>HSUBPS</td>
<td>__m128 __mm_hsub_ps(__m128 a, __m128 b)</td>
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<tr>
<td>INSERTPS</td>
<td>__m128 __mm_insert_ps(__m128 dst, __m128 src, const int ndx)</td>
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<td>LDDQU</td>
<td>__m128i __mm_lddqu_si128 (__m128i const *p)</td>
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<td>LDMXCSR</td>
<td>__mm_setcsr(unsigned int i)</td>
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<tr>
<td>LFENCE</td>
<td>int __mm_lfence(void)</td>
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<tr>
<td>MASKMOVQDQU</td>
<td>void __mm_maskmoveu_si128 (__m128i d, __m128i n, char *p)</td>
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<tr>
<td>MASKMOVQ</td>
<td>void __mm_maskmove_si64(__m64 d, __m64 n, char *p)</td>
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<td>MAXPD</td>
<td>__m128d __mm_max_pd(__m128d a, __m128d b)</td>
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<td>__m128 __mm_max_ps(__m128 a, __m128 b)</td>
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<td>__m128d __mm_max_sd(__m128d a, __m128d b)</td>
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<tr>
<td>MAXSS</td>
<td>__m128 __mm_max_ss(__m128 a, __m128 b)</td>
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<tr>
<td>MFENCE</td>
<td>int __mm_mfence(void)</td>
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<td>__m128d __mm_min_pd(__m128d a, __m128d b)</td>
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<td>__m128 __mm_min_ps(__m128 a, __m128 b)</td>
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<td>__m128d __mm_min_sd(__m128d a, __m128d b)</td>
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<tr>
<td>MINSS</td>
<td>__m128 __mm_min_ss(__m128 a, __m128 b)</td>
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### Table C-1. Simple Intrinsics (Contd.)

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<thead>
<tr>
<th>Mnemonic</th>
<th>Intrinsic</th>
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<tbody>
<tr>
<td>MONITOR</td>
<td>void _mm_monitor(void const *p, unsigned extensions, unsigned hints)</td>
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<td>MOVAPD</td>
<td>_m128d _mm_load_pd(double * p), void _mm_store_pd(double *p, __m128d a)</td>
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<tr>
<td>MOVAPS</td>
<td>_m128 _mm_load_ps(float * p), void _mm_store_ps(float *p, __m128 a)</td>
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<td>MOVD</td>
<td>_m128i _mm_cvtsi32_si128(int a), int _mm_cvtsi128_si32(__m128i a), _m64 _mm_cvtsi32_si64(int a), int _mm_cvtsi64_si32(__m64 a)</td>
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<tr>
<td>MOVDDUP</td>
<td>_m128d _mm_movdup_pd(__m128d a), _m128d _mm_loaddup_pd(double const * dp)</td>
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<td>MOVDQA</td>
<td>_m128i _mm_load_si128(__m128i * p), void _mm_store_si128(__m128i *p, __m128i a)</td>
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<tr>
<td>MOVDQU</td>
<td>_m128i _mm_loadu_si128(__m128i * p), void _mm_storeu_si128(__m128i *p, __m128i a)</td>
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<tr>
<td>MOVDPD2Q</td>
<td>_m64 _mm_movepi64_pi64(__m128i a)</td>
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<tr>
<td>MOVHLP</td>
<td>_m128d _mm_loadh_pd(__m128d a), void _mm_storeh_pd(double * p, __m128d a)</td>
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<tr>
<td>MOVHPS</td>
<td>_m128d _mm_loadh_pi(__m128d a, __m64 * p)</td>
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<td>_m128d _mm_loadl_pd(__m128d a, double * p)</td>
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<td>_m128d _mm_loadl_pi(__m128d a, __m64 * p)</td>
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<td>_m128d _mm_loadl_pd(__m128d a, double * p)</td>
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<td>int _mm_movemask_pd(__m128d a)</td>
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<td>int _mm_movemask_ps(__m128d a)</td>
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<td>MOVQ</td>
<td>_m128d _mm_loadl_epi64(__m128d * p)</td>
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Table C-1. Simple Intrinsics (Contd.)

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<td>void_mm_store_epi64(_,m128i * p, __m128i a)</td>
<td>__m128i_mm_move_epi64(_,m128i a)</td>
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<td>__m128i_mm_movepi64_epi64(_,m64 a)</td>
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<td>__m128d_mm_load_sd(double * p)</td>
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<td>__m128d_mm_move_sd(_,m128d a, __m128d b)</td>
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<td>__m128_mm_movhdup_ps(_,m128 a)</td>
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<td>MOVSLDUP</td>
<td>__m128_mm_moveldup_ps(_,m128 a)</td>
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<td>__m128_mm_load_ss(float * p)</td>
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<td>void_mm_store_ss(float * p, __m128 a)</td>
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<td>MOVUPD</td>
<td>__m128d_mm_loadu_pd(double * p)</td>
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<td>MOVVUPS</td>
<td>__m128_mm_loadu_ps(float * p)</td>
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<td>__m128i_mm_mpsadbw_epi8(_,m128i s1, __m128i s2, const int mask)</td>
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<td>__m128d_mm_mul_pd(_,m128d a, __m128d b)</td>
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<td>__m128i_mm_mul_ss(_,m128 a, __m128 b)</td>
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<td>__m128_mm_mul_ss(_,m128 a, __m128 b)</td>
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<td>void_mm_mwait(unsigned extensions, unsigned hints)</td>
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<td>__m128_mm_or_ps(_,m128 a, __m128 b)</td>
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<td>__m128i_mm_packss_epi16(_,m128i m1, __m128i m2)</td>
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<td>PACKUSDW</td>
<td>__m128i_mm_packus_epi32(_,m128i m1, __m128i m2)</td>
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<td>PACKUSWB</td>
<td>__m128i_mm_packus_epi16(_,m128i m1, __m128i m2)</td>
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### Intel® C/C++ Compiler Intrinsics and Functional Equivalents

#### Table C-1. Simple Intrinsics (Contd.)

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<td>PACKUSWB</td>
<td><code>__m64 _mm_packs_pu16(__m64 m1, __m64 m2)</code></td>
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<td><code>__m128i _mm_add_epi8(__m128i m1, __m128i m2)</code></td>
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<td>PADDB</td>
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<td><code>__m64 _mm_alignr_epi8(__m64 m1, __m64 m2)</code></td>
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<td><code>__m128i _mm_alignr_epi8(__m128i m1, __m128i m2)</code></td>
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<td><code>__m128i _mm_and_si128(__m128i m1, __m128i m2)</code></td>
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<td>PAUSE</td>
<td>void _mm_pause(void)</td>
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<td><code>__m128i _mm_blend_epi8(__m128i v1, __m128i v2, __m128i mask)</code></td>
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<td>Mnemonic</td>
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<td>__m128i _mm_cmpeq_epi32(__m128i m1, __m128i m2)</td>
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<td>PCMPEQD</td>
<td>__m64 _mm_cmpeq_pi32(__m64 m1, __m64 m2)</td>
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<td>int _mm_cmpestri(__m128i a, int la, __m128i b, int lb, const int mode)</td>
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<td>__m64 _mm_cmpgt_pi32(__m64 m1, __m64 m2)</td>
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<td>PEXTRB</td>
<td>int _mm_extract_epi8(__m128i src, const int ndx)</td>
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<td>__int64 _mm_extract_epi64 (_m128i src, const int ndx)</td>
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<td>PEXTRW</td>
<td>int _mm_extract_epi16(_m128i a, int n)</td>
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<td>PEXTRW</td>
<td>int _mm_extract_pi16(_m64 a, int n)</td>
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<td>int _mm_extract_epi16 (_m128i src, int ndx)</td>
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<td>__m64 _mm_hadd_pi32 (__m64 a, __m64 b)</td>
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<td>int _mm_movemask_pl8(__m64 a)</td>
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<td>_m128i _mm_mullo_epi32(__m128i m1, __m128i m2)</td>
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### Table C-1. Simple Intrinsics (Contd.)

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<td>_mm_or_si128(_mm128i m1, _mm128i m2)</td>
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<td>void _mm_prefetch(char *a, int sel)</td>
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### Table C-1. Simple Intrinsics (Contd.)

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<td>int __mm_testc_si128(__m128i s1, __m128i s2)</td>
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<td>int __mm_testncz_si128(__m128i s1, __m128i s2)</td>
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<td>__m128_mm_floor_pd(__m128d s1)</td>
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## Table C-1. Simple Intrinsics (Contd.)

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<td>void_mm_sfence(void)</td>
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<td>_m128d_mm_shuffle_pd(_m128d a, _m128d b, unsigned int imm8)</td>
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<tr>
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<td>_m128_mm_shuffle_ps(_m128 a, _m128 b, unsigned int imm8)</td>
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<td>_m128_mm_sqrt_ss(_m128 a)</td>
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<td>_mm_getcsr(void)</td>
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<tr>
<td>SUBSS</td>
<td>_m128_mm_sub_ss(_m128 a, _m128 b)</td>
</tr>
<tr>
<td>UCOMISD</td>
<td>int _mm_ucomieq_sd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomilt_sd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomile_sd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomigt_sd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomige_sd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomineq_sd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td>UCOMISS</td>
<td>int _mm_ucomieq_ss(_m128 a, _m128 b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomilt_ss(_m128 a, _m128 b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomile_ss(_m128 a, _m128 b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomigt_ss(_m128 a, _m128 b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomige_ss(_m128 a, _m128 b)</td>
</tr>
<tr>
<td></td>
<td>int _mm_ucomineq_ss(_m128 a, _m128 b)</td>
</tr>
<tr>
<td>UNPCKHPD</td>
<td>_m128d_mm_unpackhi_pd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td>UNPCKHPS</td>
<td>_m128_mm_unpackhi_ps(_m128 a, _m128 b)</td>
</tr>
<tr>
<td>UNPCKLPD</td>
<td>_m128d_mm_unpacklo_pd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td>UNPCKLPS</td>
<td>_m128_mm_unpacklo_ps(_m128 a, _m128 b)</td>
</tr>
<tr>
<td>XORPD</td>
<td>_m128d_mm_xor_pd(_m128d a, _m128d b)</td>
</tr>
<tr>
<td>XORPS</td>
<td>_m128_mm_xor_ps(_m128 a, _m128 b)</td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Intrinsic</th>
</tr>
</thead>
<tbody>
<tr>
<td>(composite)</td>
<td>__m128i_mm_set_epi64(__m64 q1, __m64 q0)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_set_epi32(int i3, int i2, int i1, int i0)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_set_epi16(short w7, short w6, short w5, short w4, short w3, short w2, short w1, short w0)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_set_epi8(char w15, char w14, char w13, char w12, char w11, char w10, char w9, char w8, char w7, char w6, char w5, char w4, char w3, char w2, char w1, char w0)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_set1_epi64(__m64 q)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_set1_epi32(int a)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_set1_epi16(short a)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_set1_epi8(char a)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_setr_epi64(__m64 q1, __m64 q0)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_setr_epi32(int i3, int i2, int i1, int i0)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_setr_epi16(short w7, short w6, short w5, short w4, short w3, short w2, short w1, short w0)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128i_mm_setzero_si128()</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128_mm_set_ps1(float w)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128_mm_set1_ps(float w)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128_mm_setl_pd(double w)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128d_mm_set_sd(double w)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128d_mm_set_pd(double z, double y)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128d_mm_set_ps(float z, float y, float x, float w)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128d_mm_setr_pd(double z, double y)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128_mm_setr_ps(float z, float y, float x, float w)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128d_mm_setzero_pd(void)</td>
</tr>
<tr>
<td>(composite)</td>
<td>__m128d_mm_setzero_ps(void)</td>
</tr>
<tr>
<td>MOVSD + shuffle</td>
<td>__m128d_mm_load_d_pd(double * p)</td>
</tr>
<tr>
<td>MOVSD + shuffle</td>
<td>__m128d_mm_load1_d_pd(double * p)</td>
</tr>
<tr>
<td>MOVSS + shuffle</td>
<td>__m128_mm_load_d_ps1(float * p)</td>
</tr>
<tr>
<td>MOVSS + shuffle</td>
<td>__m128_mm_load1_d_ps(float * p)</td>
</tr>
<tr>
<td>MOVAPD + shuffle</td>
<td>__m128d_mm_loadr_d_pd(double * p)</td>
</tr>
<tr>
<td>MOVAPD + shuffle</td>
<td>__m128d_mm_loadr_d_ps(float * p)</td>
</tr>
<tr>
<td>MOVSD + shuffle</td>
<td>void_mm_store1_d_pd(double *p, __m128d a)</td>
</tr>
</tbody>
</table>
### Table C-2. Composite Intrinsics (Contd.)

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Intrinsic</th>
</tr>
</thead>
</table>
| MOVSS + shuffle | void _mm_store_ps1(float * p, __m128 a)  
                 | void _mm_store1_ps(float *p, __m128 a)   |
| MOVAPD + shuffle | __mm_storer_pd(double * p, __m128d a) |
| MOVAPS + shuffle | __mm_storer_ps(float * p, __m128 a)     |
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