CS 536 Fall 2009 - Homework 1
Due 9/17/2009 in class
Total Points : 100

Instructions. Submit your homework electronically in a text or PDF file. Please use the blackboard to submit your homework by Sept 17th of 2009 before class. Late submission will not be accepted, nor will we allow group submissions. You can discuss with other students, but please write your own answers. Please also indicate the set of students you have discussed the problems with in case you collaborate.
To receive credit, all submissions should contain this statement at the beginning: "By turning in this homework submission, I certify that this work was done solely by me." Questions about this homework should be directed to the TAs or the Professor, not to fellow classmates.

Problem 1 (5pts)

Suppose users share a 6Mbps link. Also suppose each user transmits continuously at 2Mbps when transmitting, but each user transmits only 25% of the time.

a. When circuit switching is used, how many users can be supported?

b. For the remainder of this problem, suppose packet switching is used. Why will there be essentially no queueing delay before the link if three or fewer users transmit at the same time? Why will there be a queueing delay if four users transmit at the same time?

c. Suppose there are 10 users. Find the probability that at any given time, exactly n users are transmitting simultaneously. (*Hint:* Use the binomial distribution.)

d. Find the probability that there are 4 or more users transmitting simultaneously.

Problem 2 (10pts)

In this problem, you have to write some clock recovery code for a receiver that is receiving a 4-5 encoded bit stream. Assume the preamble has been received and the receiver is basically in sync except for a possible clock drift. Thus the receiver is sampling according to its current clock (see Figure 1) and should be expecting transitions only at what it thinks are bit boundaries (see dotted lines in the Figure). However, because of clock drift, the actual transitions may be a little off (see the solid line in Figure).

Remember that in 4-5 coding you are guaranteed to get *at least* one transition in every 5 consecutive bits; however, you may get *up to* 5 transitions. You may want to write your code as follows. Receive a group of 5 bits and sample them according to the current receiver clock.

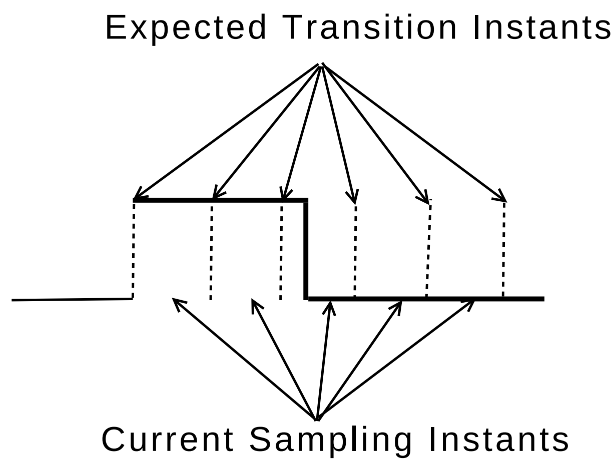

Figure 1: Expected and current transition instants

Keep track of the transitios you actually receive during these 5 bits and use this to adjust the receiver clocks for the next group of 5 bits. You can assume there is no noise and only clock drift.

Problem 3 (5pts)

Suppose two nodes start to transmit at the same time a packet of length L over a broadcast channel of rate R. Denote the propagation delay between the two nodes as d_{prop}. Will there be a collision if $d_{prop} < L/R$? Why or why not?

Problem 4 (10pts)

Suppose three active nodes — A, B, and C — are competing for access to a channel using slotted ALOHA. Assume each node has an infinite number of packets to send. Each node attempts to transmit in each slot with probability p. The first slot is numbered slot 1, the second slot is numbered slot 2, and so on.

1. What is the probability that node A succeeds for the first time in slot 4 ?
2. What is the probability that some node (either A, B, or C) succeeds in slot 2 ?
3. What is the probability that the first success occurs in slot 4 ?
4. What is the efficiency of this three-node system ?

Problem 5 (20pts)

In this problem, you will derive the efficiency of a CSMA/CD-like multiple access protocol. In this protocol, time is slotted and all adapters are synchronized to the slots. Unlike slotted ALOHA, however, the length of a slot (in seconds) is much less than a frame time (the time to transmit a frame). Let S be the length of a slot. Suppose all frames are of constant length $L = kRS$, where R is the transmission rate of the channel, k is a large integer. Suppose there are N nodes, each with an infinite number of frames to send. We also assume that $d_{prop} < S$, so that each node can detect a collision before the end of a slot time. The protocol is as follows:

- If, for a given slot, no node has possession of the channel, all nodes contend for the channel; in particular, each node transmits in the slot with probability p. If exactly one node transmits in the slot, that node takes possession of the channel for the subsequent $k-1$ slots and transmits its entire frame.
- If some node has possession of the channel, all other nodes refrain from transmitting until the node that possesses the channel has finished transmitting its frame. Once this node has transmitted its frame, all nodes contend for the channel.

Note that the channel alternates between two states: the productive state, which lasts exactly k slots, and the nonproductive state, which lasts for a random number of slots. Clearly, the channel efficiency is the ratio of $k/(k+x)$, where x is the expected number of consecutive unproductive slots.

1. For fixed N and p, determine the efficiency of this protocol.
2. For fixed N, determine the p that maximizes the efficiency.
3. Using the p (which is a function of N) found in (b), determine the efficiency as N approaches infinity.
4. Show that this efficiency approaches 1 as the frame length becomes large.

Problem 6 (10pts)

Suppose two nodes, A and B, are attached to opposite ends of a 1800 m cable, and that they each have one frame of 1,000 bits (including all headers and preambles) to send to each other. Both nodes attempt to transmit at time $t = 0$. Suppose there are five repeaters between A and B, each inserting a 20-bit delay. Assume that the transmission rate is 10 Mbps, and CSMA/CD with backoff intervals of multiples of 512 bits is used. After the first collision, A draws $K = 0$ and B draws $K = 1$ in the exponential backoff protocol. Ignore the jam signal and the 96-bit time delay.

1. What is the one-way propagation delay (including repeater delays) between A and B in seconds ? Assume the signal propagation speed is $2 \cdot 10^8$ m/sec.
2. At what time (in seconds) is A's packet completely delivered to B ?
3. Now suppose that only A has a packet to send and that the repeaters are replaced with switches. Suppose that each switch has a 40-bit processing delay in addition to a store-and-forward delay. At what time, in seconds, is A's packet delivered to B ?

Problem 7 (20pts)

While it is standard to represent messages and the CRC generator G in terms of bit strings, another popular representation based on polynomials is probably better for analysis and is explained below. Consider two bit strings 101 and 011, we can represent them as x^2+1 and $x+1$ respectively. Notice that if the i-th bit position is a 1, then we have a x^i term in the polynomial. Adding these polynomials using normal arithmetic is x^2+x+2, but in our case, we use mod 2 arithmetic (EX-OR). Thus, we can get rid of the painful carries and thus will lead to x^2+x in mod 2 arithmetic as a result of adding x^2+1 and $x+1$.

1. In this polynomial arithmetic, a bit error at positions i correspond to adding x^i to the original polynomial. If the CRC polynomial $G(x)$ has at least two terms, is it possible that this sum of the message and the bit error is divisible by $G(x)$? Explain your answer using polynomial arithmetic ?

2. Show that odd bit error polynomials (that is number of bit errors is odd, e.g., 1 bit error polynomial will be x^i, 3 bit errors will be $x^i + x^j + x^k$ and so on) are never divisible by $x+1$. [Hint: Use the reduction $x^i + x^j = x^i(1 + x^{(j-i)})$ so you really need to check for reduced polynomials. Substitute $x = 1$ in the polynomial E and then use proof by contradiction]

3. If the CRC generator polynomial is such that it is a multiple of $x + 1$, then can it catch all odd bit errors ? Justify.

4. What do burst errors of length k starting at position i correspond to ? If $k \leq d$, where d is the degree of the CRC polynomial, can we catch all k bit burst errors ? Justify.

Problem 8 (10pts)

Let's consider the operation of a learning switch in the context of the network shown below in Figure 2:

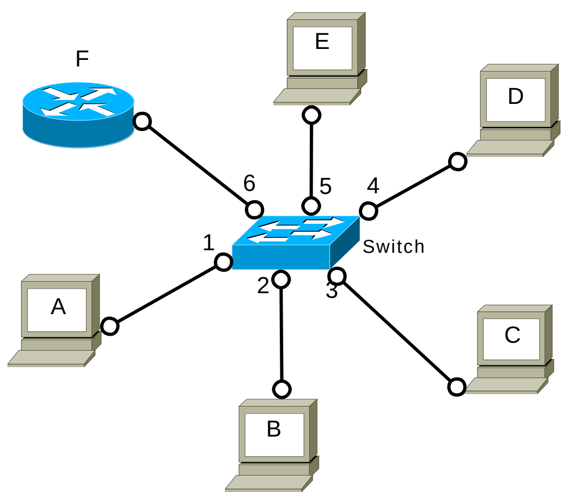

Figure 2: Sample topology for a learning switch

Suppose that (i) A sends a frame to D, (ii) D replies with a frame to A, (iii) C sends a frame to D, (iv) D replies with a frame to C. The switch table is initially empty. Show the state of the switch table before and after each of these events. For each of these events, identify the link(s) on which the transmitted frame will be forwarded, and briefly justify your answers. (Note, for the purposes of the table, let the letter represent the interface link/MAC address).

Problem 9 (10pts)

It often happens that a node knows the higher layer address of another node and needs to know its Data Link address. Suppose someone builds an introduction service to do this, that works as follows. An intro server has a well known multicast address, say INTRO. A node X that wishes to know the Data Link address corresponding to higher level address H, sends a LAN frame with destination address INTRO and with its own source address X, but with H in the data portion of the frame. When the server gets the frame, it looks up the Data Link address corresponding to H (say Y). It then forwards the original frame to Y by changing the destination address from INTRO to Y . When Y gets the frame, Y knows Xs address from the source address and so can send a reply directly to X. When X gets such a reply, X also knows the Data Link address of Y. This protocol works fine on a LAN. But it can fail in an Extended LAN with transparent bridges.

1. Describe a topology and a scenario in which this protocol fails.

2. How can you fix the introduction protocol to work in an Extended LAN?